dRICH Electronics and Integration towards the Future

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on behalf of the sipm4eic-elettronica group
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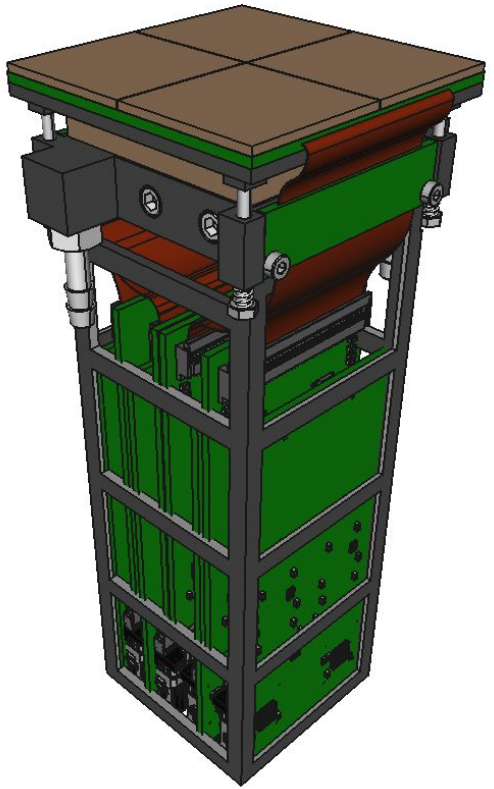
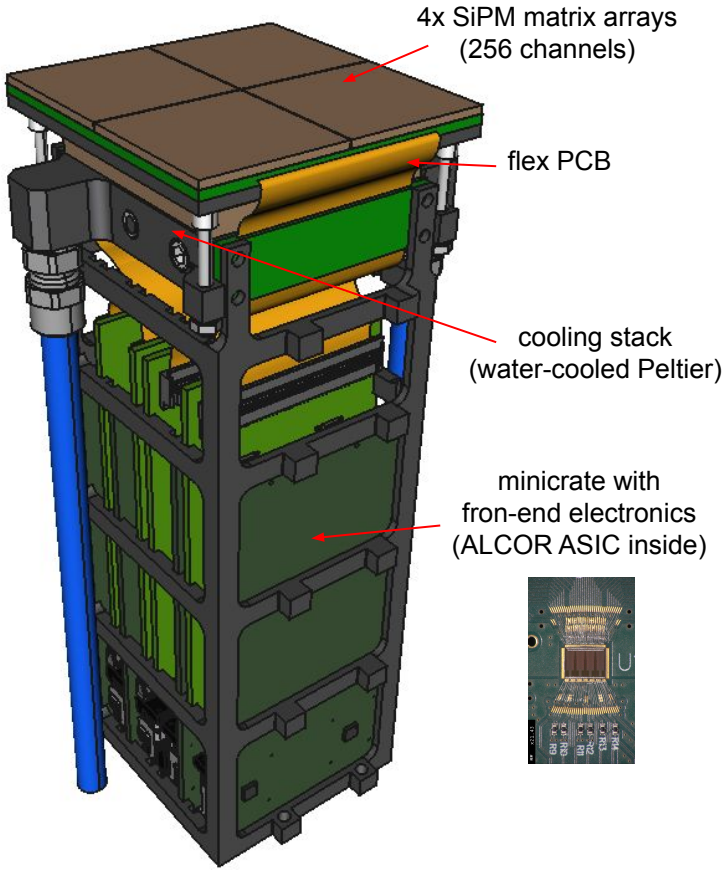
extracted from the presentation at the dRICH meeting, 3 May 2023

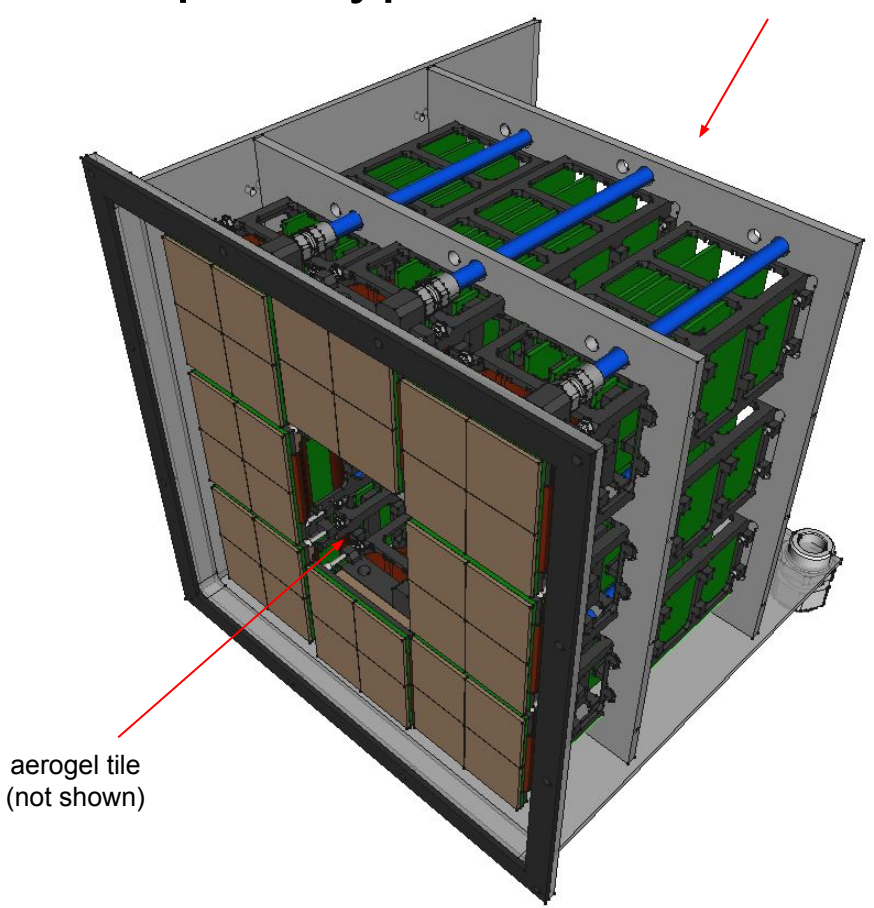
the present (2023)



EIC ePIC-dRICH SiPM photodetector prototype



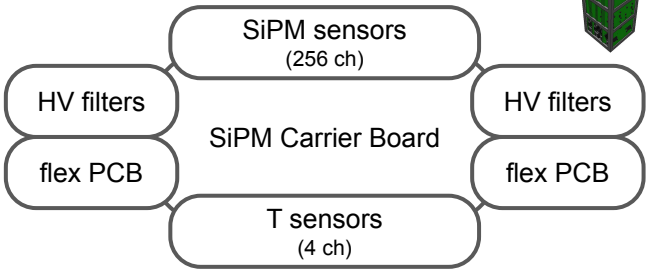
prototype PhotoDetector Unit (PDU-v2)

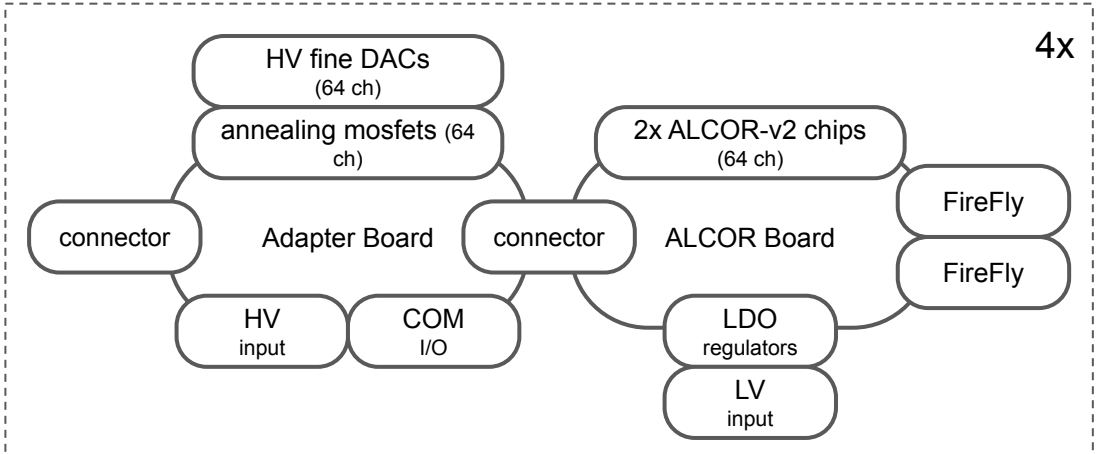


Readout Box

prototype photodetector unit

main components and devices





inside

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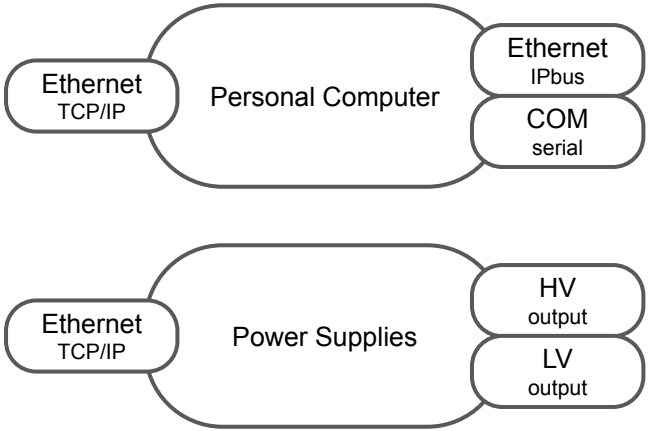
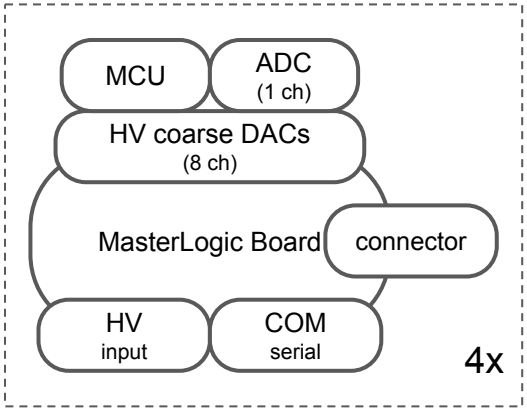
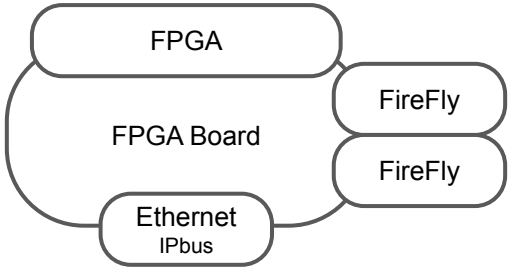
outside

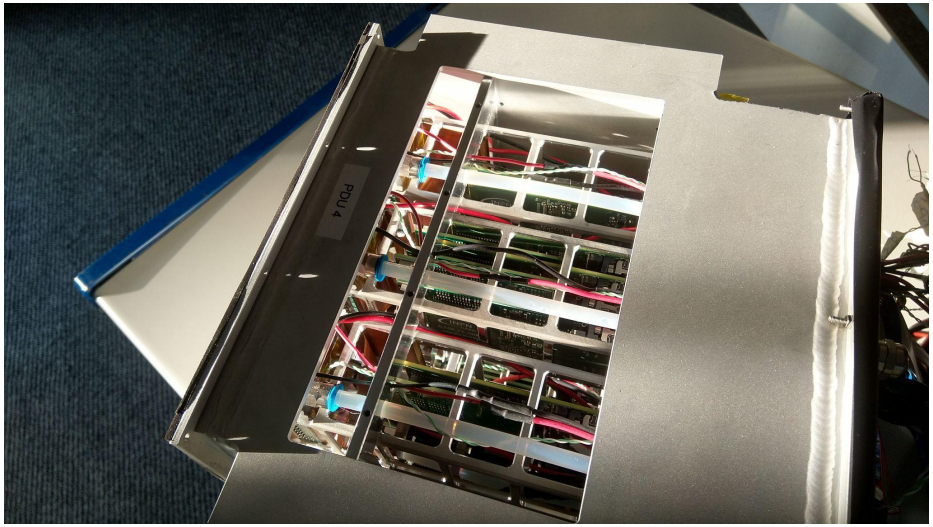




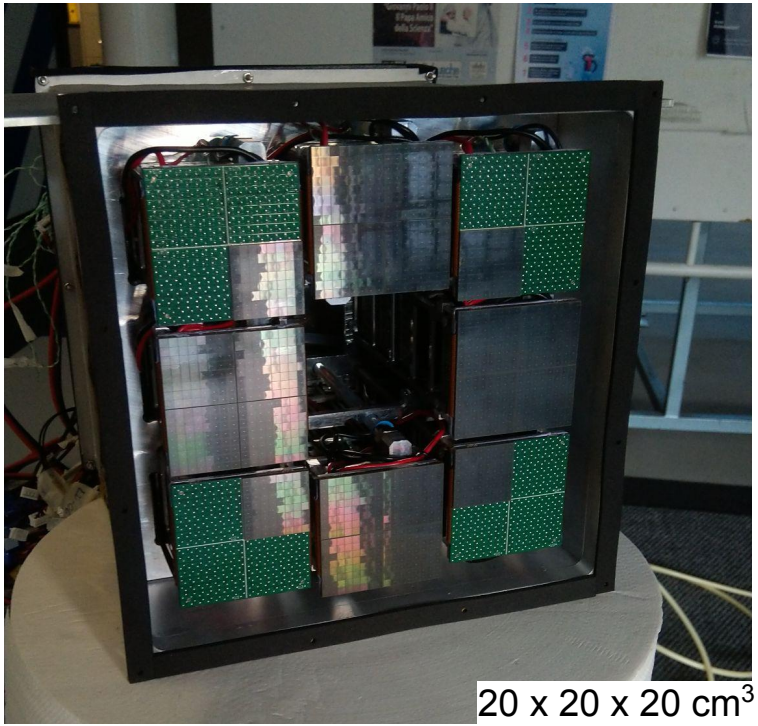


EIC ePIC-dRICH SiPM photodetector prototype

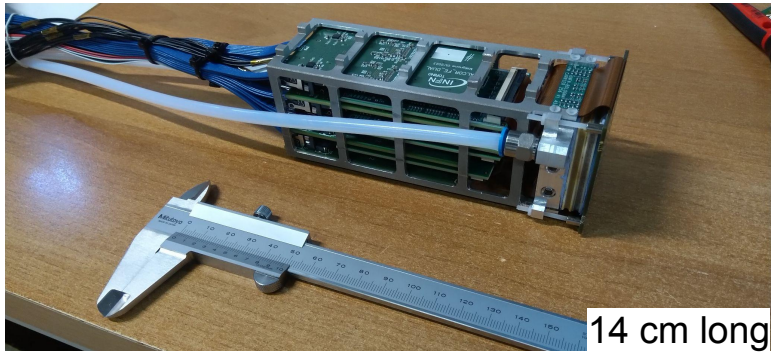
Readout Box (top)



Readout Box (front)

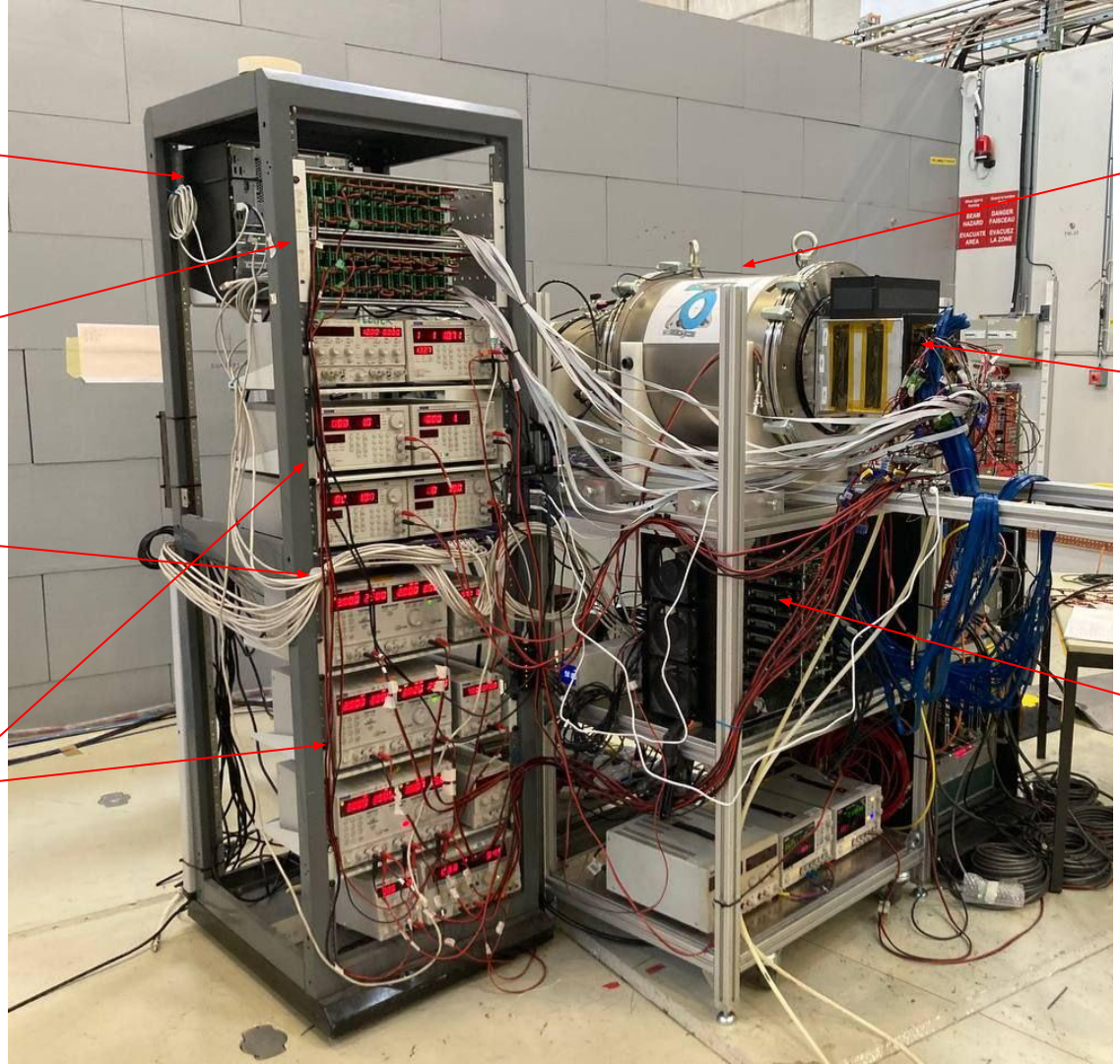


20 x 20 x 20 cm^3



14 cm long

PDU

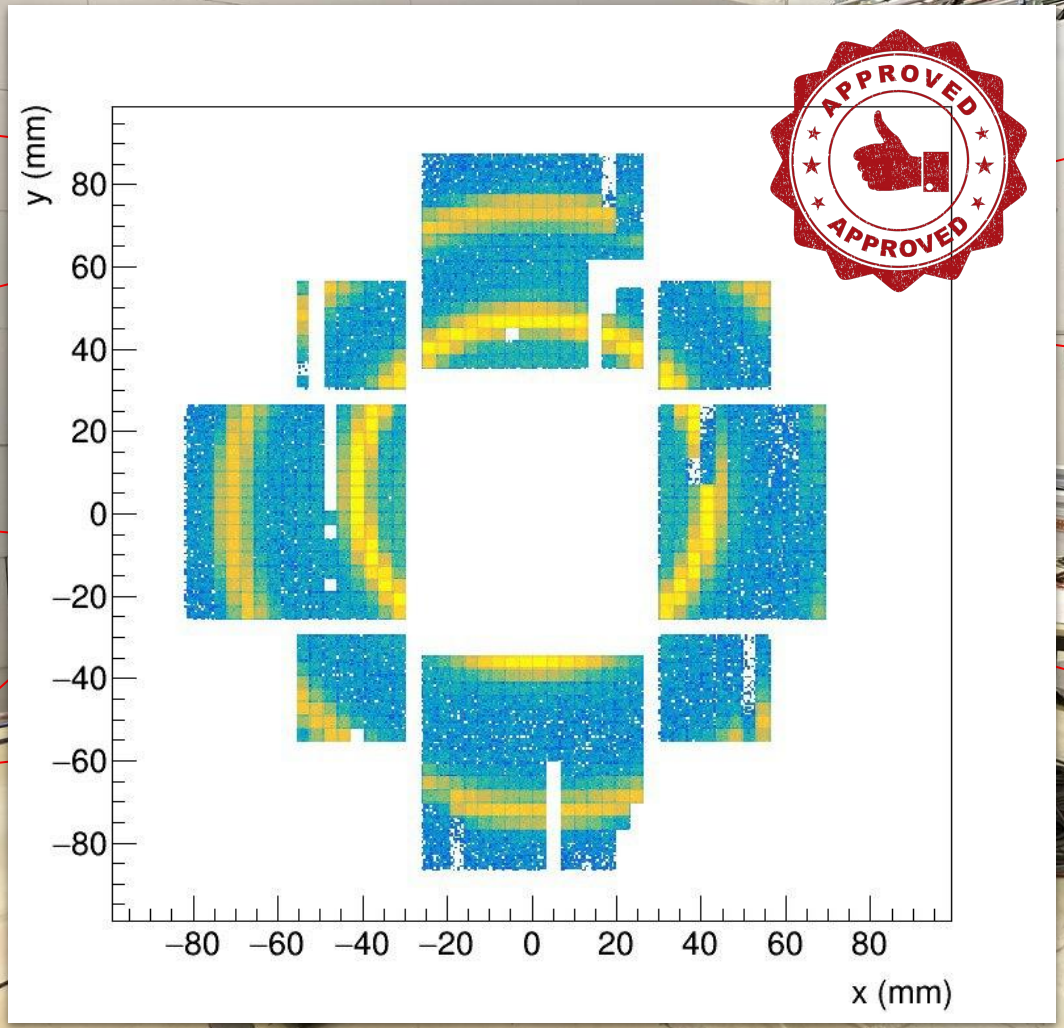

DAQ and DCS computers
auxiliary control electronics crates
gigabit ETH switch for DAQ and DCS
low voltage and high voltage power supplies
dRICH prototype
SiPM photodetector readout box
DAQ FPGAs and clock distribution

DAQ and DCS computers

auxiliary control electronics crates

gigabit ETH switch for DAQ and DCS

low voltage and high voltage power supplies

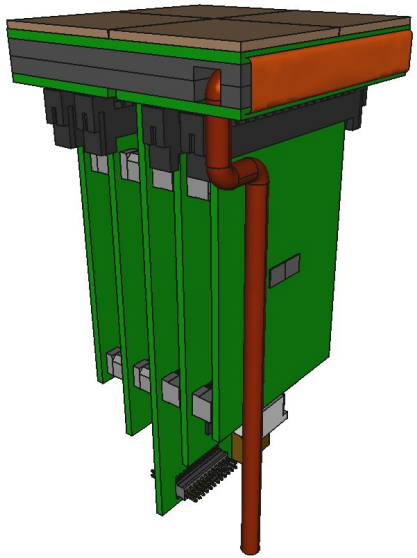


dRICH prototype

SiPM photodetector readout box

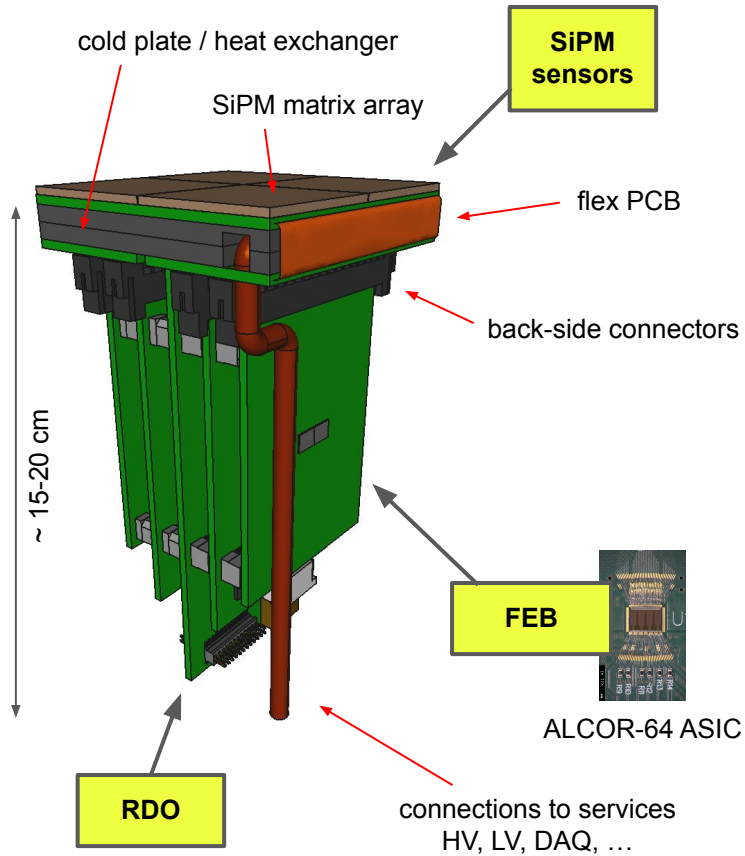
DAQ FPGAs and clock distribution

the future (2025)



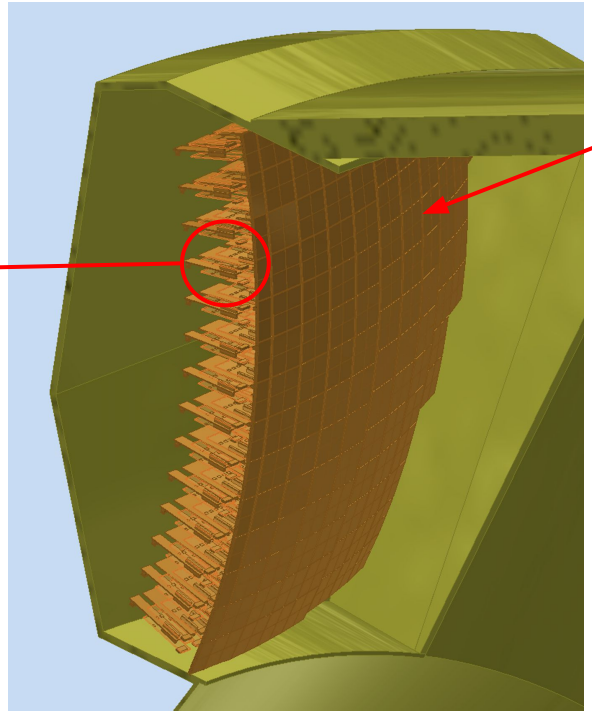
Photodetector unit

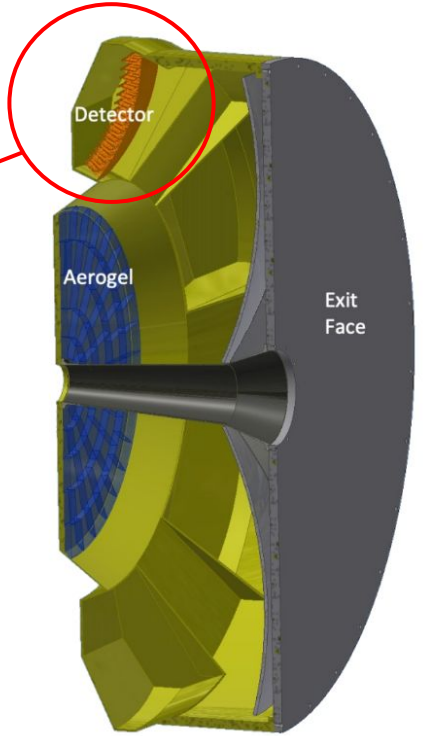
conceptual design of final layout



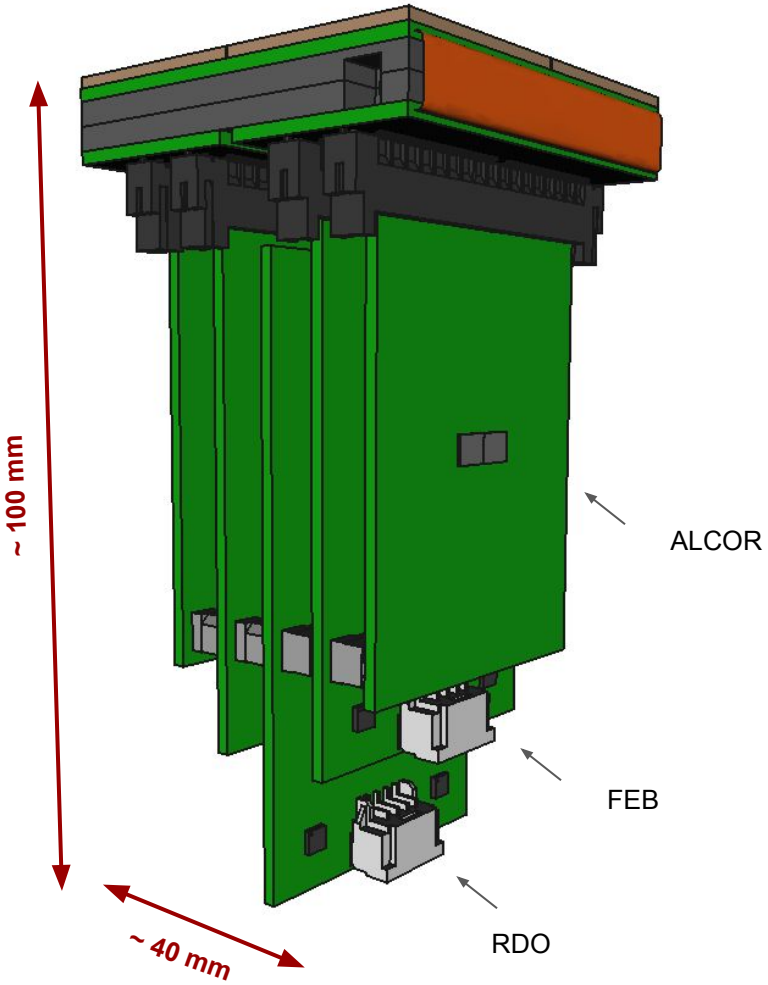
SiPM sensor matrices mounted on carrier PCB board

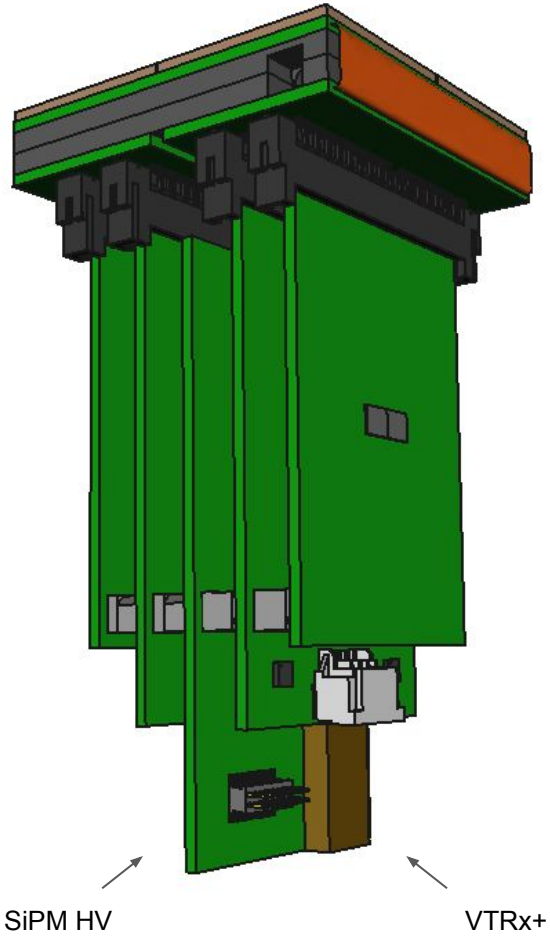
- 4x 64-channel SiPM array device (256 channels) for each unit
- 1248 photodetector units for full dRICH readout
  - 4992 SiPM matrix arrays (8x8)
  - 4992 ALCOR-64 chips
  - 319488 readout channels





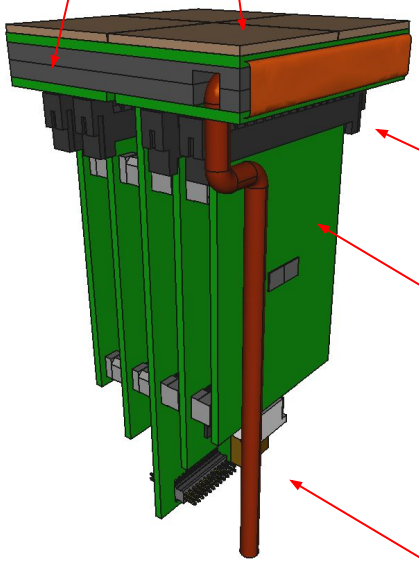
256-channels RDO, 2+2 ALCOR-64 mezzanines





PDU electronics

initial ideas to be further developed



SiPM sensors (256 ch)

SiPM Carrier Board

T sensors (4 ch)

flex PCB

flex PCB

HV filters

HV filters

connector

4x FEB

1x ALCOR-64 chips (64 ch)

FEB Board

annealing mosfets (64 ch)

connector

connector

connector

connector

FPGA

LDO regulators

RDO Board

ADC (4 ch)

MCU

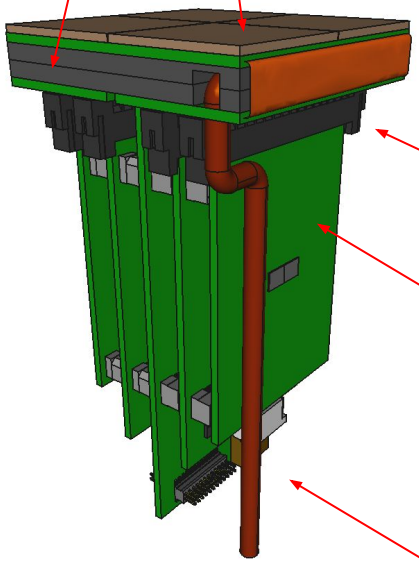
DAQ fibre link

HV input

LV input

Develop RDO prototype

one of the goals for 2024 electronics



SiPM sensors (256 ch)

SiPM Carrier Board

T sensors (4 ch)

flex PCB

flex PCB

HV filters

HV filters

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4x FEB

1x ALCOR-64 chips (64 ch)

FEB Board

annealing mosfets (64 ch)

connector

connector

connector

connector

FPGA

LDO regulators

RDO Board

ADC (4 ch)

MCU

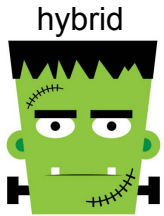
DAQ fibre link

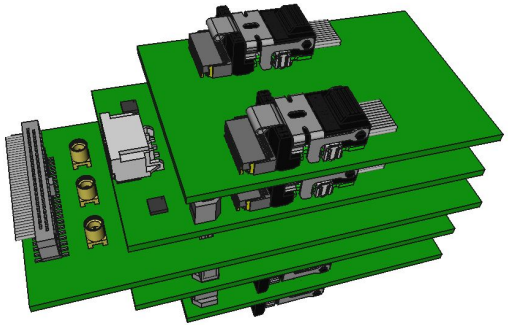
HV input

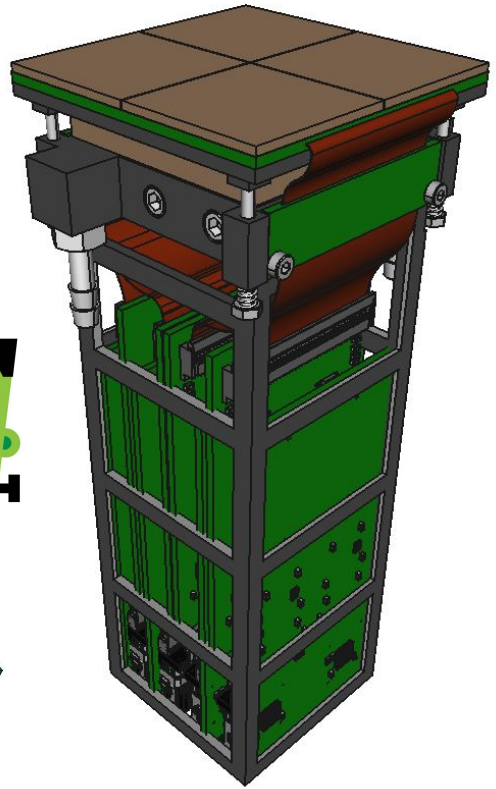
LV input

target October 2024 beam test

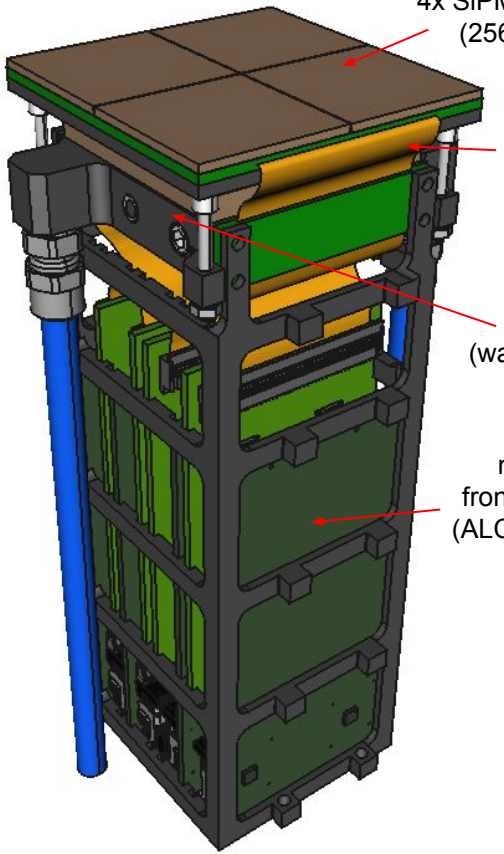
next year (2024)



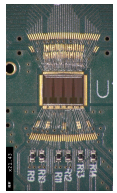




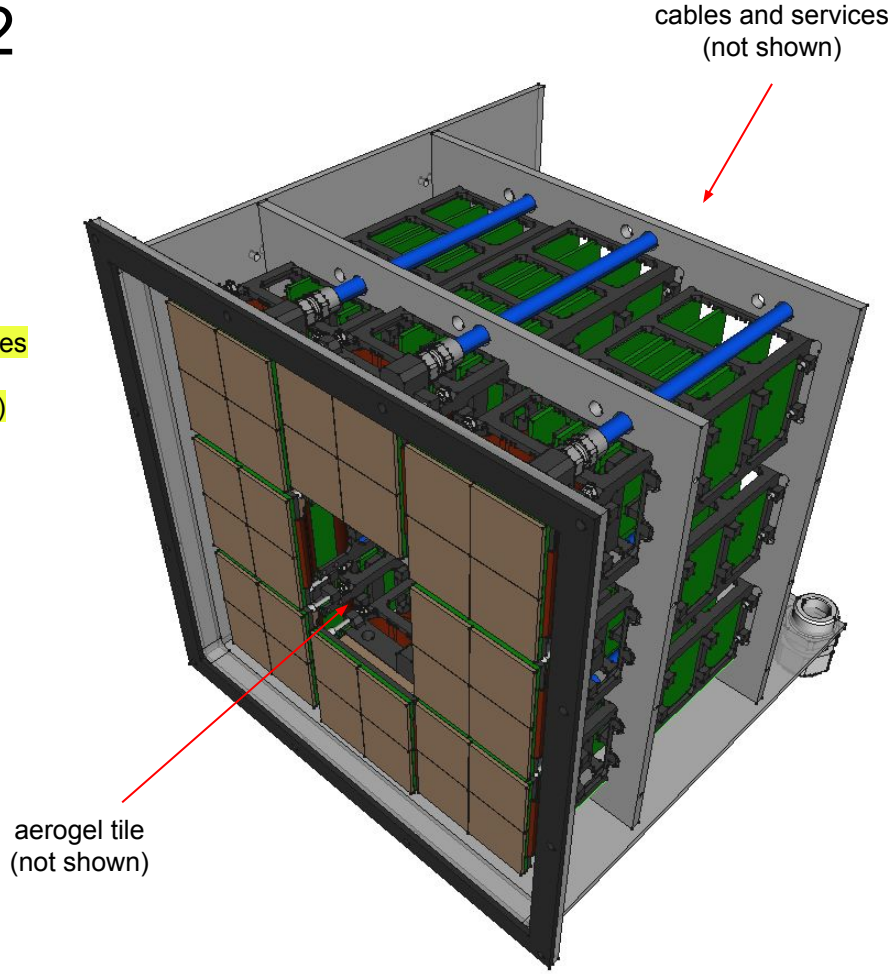
Use the same prototype PDU-v2



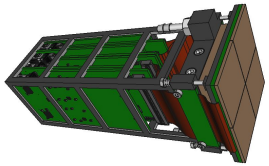
remove Peltier modules
fluid-based cooling
(siliconic, T = -40 C)



PhotoDetector Unit (PDU-v2)

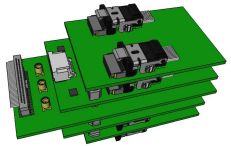


Readout Box layout might differ
to match a full-scale dRICH prototype



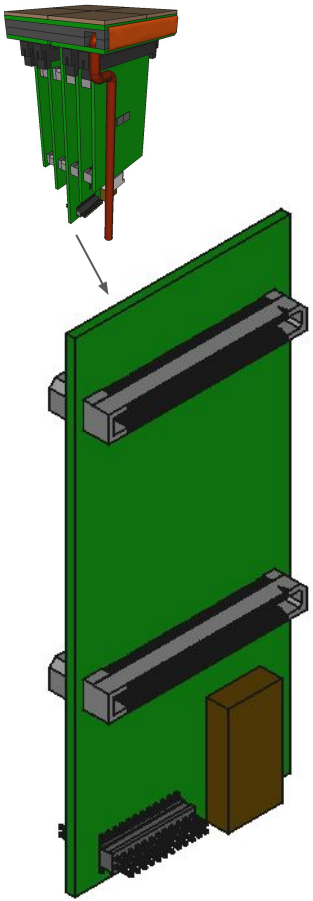
SiPM photodetector readout box
(PDU-v2 inside)

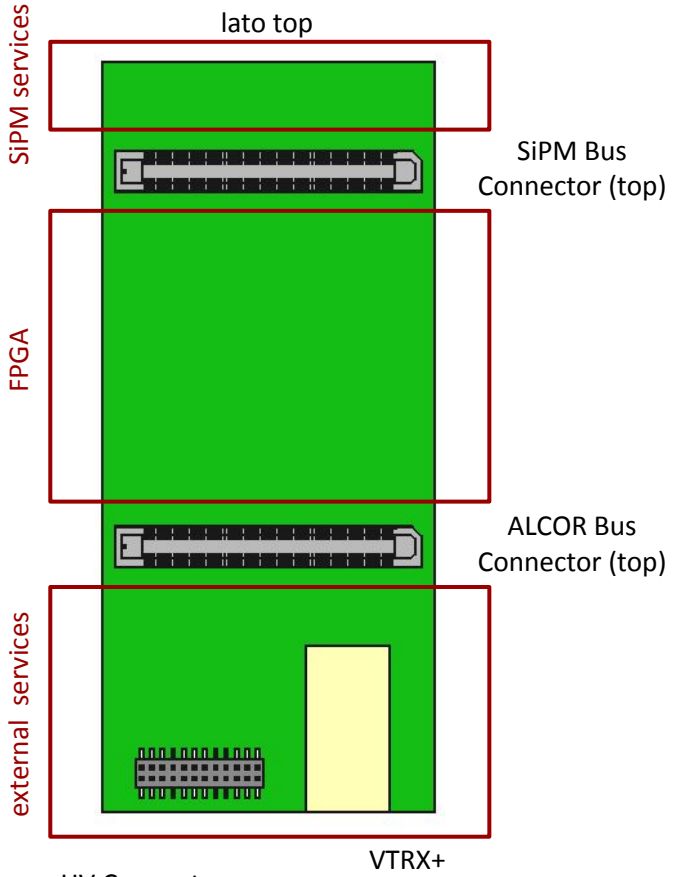
replace stack of commercial FPGAs with prototype RDOs

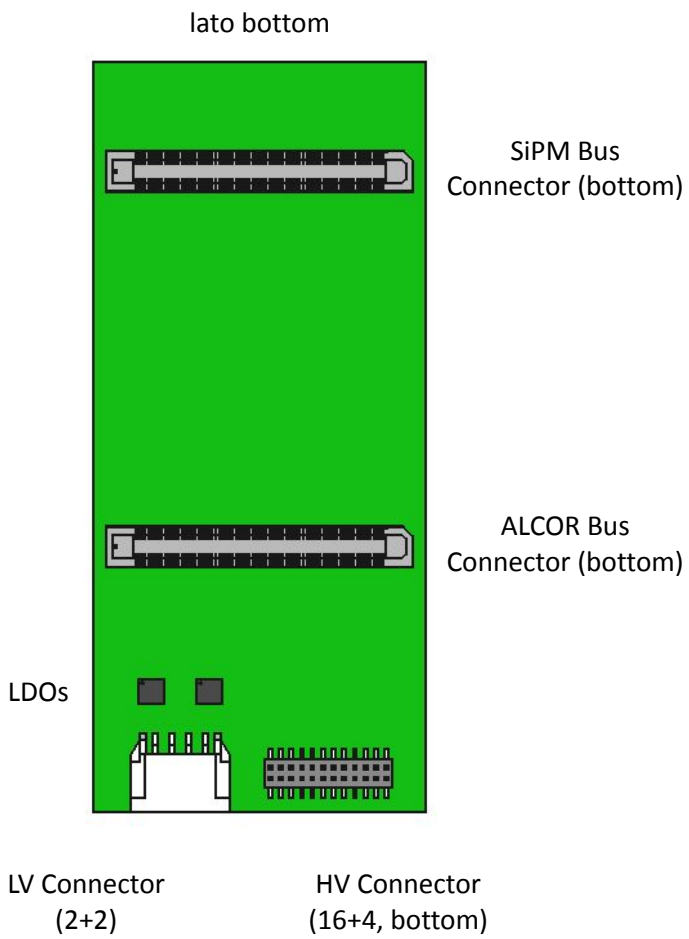


Prototype RDO

this is just a concept, see slides of Pietro & Davide for real details



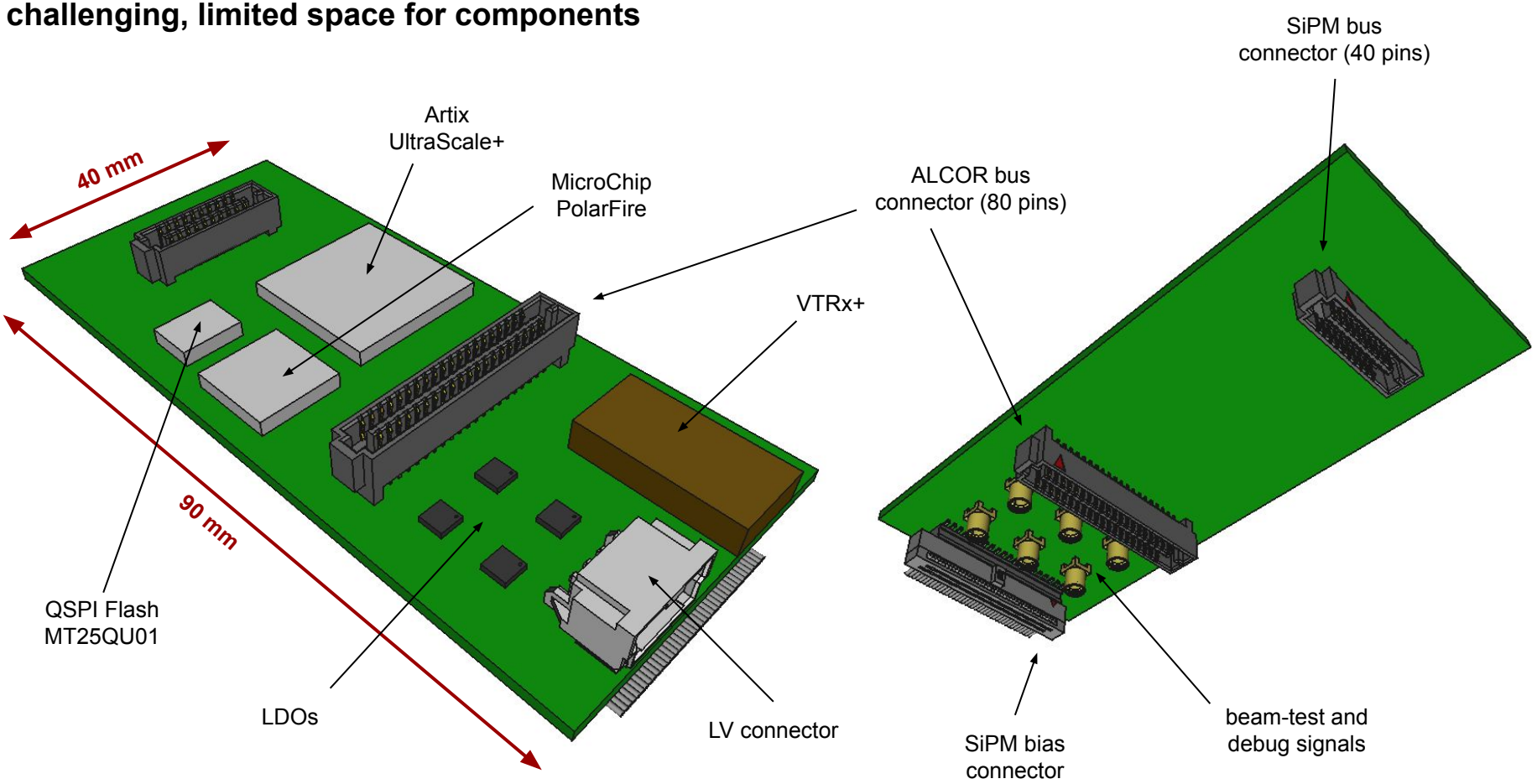




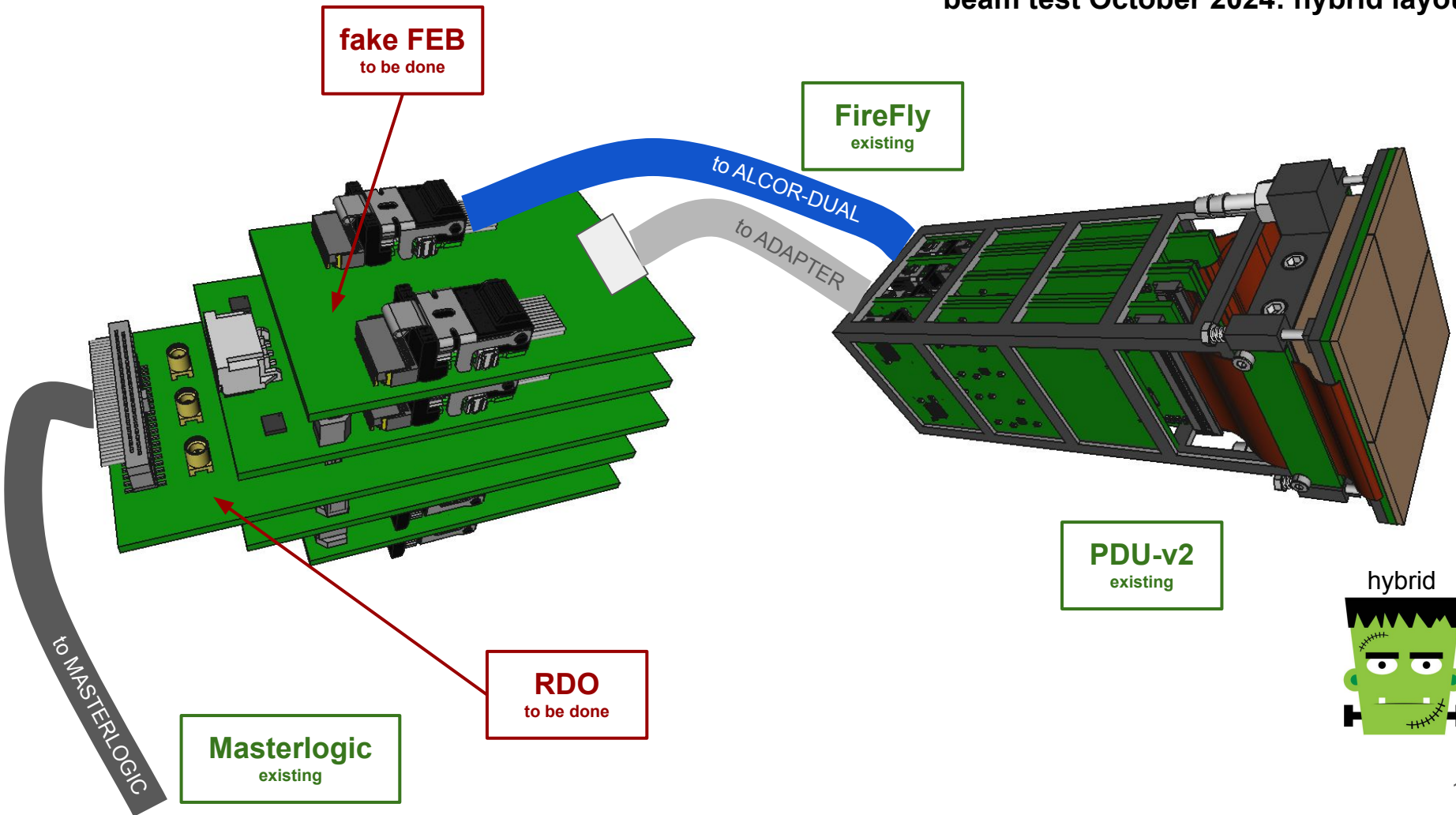
Prototype RDO

imaginative layout with real-size components

challenging, limited space for components



beam test October 2024: hybrid layout



LV power considerations

this is preliminary, need to move towards definition of requirements

- **ALCOR**
  - analog: 1.2 V
  - digital: 1.2 V, 2.5 V
    - keep analog separated from digital
    - yes, because of noise!
- **RDO**
  - main FPGA: 0.85, 1.2, 1.8 V
  - scrubber: 1.0, 1.8 V
  - VTRx+: 1.2, 2.5 V
    - is 2.5 V needed?
  - FLASH: 1.8 V
  - other electronics: 3.3 V
    - is 3.3 V needed?

~ 13 W / PDU
2.7 kW / dRICH sector
16.5 kW total