dRICH DAQ: RDO and ePIC DAQ 2024 plans and beyond

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Reference: previous major update at dRICH meeting was last 14 June

Outline

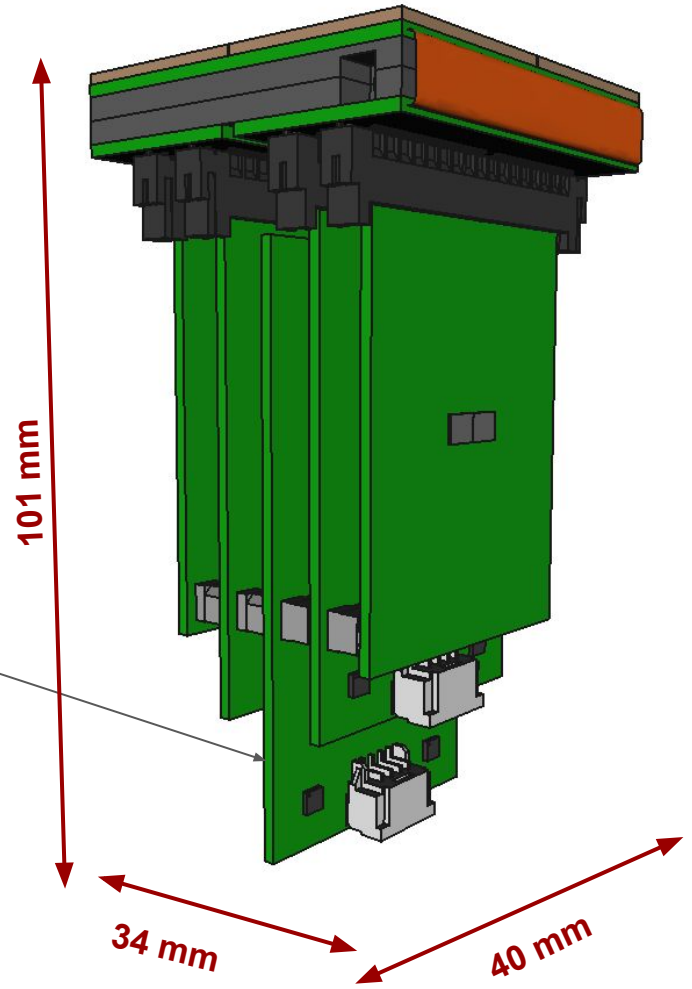
- RDO Overview
- Design elements and miscellanea updates toward RDO baseline/specs
  - Data bus considerations/design ALCOR BUS, SIPM Bus
  - VTRx+ update
  - Inputs from CMS Padova and ePIC DAQ
  - SEU rates + FPGA choice and baseline selections
- Baseline RDO design
- Back-end information
- Rough cost estimates based on baseline options
- Plans

RDO Overview

see previous presentation:
RDO is as a *component* of dRICH PDU

basic RDO specs/numbers:

- provide interface to ePIC DAQ
- provide readout/config to 4 ALCOR64
- route HV to SiPM via FEB
- 1 optical link (TX/RX)
- “control” annealing (MOSFET setup)
- services (T sensors, current monitor, …)
- 4x9 cm^2 surface available



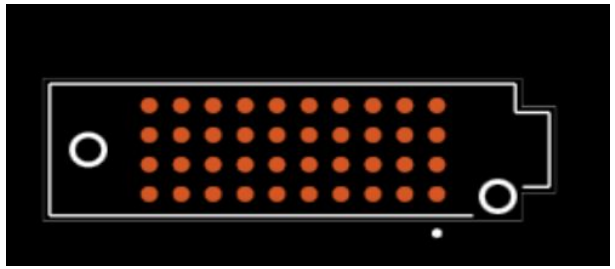
Need of high integration → RDO/FEB/ALCOR teams working together

RDO-FEB communication: ALCOR bus

- for each ALCOR64 (64 channels)
  - 8 DOUT signal (8 lanes per chip)
  - 1 CLKIN
  - 1 CLKOUT
  - 1 TP/SHUTTER
  - 1 RESET
  - 4 SPI

→ 32 differential pairs

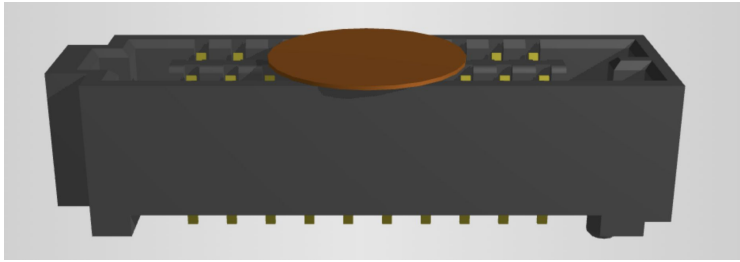
- for each ALCOR Bus Connector (serving 2 ALCOR64)
  - 64 differential pairs → could be reduced (down to 48) adding buffers and sharing SPI but we try this way (64) as baseline
- I/O requirements for FPGA: 128 pins devoted to ALCOR
- can use SAMTEC SEARAY **SEAF-20-06.5-S-04-1-A-K-TR**
  https://www.samtec.com/products/seaf-10-05.0-l-04-1-a-k-tr



Note: fake-FEB/2024 will need to buffer some signals going to ALCOR32

RDO-FEB communication: SIPM bus

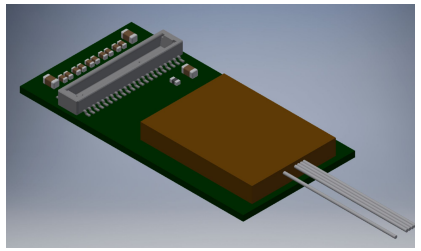
- for each SiPM matrix (64 channels)
  - 8x VBIAS lines → “segmentation by 8”
  - 2x GND lines
  - 2x NTC lines → temperature measurements
  - 8x ANN lines → I/O to drive MOSFET
- for each SiPM Bus Connector (128 channels, 40 lines)
  - 16x VBIAS lines
  - 4x GND lines
  - 4x NTC lines
  - 16x ANN lines → 32 I/O on FPGA or use some I/O expander
- can use SAMTEC SEARAY strip connector
  https://www.samtec.com/products/seaf-10-05.0-l-04-1-a-k-tr

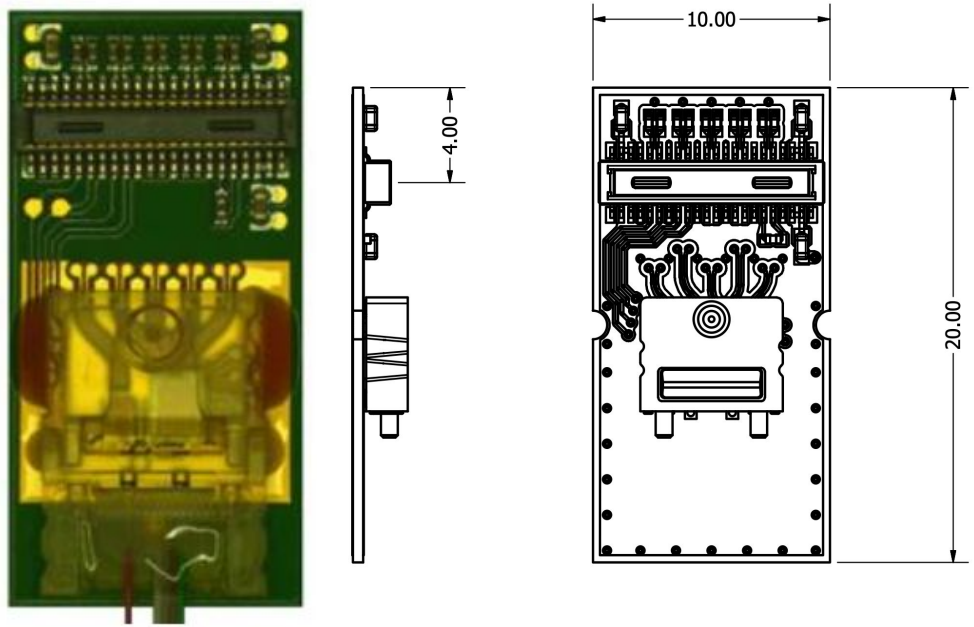


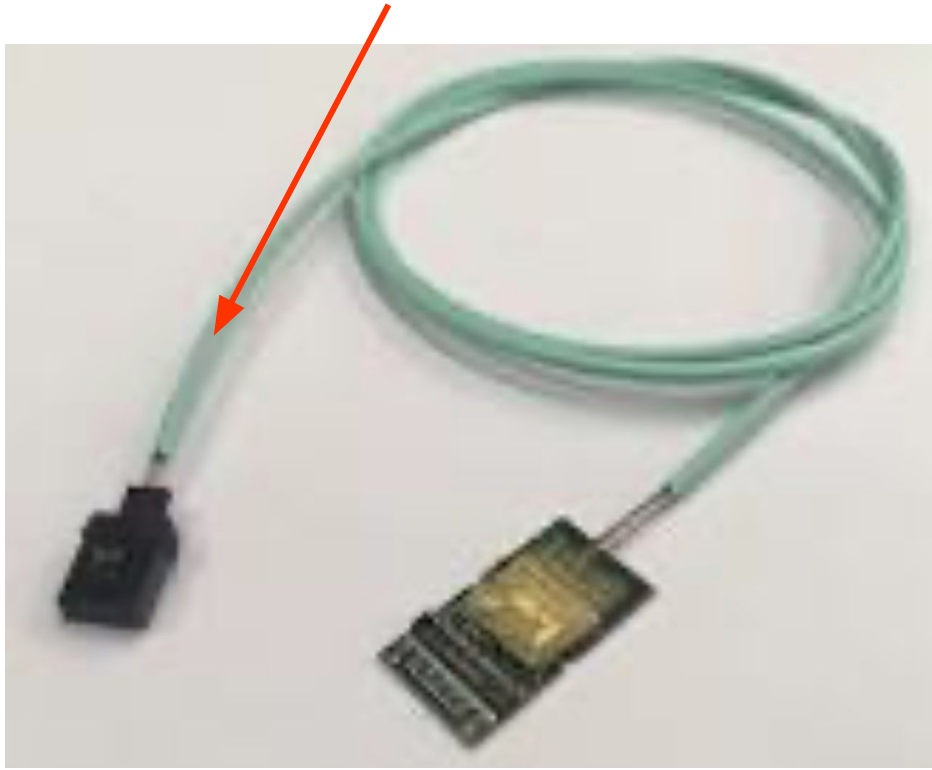
this choice assumes SiPM annealing in forward bias

VTRx+ update

- remember: VTRx+ has a “compact and rad-tolerant” optical transceiver
- bandwidth: 10 Gbps TX, 2.5 Gbps RX
- in ePIC will be used by SVT and dRICH
- requested ePIC/EIC project to prebook 1500 VTRx+ for dRICH
- ordered via CERN/ALICE 20 VTRx+ for 2024/5 pre-production (pigtail 40 cm length with MTP connector)



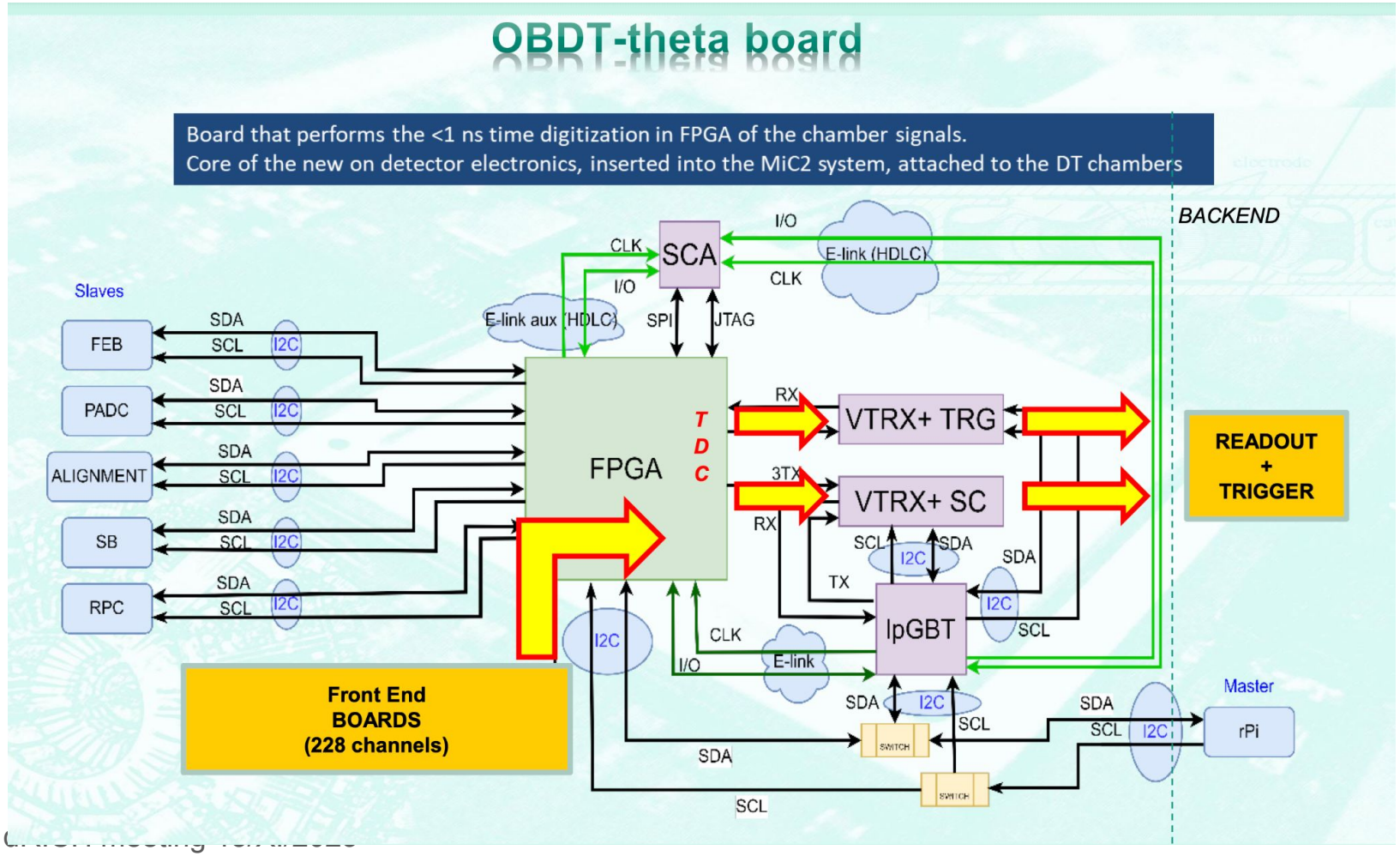




note traditional LHC application is lpGBT + VTRx+

Input from CMS Padova

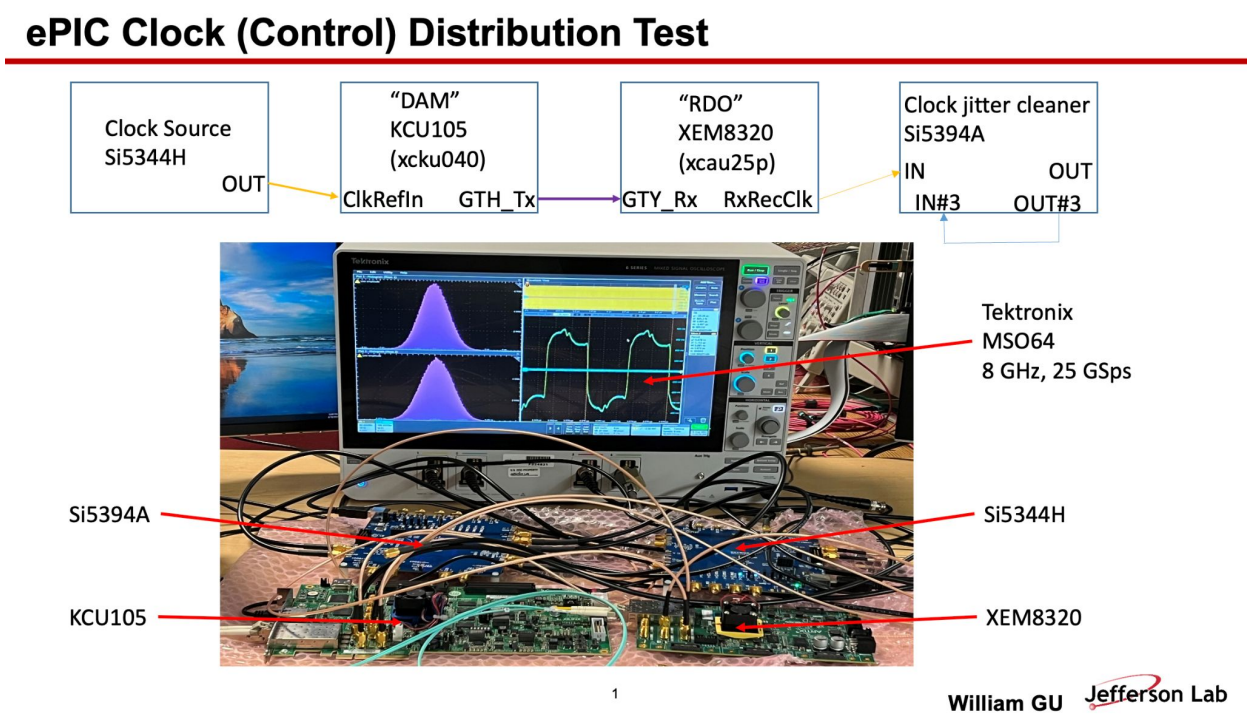
CMS Padova realized for Drift Tube chambers readout a card with a Polarfire FPGA without using lpGBT (to send data)

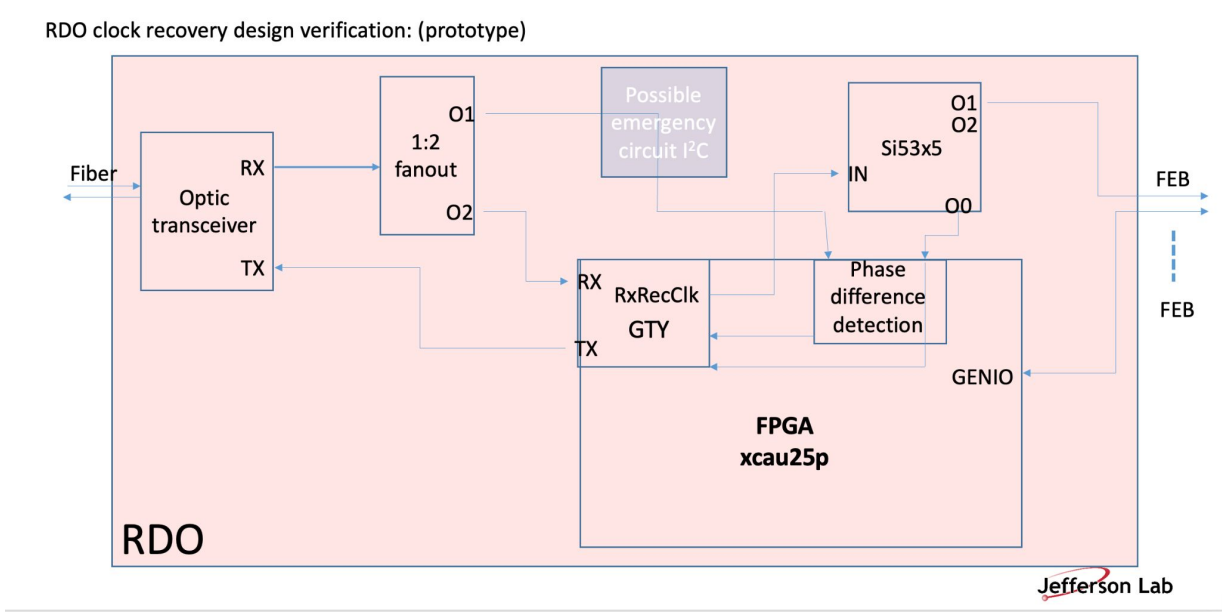


- no problem connecting directly FPGA serializer to VTRX+
- however clock still reconstructed via lpGBT

clock recovery on PolarFire might be challenging

Input from ePIC timing subgroup



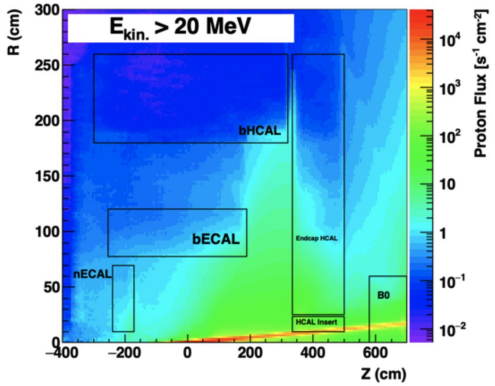


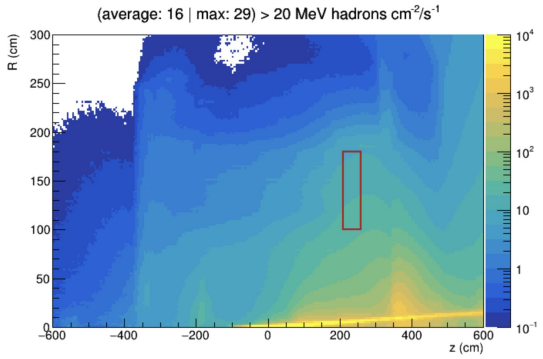
- Context: ePIC timing subgroup is a subset of DAQ&Electronics WG
  - First tests from W. Gu (JLab)
  - J. Schombach (ORNL) testing lpGBT+VTRx+ clock transmissions
  - Next meeting 16 Nov

- ePIC link protocol not yet defined
- default RDO should have ARTIX UltraScale+
- clock multiplier from 98 MHz to 396 MHz to be studied with care

SEU rates + FPGA selection

Xilinx declares 2.67 × 10^{-16} cm^2/bit cross-section for CRAM bits
AUP15 has 42.8 × 10^{+6} configuration bits
dRICH flux (hadrons > 20 MeV): 20 $cm^{-2}s^{-1}$





1 SEU every 4.3x10^6 s/FPGA

↓

1 SEU every 3.5x10^3s/dRICH

↓

1 SEU every hour in whole dRICH

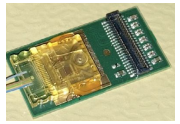
- SEU rate if confirmed seems manageable
- A scrubber might not be strictly needed (no plans in ePIC as far as we know)
- RDO final design to be validated with a full irradiation test

- Artix Ultrascale+ AU15P-SBVB484 (see backup) good compromise between physical size 1.9x1.9 cm^2, resources (5.1 Mb RAM), I/O pins (204)
- Smallest available Polarfire (MPF050T) as rad-tolerant scrubber seems effective choice (see later)

RDO Baseline (I)

Artix SBVB484

VTRx+

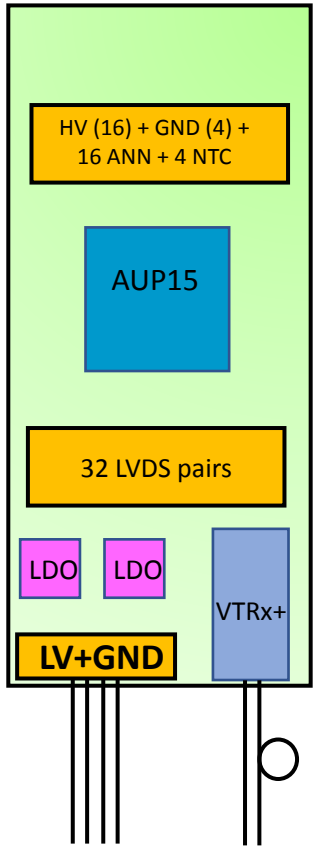


QSPI Flash MT25QU01

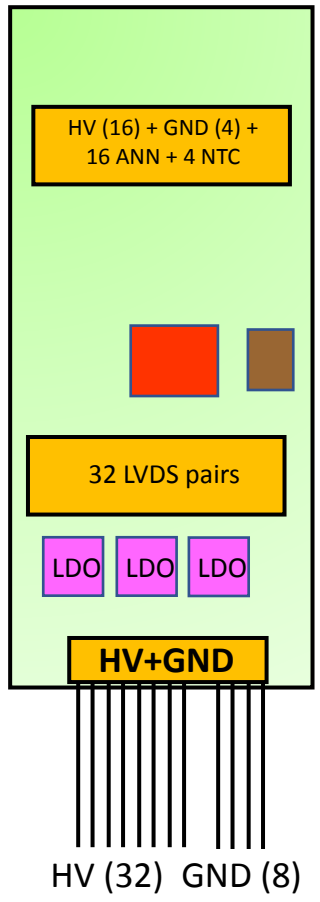
scrubber

Microchip PolarFire MPFO50T-FCS9325

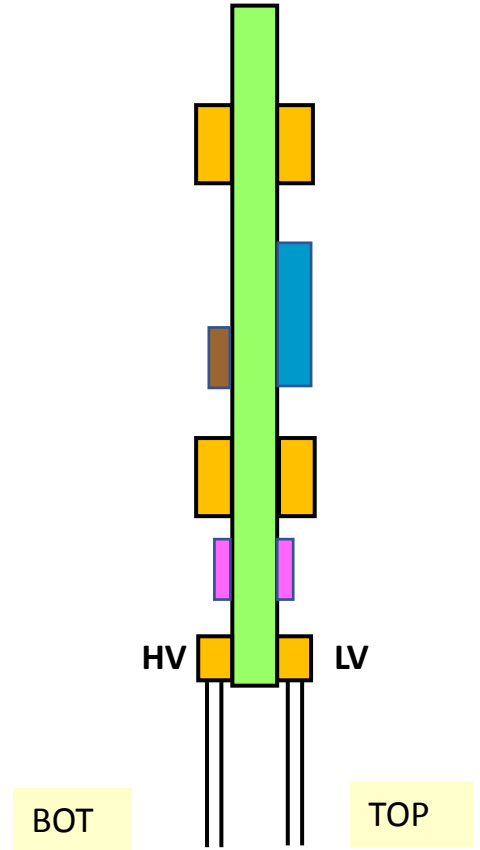
RDO TOP side



RDO BOT side



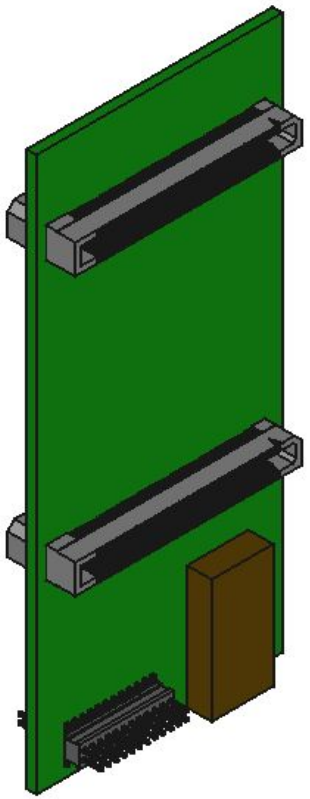
RDO side



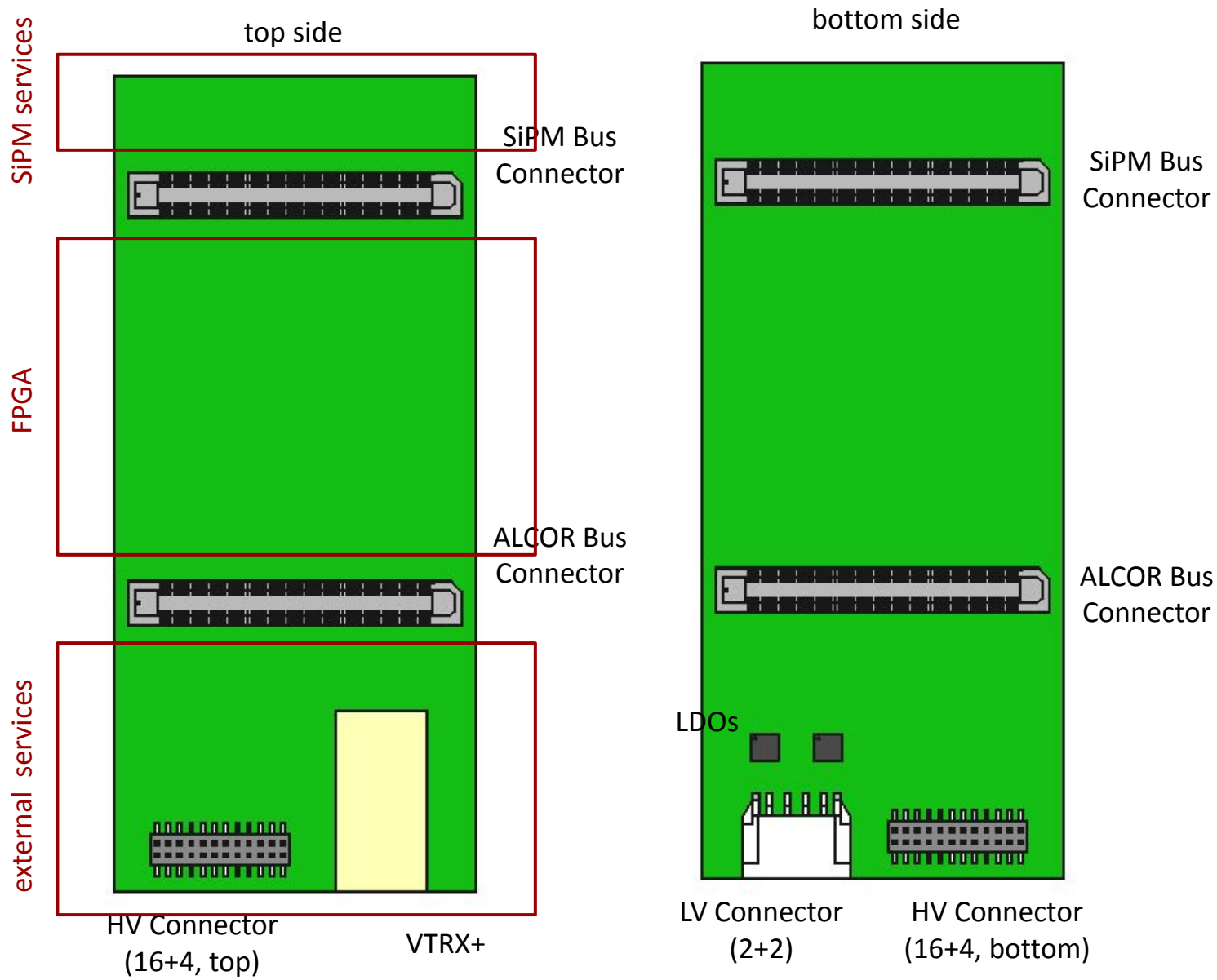
RDO does not distribute LV to the FEBs

components on scale excluding connectors

RDO baseline (II)



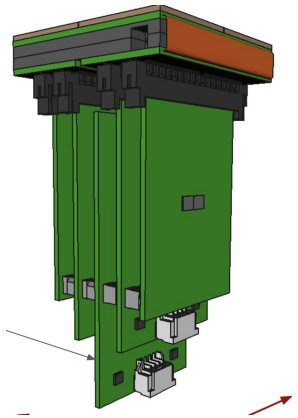
- 14-16 layers min
- HV in shielded middle-layer"!
- the earlier we have a full schematics to begin the layout, the better it is !!



RDO baseline (III): components

Component function	Baseline option	Comments
Main FPGA	Xilinx AU15P-SBVB484	
Scrubber FPGA	Microchip MPF050T-FCS9325	
QSPI Flash	MT25QU01	
VTRX+	CERN	
SIPMbus connector	Samtec Searay 40 pins	
ALCORbus connector	Samtec Searay 128/160 pins	“think about spares”
ADC	MICROCHIP MCP3550-50E/SN	T measurements (V_{MIN}=2.7V). We might use ADC in FPGA or uC
IO expander (I2C)	Microchip MCP23017	likely needed: we save 32 I/O on FPGA
LDO		
Temperature sensors	AD7416AR3	10-bit digital T sensors
Current monitor		
uC as voltage monitor	AT-MEGA16L-8AU	8 10-bit ADCs available
Clock multiplier/clock jitter cleaner	SkyWorks SI53xx	important!

RDO and ePIC DAQ



1248

- PDU: 1248
- RDO: 1248
- FEB: 4992

1248

I-level DAM (27)

- 47 links to PDU
- 1 link to II-level DAM

27

in exp. hall, rack mounted

PC with 4 FELIX each (??)

27

II-level DAM (1)

- 27 links to I-level DAM
- link from central ePIC [clock/trigger]

ePIC interaction tagger
able to reach our DAMS in 10 μs!

1

1

dRICH has largest number of RDOs in ePIC

EPIC Detector Scale and Technology Summary:

Detector System	Channels	RDO	Gb/s (RDO)	Gb/s (Tape)	DAM Boards	Readout Technology	Notes
Si Tracking: 3 vertex layers, 2 sagitta layers, 5 backward disks, 5 forward disks	7 m^2 36B pixels 5,200 MAPS sensors	400	26	26	17	MAPS: Several flavors: curved its-3 sensors for vertex Its-2 staves / w improvements	Fiber count limited by Artix Transceivers
MPGD tracking: Electron Endcap Hadron Endcap Inner Barrel Outer Barrel	16k 16k 30k 140k	8 8 30 72	1	.2	5	uRWELL / SALSA uRWELL / SALSA MicroMegas / SALSA uRWELL / SALSA	64 Channels/Salsa, up to 8 Salsa / FEB&RDO 256 ch/FEB for MM 512 ch/FEB for uRWELL
Forward Calorimeters: LFHCAL HCAL insert* ECAL W/SciFi Barrel Calorimeters: HCAL ECAL SciFi/PB ECAL ASTROPIX Backward Calorimeters: NHCAL ECAL (PWO)	63,280 8k 16,000 7680 5,760 500M pixels 3,256 2852	74 9 64 9 32 230 18 12	502	28	19	SiPM / HG2CROC SiPM / HG2CROC SiPM / Discrete SiPM / HG2CROC SiPM / HG2CROC Astropix SiPM / HG2CROC SiPM / Discrete	Assume HGCROC 56 ch * 16 ASIC/RDO = 896 ch/RDO 32 ch/FEB, 16 FEB/RDO estimate, 8 FEB/RDO conserve. HCAL 1536x5 *HCAL insert not in baseline Assume similar structure to its-2 but with sensors with 250k pixels for RDO calculation. 24 ch/feb, 8 RDO estimate, 23 RDO conservative
Far Forward: B0: 3 MAPS layers 1 or 2 AC-LGAD layer 2 Roman Pots 2 Off Momentum ZDC: Crystal Calorimeter 32 Silicon pad layer 4 silicon pixel layers 2 boxes scintillator	300M pixel 1M 1M (4 x 135k layers x 2 dets) 640k (4 x 80k layers x 2 dets) 400 11,520 160k 72	10 30 64 42 10 10	15	8	8	MAPS AC-LGAG / EICROC AC-LGAD / EICROC AC-LGAD / EICROC APD HGCROC as per ALICE FoCal-E	3x20cmx20cm 600^cm layers (1 or 2 layers) 13 x 26cm layers 9.6 x 22.4cm layers There are alternatives for AC-LGAD using MAPS and low channel count DC-LGAD timing layers
Far Backward: Low Q Tagger 1 Low Q Tagger 2 Low Q Tagger 1+2 Cal 2 x Lumi PS Calorimeter Lumi PS tracker	1.3M pixels 480k pixels 700 1425/75 80M pixels	12 12 1 1 24	150	1	4	Timepix4 Timepix4 (SiPM/HG2CROC) / (PMT/FLASH) Timepix4	
PID-TOF: Barrel Endcap	2.2M 5.6 M	288 212	31	1	17	AC-LGAD / EICROC (strip) AC-LGAD / EICROC (pixel)	bTOF 128 ch/ASIC, 64 ASIC/RDO eTOF 1024 pixel/ASIC, 24-48 ASIC/RDO (41 ave)
PID-Cherenkov: dRICH	317,952	1242	1240	13.5	28	SiPM / ALCOR	Worse case after radiation. Includes 30% timing window. Requires further data volume reduction software trigger
pfRICH	69,632	17	24	12.5	1	HRPPD / EICROC (strip or pixel)	
DIRC	69,632	24	11	6	1	HRPPD / EICROC (strip or pixel)	

work (almost) done communicating dRICH numerology in ePIC

Data throughput modeling (update)

dRICH DAQ parameters	
RDO boards	1248
ALCOR64 x RDO	4
dRICH channels (total)	319488
Number of DAM L1	27
Input link in DAM L1	47
Output links in DAM L1	1
Number of DAM L2	1
Input link to DAM L2	27
Link bandwidth [Gb/s] (assumes VTRX+)	10
Interaction tagger reduction factor	200
Interaction tagger latency [s]	2,00E-06
EIC parameters	
EIC Clock [MHz]	98,522
Orbit efficiency (takes into account gap)	0,92

ALCOR parameters		Notes
Front end limit [kHz]	4000	
ALCOR Clock [MHz]	394,08	It will be 394.08 MHz or 295.55 MHz
Channels/serializer	8	
Bits per hit	64	2 32-bit words per hit (also TOT)
Bits per hit encoding 8/10	80	
Serializer band limit [Mb/s]	788,16	
Theoretical Serializer limit/ channel [kHz]	1231,5	this would be with 0 control words
Serializer limit single ch [kHz]	800	this is expected to improve with ALCOR v3
Number of serializer per chip	8	
Channel/chip	64	
Shutter width (ns)	2	

- numbers passed to ePIC
- interaction tagger critical (**not enough ePIC discussion on it**)
- pressure transferred to budget

	Bandwidth analysis		Limit	Comments
INPUT	Sensor rate per channel [kHz]	300,00	4.000,00	
	Rate post-shutter [kHz]	55,20	800,00	
	Throughput to serializer [Mb/s]	34,50	788,16	
	Throughput from ALCOR64 [Mb/s]	276,00		limit FPGA dependent: with RDO prototype we will have something
	Throughput from RDO [Gb/s]	1,08	10,00	based on VTRX+
	Input at each DAM I [Gbps]	50,67	470,00	
	Buffering capacity at DAM I [MB]	0,01		to be checked but seems manageable
	Throughput from DAM I to DAM II [Gbps]	0,25	10,00	this might be higher (from FELIX to FELIX)
	Output to each DAM II [Gbps]	6,84	270,00	

Aggregated dRICH data		Comments
Total input at DAM I [Gb/s]	1.368,14	This is only "inside" DAM, not to be transferred on PCI
Total input at DAM II [Gb/s]	6,84	This is based on aggregation above + reduction factor of the interaction tagger
Total output from DAM II [Gb/s]	6,84	Further reduction possible to be investigated (FPGA level?)

Preliminary (draft!) cost estimate (RDO+DAQ)

AU15P	250 $
MPF050T-FCSG32SI	125 $
VTRx+	130 $
connectors	30 $
others (LDO, I2C registers, misc.)	50 $
PCB (prod. cost)	400 $

≅1000 $

FELIX2	30 K$
fibers	?

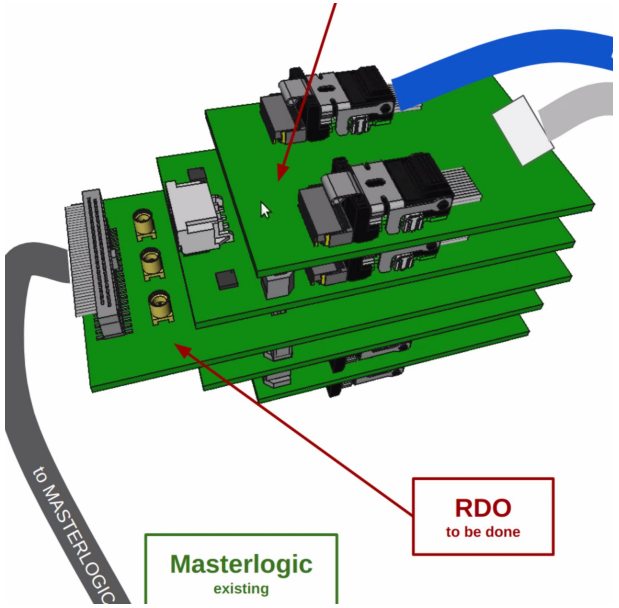
dRICH needs:

- 1500/1600 RDO (incl. 20% spares)
- 28 DAM (not incl. spares)
- 2500 fibers (1248*2)

Aggregated cost: 1.5 M$ (RDO) + 1 M$ (DAQ) → 2.5 M$

Additional notes/plans for 2024

- remember fake-FEB solution to speak with FEB/23
- remember RDO/24 will have ext. connectors for clock and spill
- communication protocol: IPBUS over optical link
- ordered a DELL server with 8 Ethernet/SFP optical link



After RDO schematics is sent for layout:

- work on FW (IPBUS over SFP with KC705)
- prepare for scrubbing (ALICE PD)

→ RDO by June → validate readout for Oct. test beam with RDO

After October 2024 test

- move RDO to ePIC protocol/clock distribution → VC709
  [VC709 is a Virtex evaluation board where miniFELIX FW is available. Can cover protocol developments. It might read out up to 8 PDUs (TBC)]

The big plan (just DAQ)

2024	2025	2026
• **hardware effort** • RDO prototype as close as possible to final • RDO readout of old FEB32 • initial ePIC link test with RDO (clock) • input to TDR • radiation tests	• integration with ALCOR64 in the PDU • **readout with VC709 & ePIC link (including clock)** • RDO rev. 2 final components • possibly test in detector box • (likely radiation tests again….)	• FELIX available in ePIC to groups • use of DAM (FELIX2) • **crucial firmware development L1-DAM / L2-DAM**

2027	2028	2029
production	assembly	assembly in-situ DAM deployment + commissioning

in parallel:

- someone has to build ePIC interaction tagger
- data reduction/calibration through L2-DAM FPGA or SRO to be integrated

Conclusions

- ongoing effort toward specifications/requirements for RDO (at 60/70%)
- secured VTRx+ and defined FPGA baseline
- need of highly integrated development of RDO with other dRICH electronic components (→ BO-FE-TO)
- ePIC link protocol still not defined, we need to remain close to central ePIC DAQ
- at the forefront → designing first ePIC RDO (risk of later specs/surprises)
- ePIC interaction tagger is crucial to dRICH architecture → need to work with ePIC/EIC project

Backup

Xilinx selection

	AU7P	AU10P	AU15P	AU20P	AU25P
System Logic Cells	81,900	96,250	170,100	238,437	308,437
CLB Flip-Flops	74,880	88,000	155,520	218,000	282,000
CLB LUTs	37,440	44,000	77,760	109,000	141,000
Max. Distributed RAM (Mb)	1.1	1.0	2.5	3.2	4.7
Block RAM Blocks	108	100	144	200	300
Block RAM (Mb)	3.8	3.5	5.1	7.0	10.5
UltraRAM Blocks	–	–	–	–	–
UltraRAM (Mb)	–	–	–	–	–
CMTs (1 MMCM and 2 PLLs)	2	3	3	3	4
Max. HP I/O(1)	104	156	156	156	208
Max. HD I/O(2)	144	72	72	72	96
DSP Slices	216	400	576	900	1,200
System Monitor	1	1	1	1	1
GTH Transceiver(3)	4	12	12	–	–

Package (1)(2)(3)	Package Dimensions (mm)	AU7P	AU10P	AU15P	AU20P	AU25P
		HD I/O, HP I/O, GTH, GTY				
UBVA292	10.5x8.5	72, 58, 4, 0				
UBVA368	11.5x9.5		24, 104, 8, 0	24, 104, 8, 0		
SBVB484	19x19		48, 156, 12, 0	48, 156, 12, 0		
SBVC484	19x19	144, 104, 4, 0				
SFVB784	23x23				72, 156, 0, 12	96, 208, 0, 12
FFVB676	27x27		72, 156, 12, 0	72, 156, 12, 0	72, 156, 0, 12	72, 208, 0, 12

256-channels RDO, 2+2 ALCOR-64 mezzanines