FY24 eRD109 “Clock Distribution”

FY24 – Proposals, DAC reviewed 28-31 August 2023:

Also known as “RDO Prototype”

	Detector/Technology	Discrete/ASIC	Group
A	Calorimeter	Discrete	IUCF
B	Calorimeter	HGCROC	ORNL
C	dRICH	ALCOR	INFN – BO, TO
D	AC-LGAD	EICROC	Omega/IN2P3/IJCLab/CEA/IRFU
		FCFD	FNAL
		Barrel L-M Serv. Hybrid	ORNL
		High Precision Clock Distribution	BNL/Rice/UIC
E	MPGD/µRWell	SALSA	CEA
			USP

Under consideration. Exact work division will likely be slightly modified ⇒

Inst.	Resource	FTE (%)	Budget (k$)
	TOF readout electronics R&D		
BNL	Electrical Engineering	40	120
BNL	Development Kit	-	10
BNL	Travel	-	4
BNL	Other component	-	3
Rice	Electrical Engineering	30	45
Rice	Travel	-	2
Rice	Other component	-	2
UIC	Electrical Engineering	30	30
UIC	Travel	-	2
UIC	Other component	-	2
Total			**220**

What

- Design and manufacture an “RDO Prototype” (“Service Hybrid”) based upon
  - Artix FPGA, 10 Gbs SFP+ fiber, include VTRX+?, clock-cleaner PLLs, bPOL12V CERN power scheme, etc
  - firmware & support software with streaming scheme in mind
- Connect to
  - EICROC0 prototype board (via FMC connector)
  - future EICROC1 prototype (via FMC connector) ⇐ main target, but end of FY24?
  - ETROC (for testing of board features with a realistic but existing and similar ROC used for TOF in CMS) via CMS ETL-type connectors.
  - ORNL-developed (also under eRD109) FLEX PCB. Under discussion.
  - other ePIC ASICs? TBD
- Produce ~5 boards
  - with associated power distribution sister boards. TBD.

Milestones (what we want to learn)

1. Low-jitter (5 ps) EIC (98.5 MHz) clock extraction & distribution
   a. together with clock distribution to the many ROCs (~60 or so)
2. Develop a simple (basic for now) streaming scheme for data and timing
   a. word sizes, frame sizes, basic commands, basic frame headers
3. Gain Xilinx Artix FPGA experience
   a. robust poweron/startup & configuration
   b. use of high-speed serial (fiber) primitives (“GTP”)
   c. clocking schemes of the FPGA
4. Test ROC readout capabilities
   a. e.g. number of pins required, ROC data deserialization, feeding the ROC data to the fiber, internal FPGA resources needed, etc
   b. specific target is EICROC1 but perhaps we can use some other available (but similar) ROC immediately, while we wait: ALTIROC, ETROC, other??
5. Gain experience with CERN LV ASICs
   a. with power measurement
6. Radiation issues: SEU remediation schemes, irradiation tests at facilities
   a. basic for now, more involved later (FY25)?
7. Create shared firmware blocks for all of ePIC DAQ RDOs
   a. fiber interfaces (down- & up-stream), I2C, 1wire, PROM R/W, temperature/id, others
   b. develop a robust and intuitive code sharing scheme that can be used by all collaborators (shared disks? Git?)
      i. in concert with the ePIC Software & DAQ Group

⇒ Exact milestones (with schedule) for each institution under consideration → will be submitted to eRD109 soon