OAK RIDGE National Laboratory

H2GCROC3A testing

Norbert Novitzky
(ORNL)
Miklos Czeller, Gabor Nagy
(Debrecen)
Nov 1st, 2023

H2GCROC3A architecture

Overall chip divided in two symmetrical parts:

- One half is made of:
  - 39 channels (in CMS 36 channels, 1 Calib, 2 CMN)
  - Bandgap, voltage reference close to the edge
  - Bias, ADC reference, Master TDC in the middle
  - Main digital block and 3 differential outputs (2 trigger, 1 data)

Measurements:

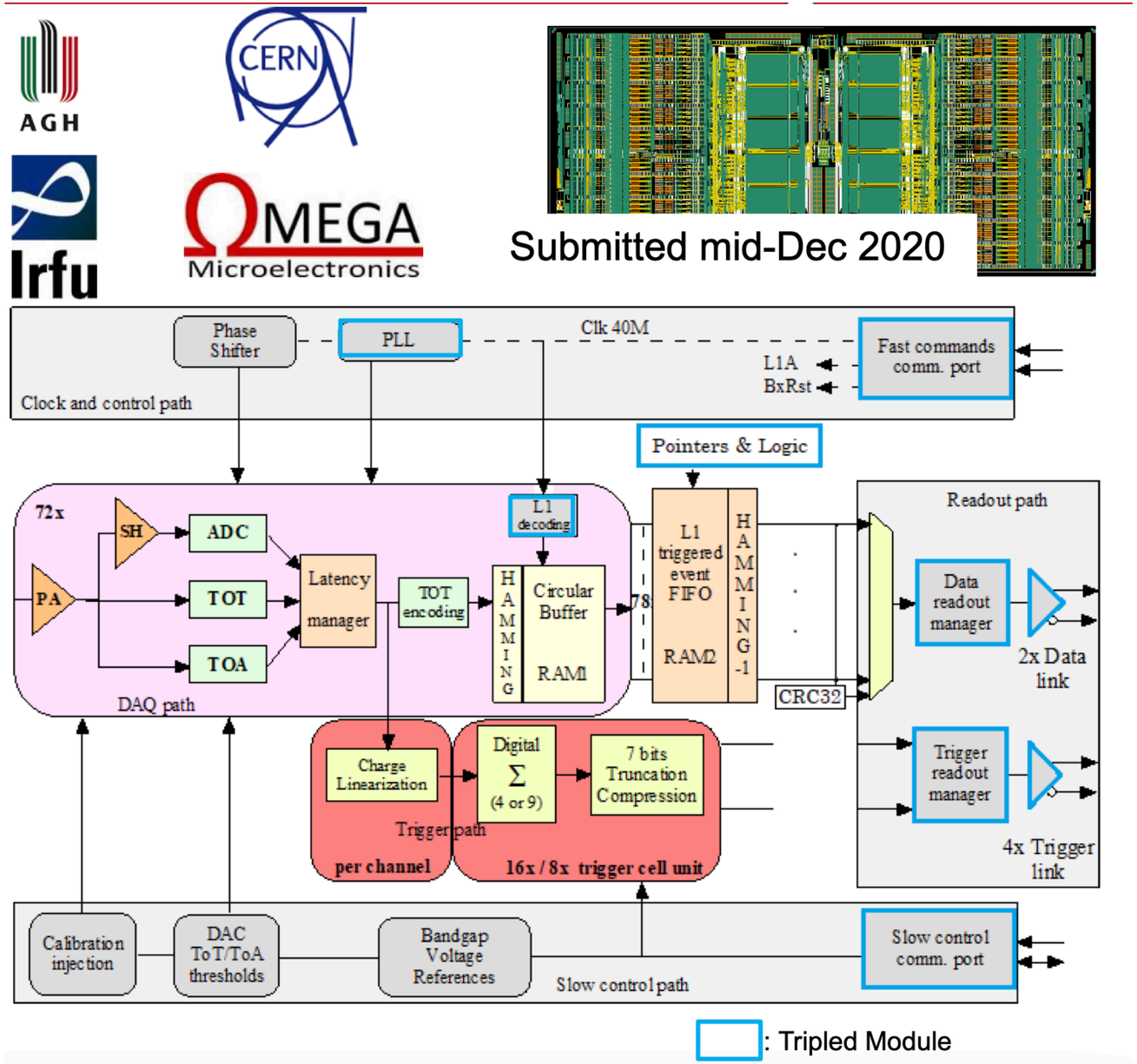
- Charge:
  - ADC peak measurement, 10 bits at 40 MHz, different gain setups possible, 0.4fC resolution
  - TDC: (Time over Threshold), 12 bits, 2.5fC resolution
- Time:
  - Time of arrival, 10 bits (25ps)

Data flow:

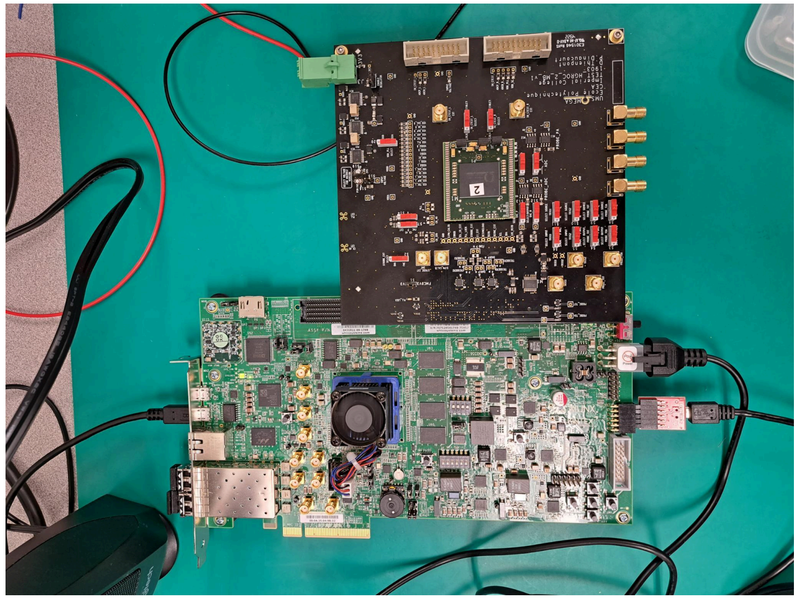
- DAQ path:
  - 512 dept RAM1, circular buffer
  - Secondary RAM2, 32 dept
  - Store all channel data, ADC, TOA, TOT
  - Output 2x 1.28 Gbps links
- Trigger path:
  - Sum of 4 or 9 channels, linearization, compression to 7bits
  - 4 x 1.28 Gbps links

Control:

- Fast commands, 40MHz and 320MHz clock
- I2C for slow control

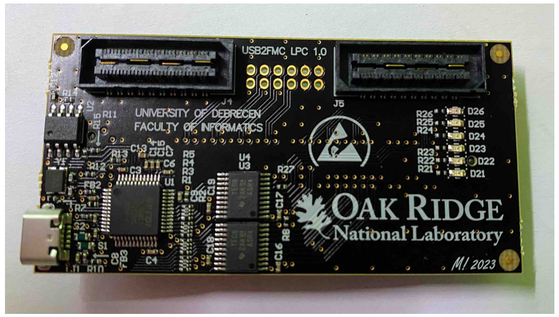


What do we have? What we produced so far



First mezzanine + carrier board designed by Omega:

- Received the chip and produced couple of mezzanines and carrier boards for testing
- Understanding the communication, setup of the chip
- We can physically solder inputs (SiPM) on channels, but this is more for single-channel testing



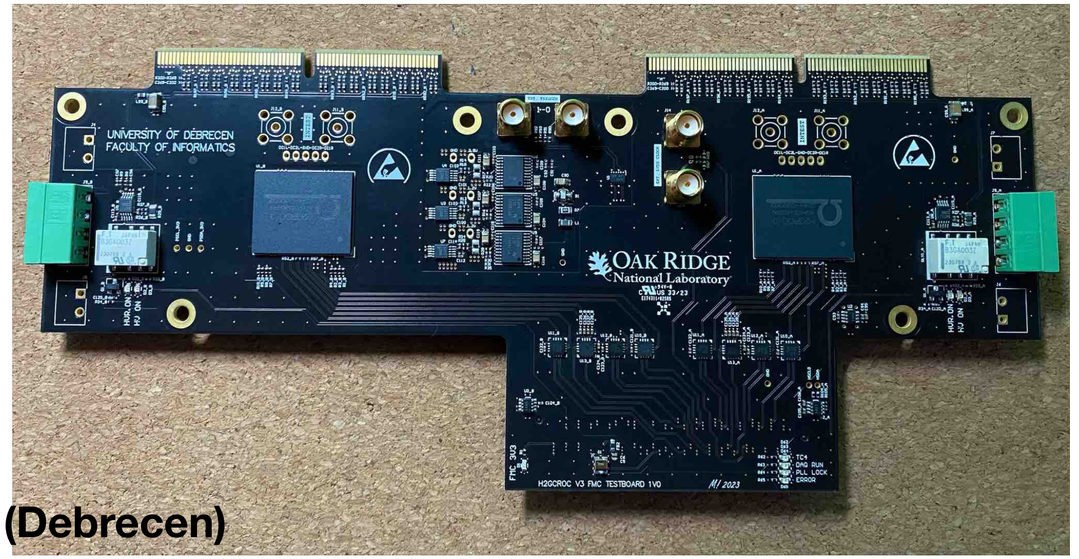
ComBoard1.0:

- USB3 readout communication
- Testing the Samtec Cables (connectors attached)

ProtoBoard1.0:

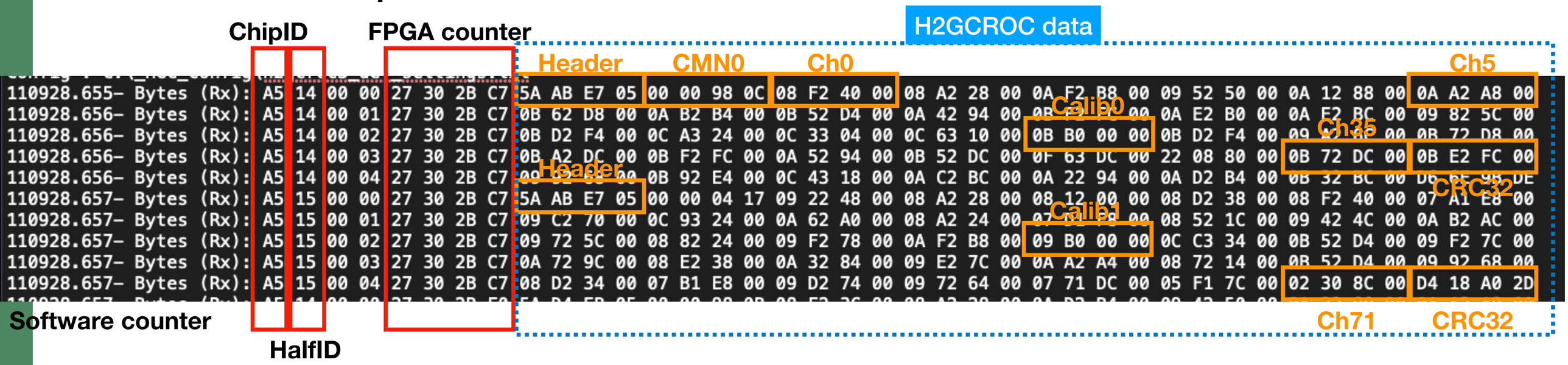
- Produced 2 of these boards so far with H2GCROC3A
- Made so it is compatible with the CAEN commercial readout
  - The upper golden pins can accept the CAEN backboards (2x)
- 64x2 = 128 channel readout - not every of the 72 channel is connected
- LVDS readout via the FMC connector
- Compatible with the KCU105 (firmware, software done):
  - Still work-in-progress, there are improvements coming as we speak

ProtoBoard1.0



Thanks a lot to Miklos Czeller and Gabor Nagy (Debrecen)

Data format explained



Ch0 `08 F2 40 00`

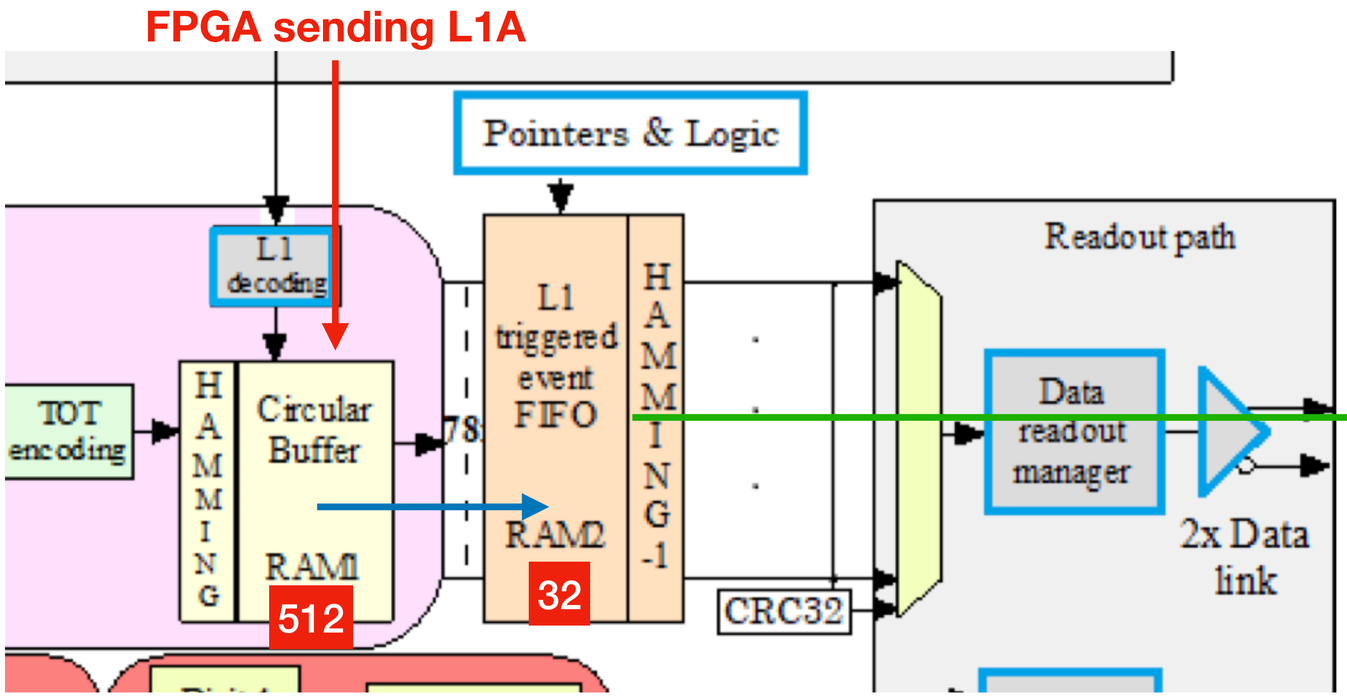
0 0 0010001111 0010010000 0000000000

Tc Tp ADC(BX-1) ADC(BX) TOA(BX)

Different data format with different charge inputs:

Tc	Tp	10-bit	10-bit	10-bit	Explanation
0	0	ADC(BX-1)	ADC(BX)	TOA(BX)	TOA and TOT threshold is not reached
0	1	ADC(BX-1)	ADC(BX)	TOA(BX)	TOA threshold reached, TOT not
1	0	ADC(BX-1)	TOT(BX)	TOA(BX)	TOT threshold reached
1	1	ADC(BX)	TOT(BX)	TOA(BX)	Characterization

One known problem quickly discovered – this is only H2GCROC3A



How we see it working:

1. **FPGA sends an L1A trigger signal**
2. **RAM1->RAM2 moving data**
3. **RAM2 trickles down the data as they come in**

Problem arrises in step 2:

- **When RAM1—>RAM2 move is done, the power can decrease**
- **If the next L1A comes quickly, then it might flip 1—>0 bit**
- **Depends on the frequency of the L1A coming in**

Problem fix:

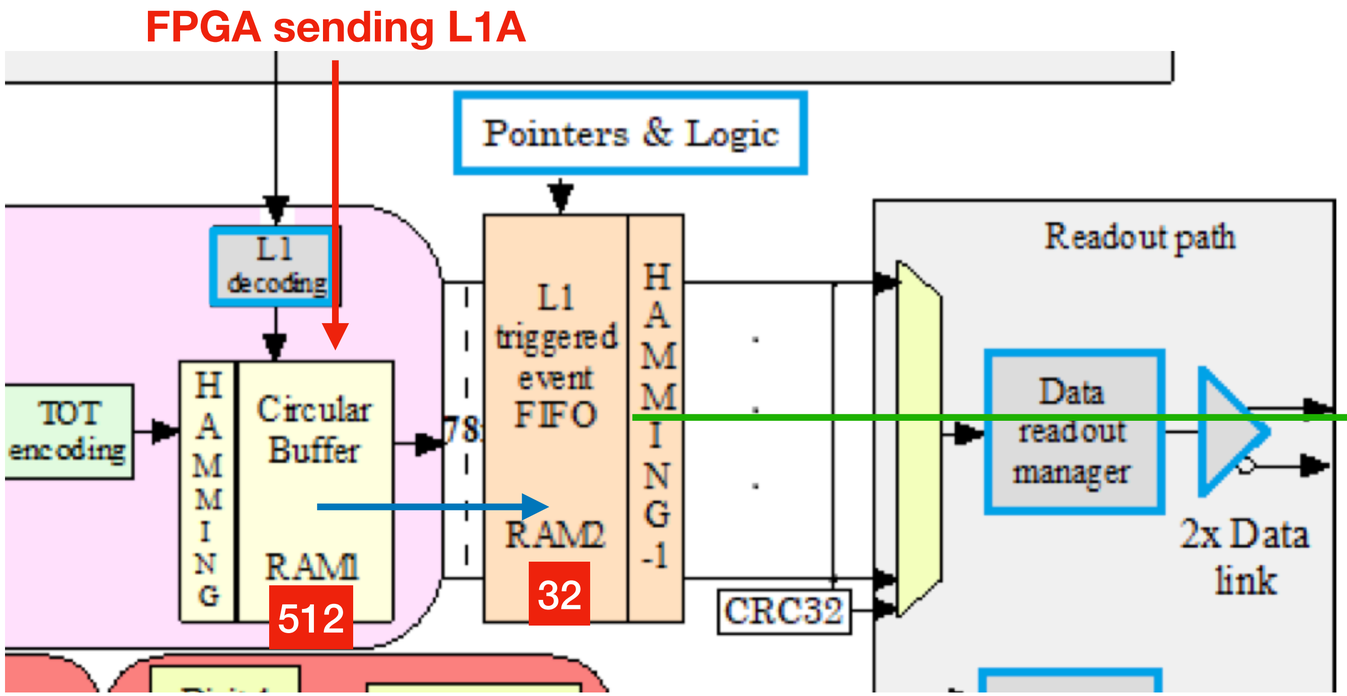
- Connect the VH10 pin to the 1.2 V
- This prevents the drop of power and corruption of the data
- Hamming code has to be ==0 in order to see no corruption

This problem is annoying, we fix it with implementation of dead time. We found 1 μs is sufficient for see no significant Hamming code errors

We connected the 1.2V and will retest

This bug is fixed in the H2GCROC3B - available in early November

One known problem quickly discovered – this is only H2GCROC3A



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3. RA

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- If the 1—>
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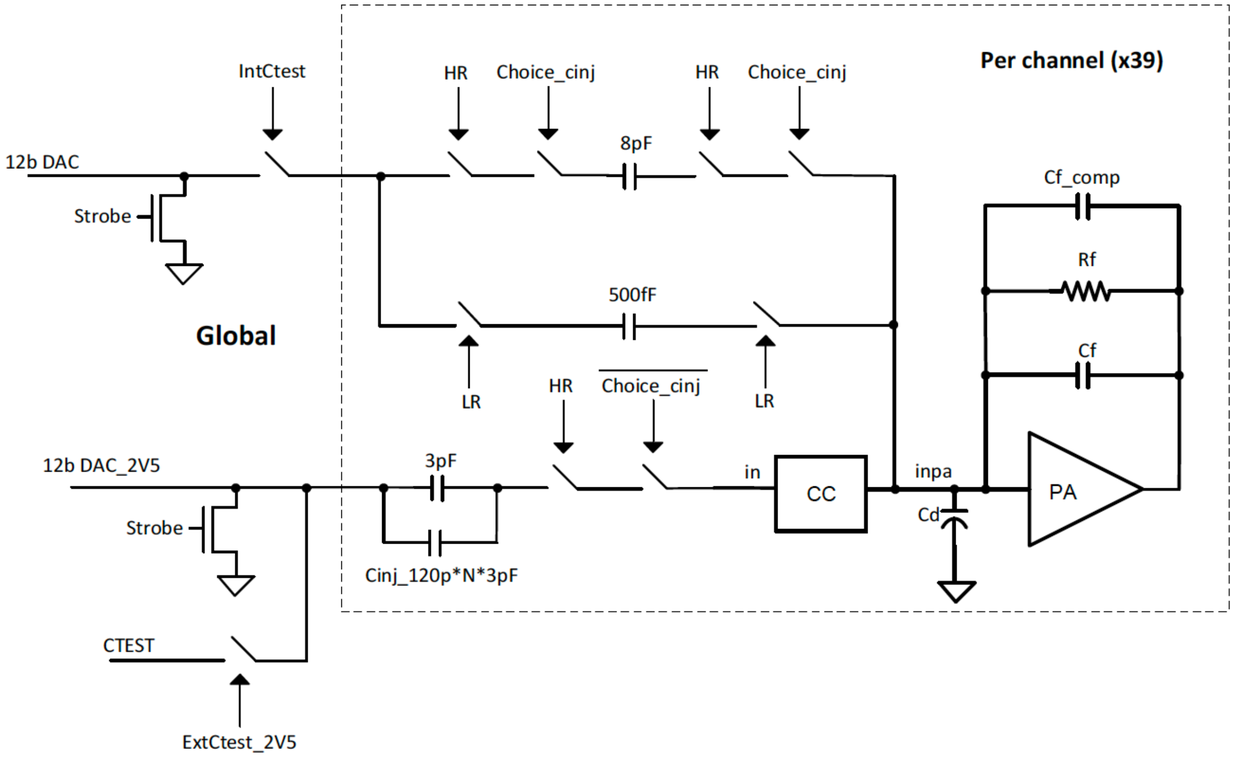
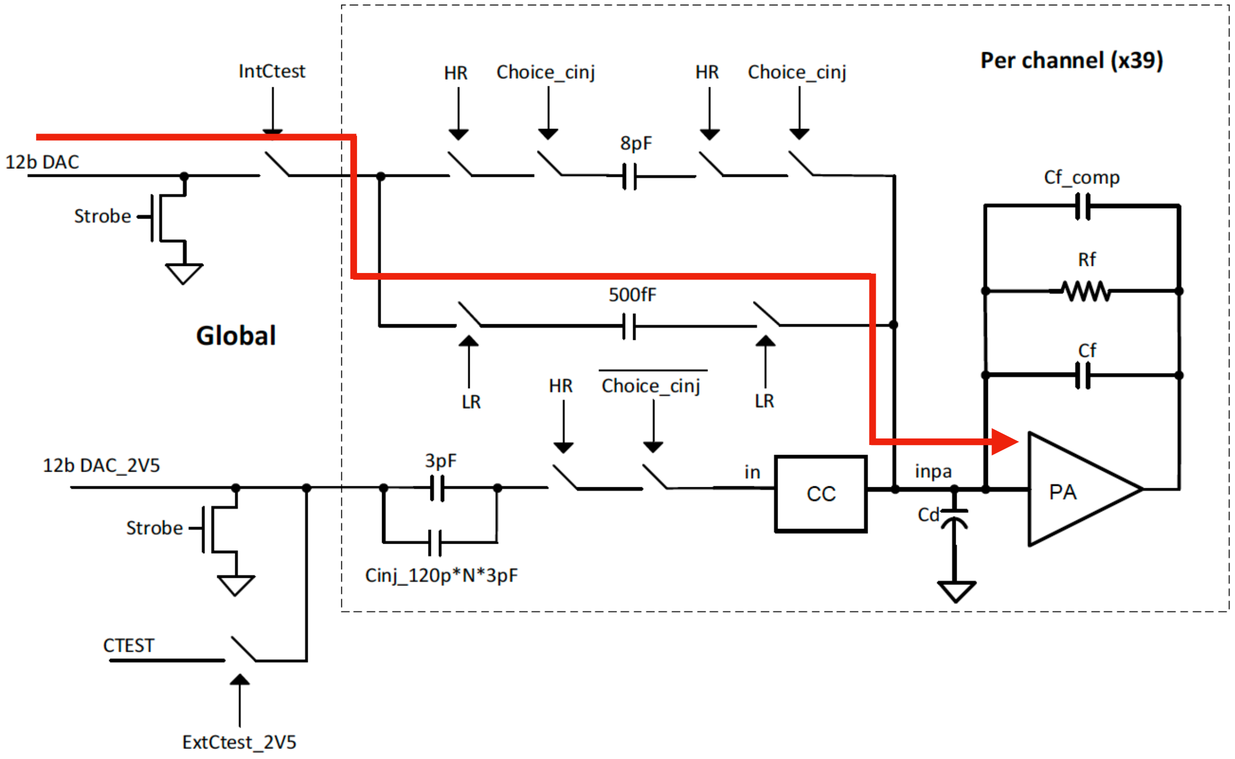
Internal injection circuit (Slow control)



Three different internal injection path:
(There is no need to connect any channels, all is inside the chip):
All of them have a 12-bit range as input value, can be setup via I2C

Internal injection circuit (Slow control)



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Low injection path:

- Goes through the 500fF capacitor, directly to the pre-amp
- Circumvents the current conveyor
- Testing mostly the ADC range in small steps
- TOA threshold setup

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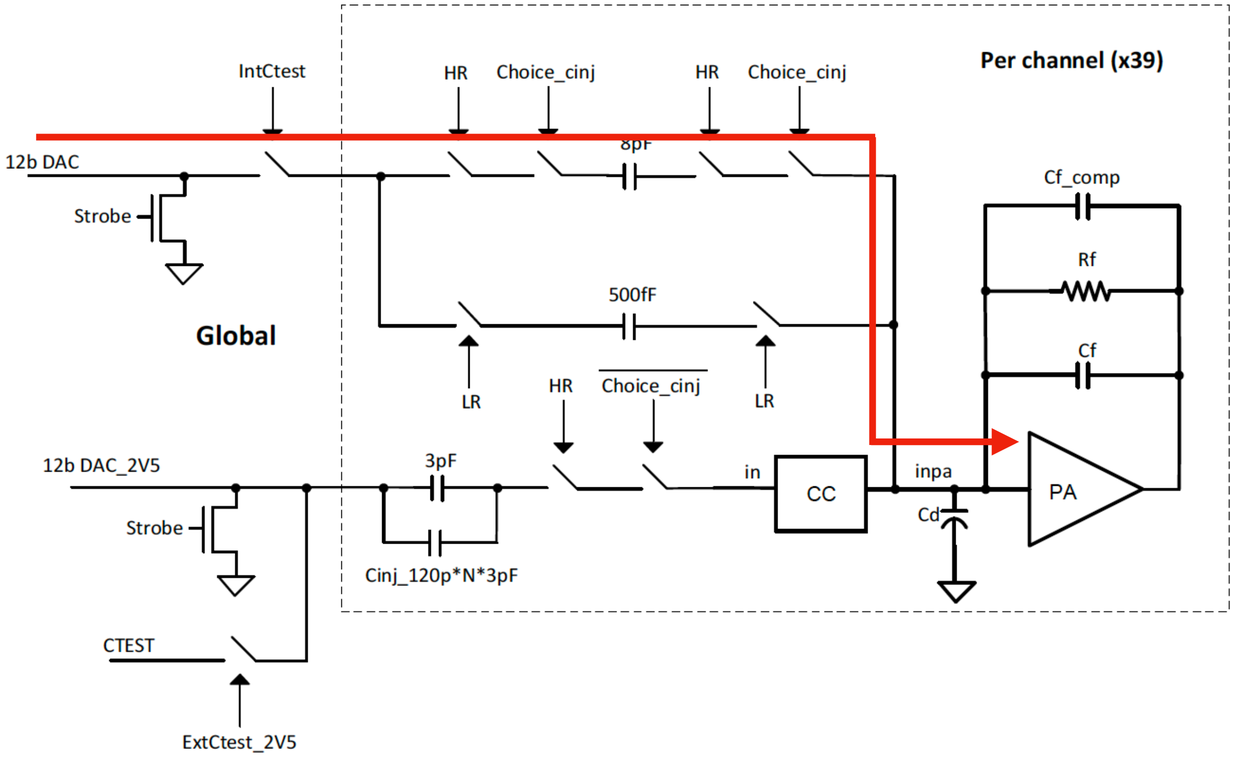
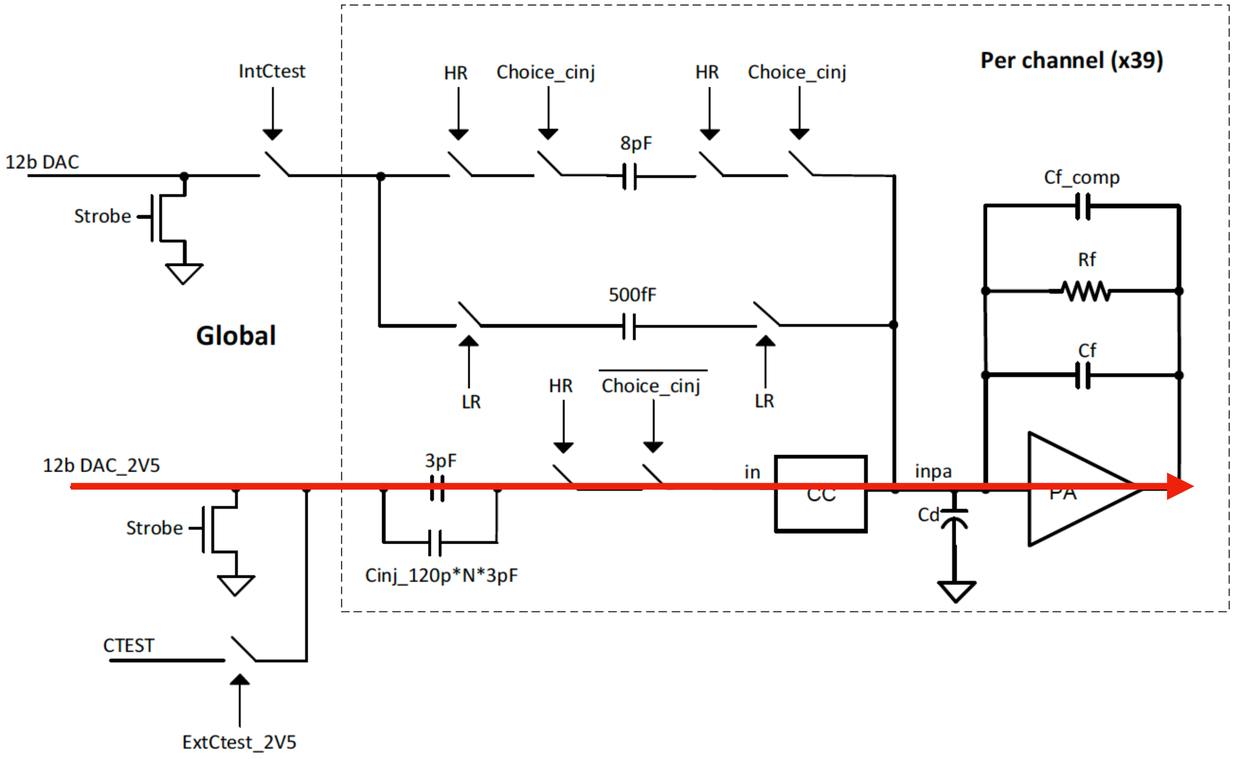


Three different internal injection path:
(There is no need to connect any channels, all is inside the chip):
All of them have a 12-bit range as input value, can be setup via I2C

High injection path:

- Goes through the 8pF capacitor, directly to the pre-amp
- Circumvents the current conveyor
- Testing mostly the TOT threshold
- Linearity on entire dynamic range

Internal injection circuit (Slow control)



Three different internal injection path:
(There is no need to connect any channels, all is inside the chip):
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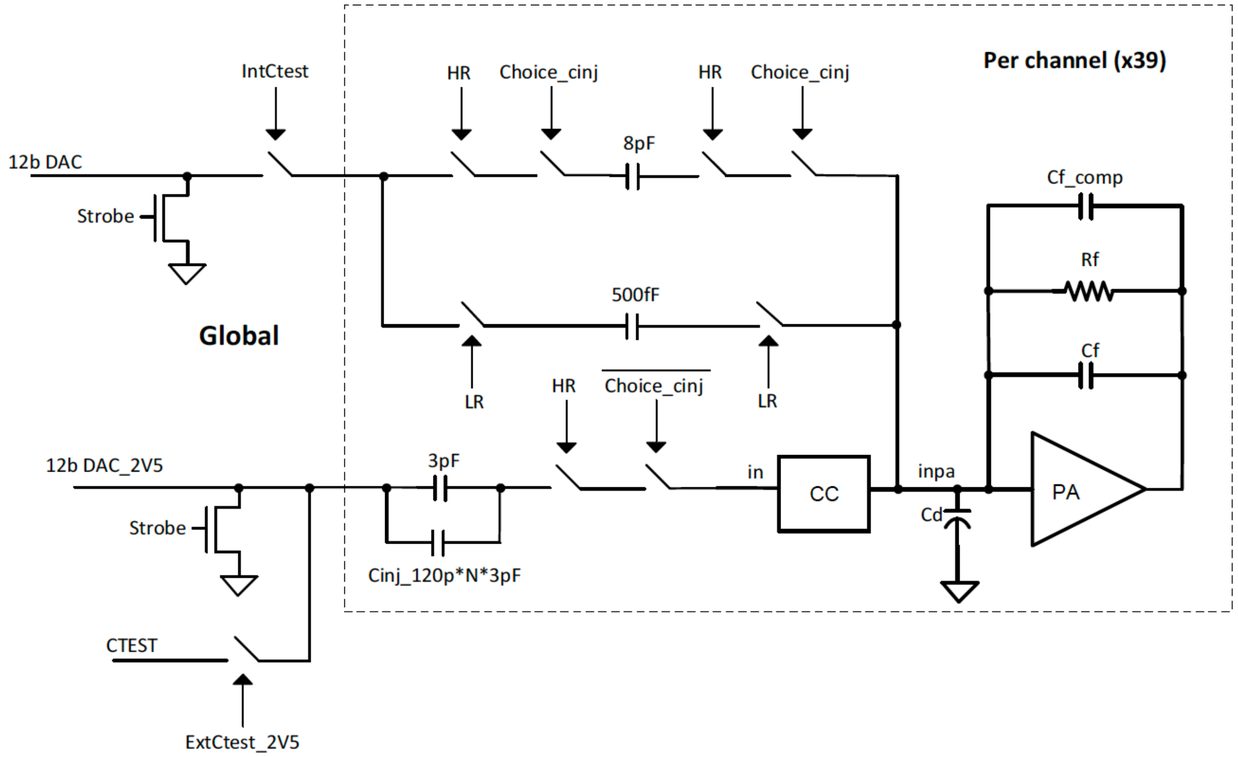
2V5 injection

- Same as an external signal (mimics the SiPM input)
- Setup the current conveyor attenuation of the signal

Internal injection circuit (Slow control)



The following tables show how to select the different configurations for internal/external calibration:

	DAC LR	DAC HR	CINJ 3pF	CINJ 3pF*N	CTEST 3pF	CTEST 3pF*N
HighRange	0	1	1	1	0	0
LowRange	1	0	0	0	0	0
Choice_cinj	X	1	0	0	0	0
Cinj_120p	0	0	0	1	0	1
IntCtest	1	1	0	0	0	0
ExtCtest_2V5	0	0	0	0	1	1
Calib INPA	0 - 500fC	0 - 8pC	-	-	-	-
Calib IN	-	-	0 – 3pC	0 – 3pC*N	-	-
Calib Ext Inj	-	-	-	-	CTEST * (0 – 3pC)	CTEST * (0 – 3pC*N)

This is the map of I2C registers to set each injection path

Three different internal injection path:
(There is no need to connect any channels, all is inside the chip):
All of them have a 12-bit range as input value, can be setup via I2C

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2V5 injection
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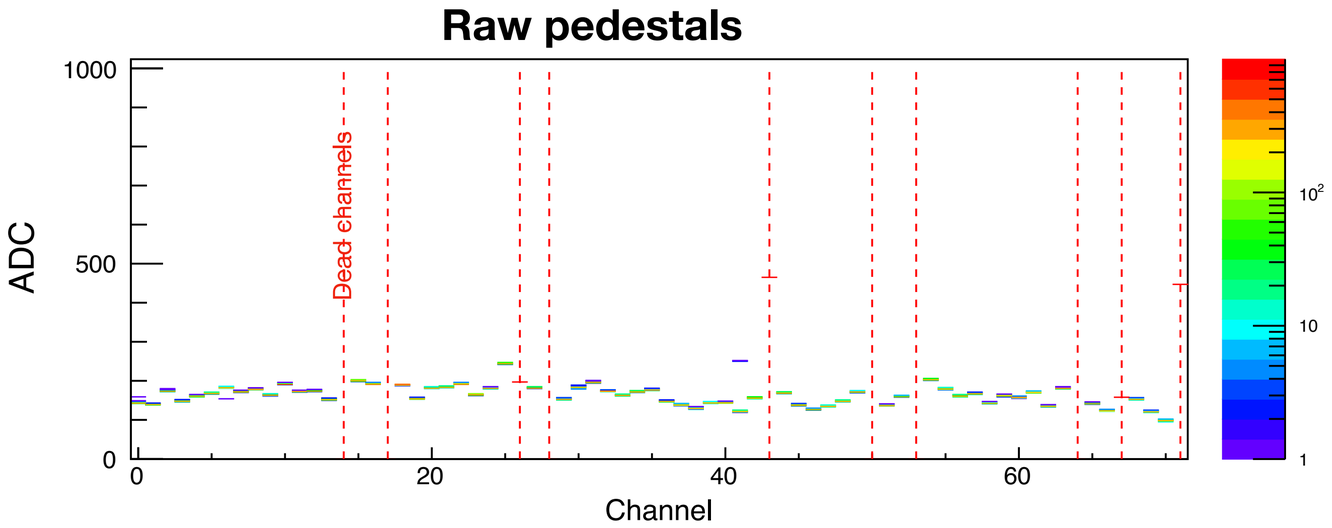
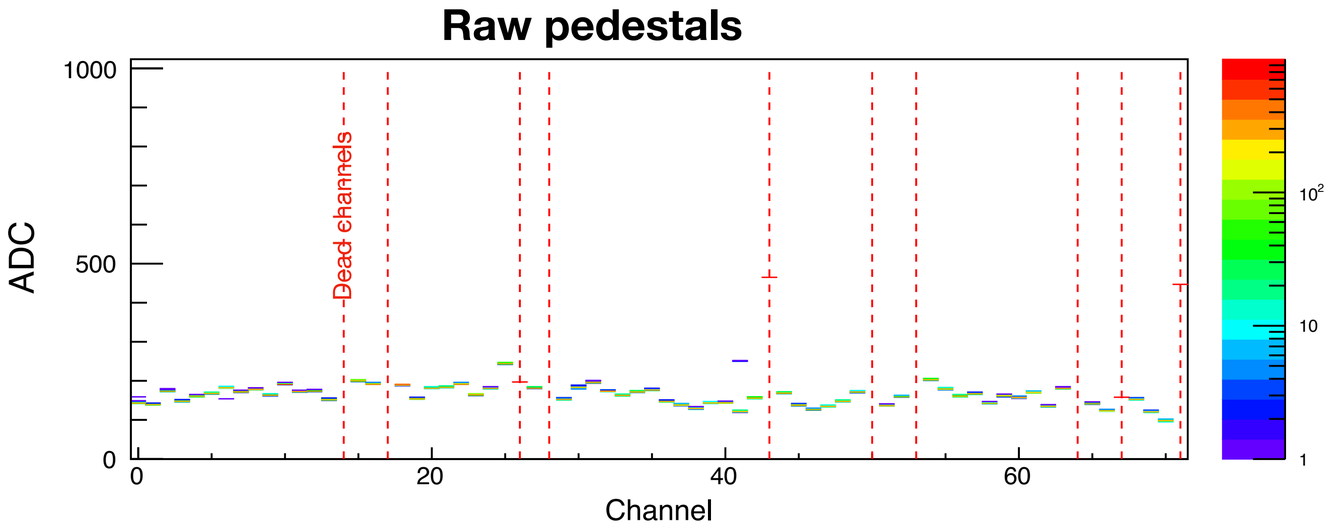
First test, pedestals calibration (Slow control)



Pedestals as we turn-on the chip:

- This is a CMS leftover chip, so it had 10 dead channels
- This is also a H2GCROC3A chip

First test, pedestals calibration (SC)



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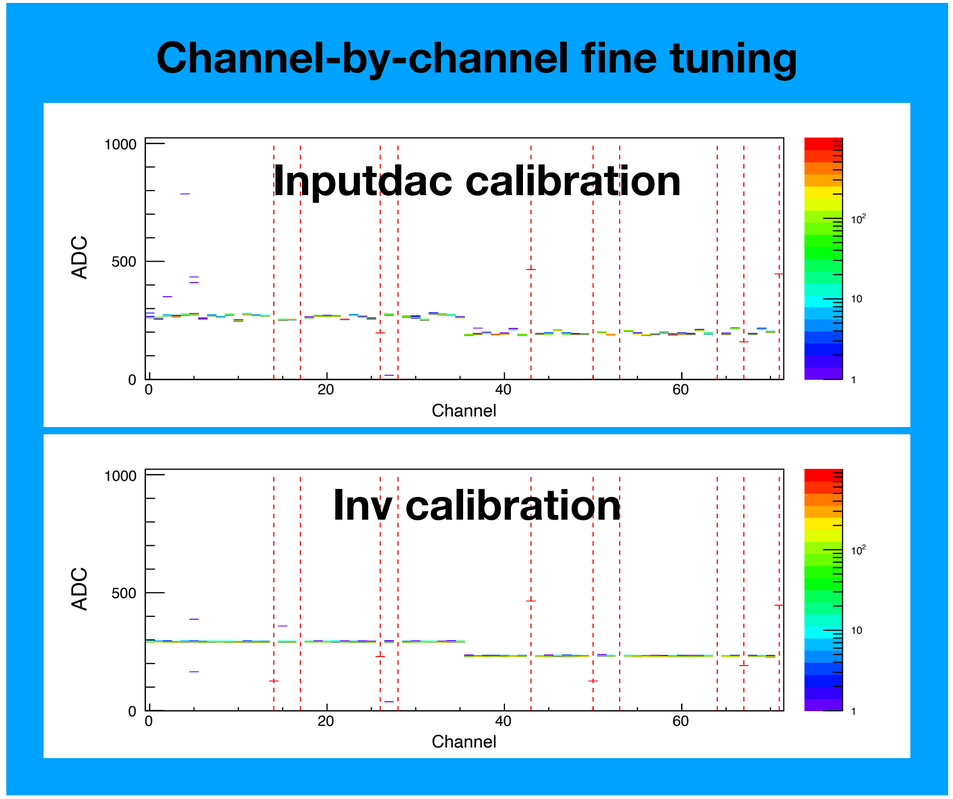
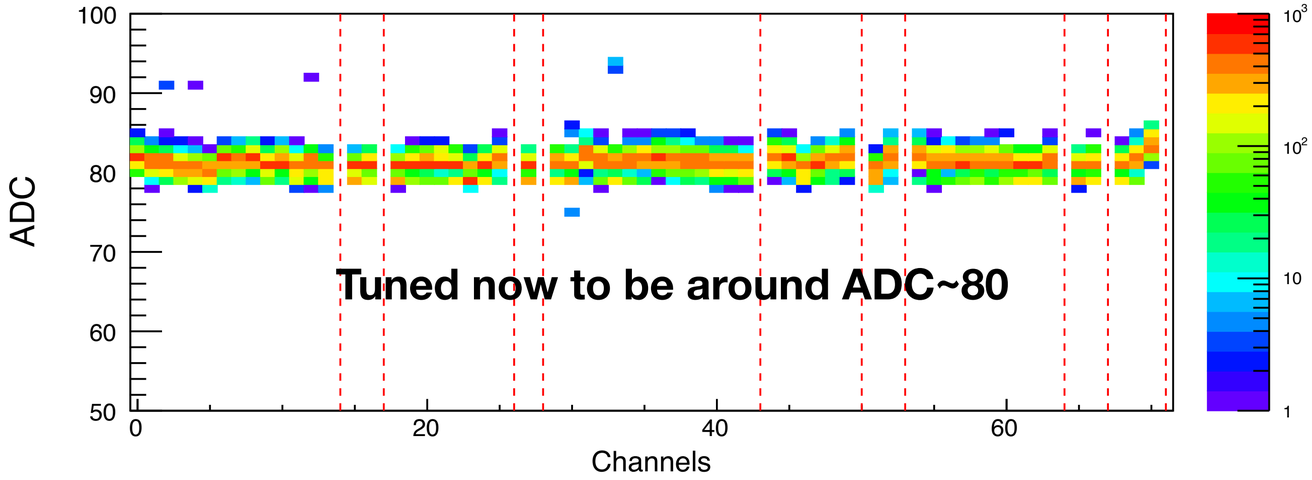
- This is a CMS leftover chip, so it had 10 dead channels
- This is also a H2GCROC3A chip

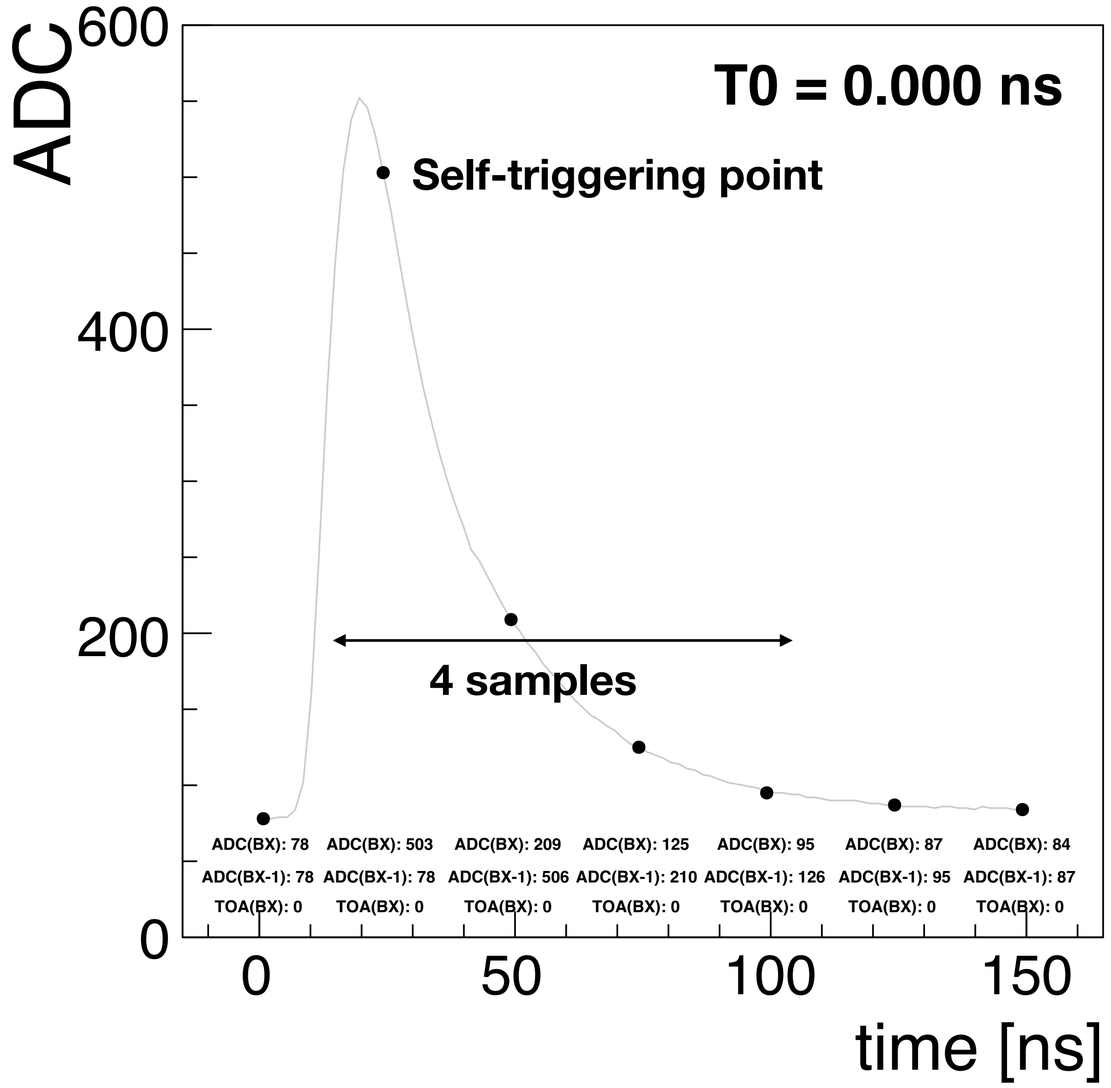
Pedestals after calibration:

- Channel-by-channel calibration is done:
  - Register_0 inputdac
  - Register_3 trim_inv
- We can set the global pedestals by half-chip:
  - Register_4 Inv_vref
  - Register_5 Noinv_vref





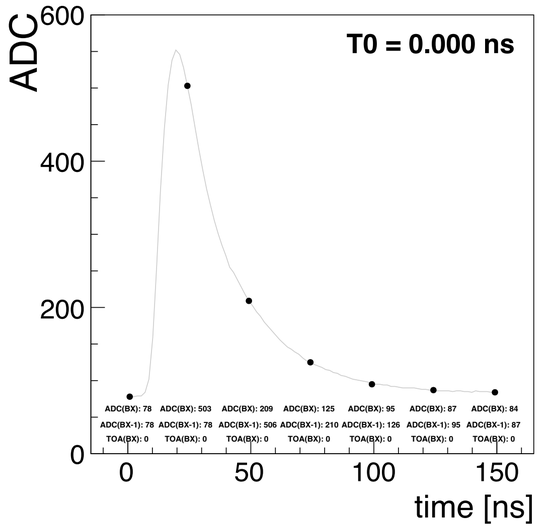
How it would look in ePIC (Sampling Readout)

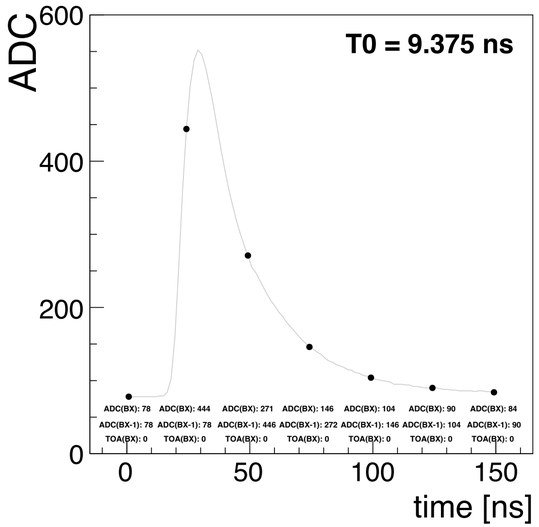


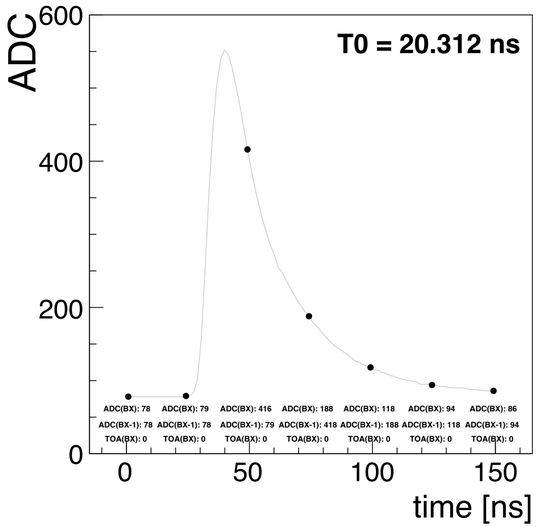
What we will see in the signal with the 25ns sampling:

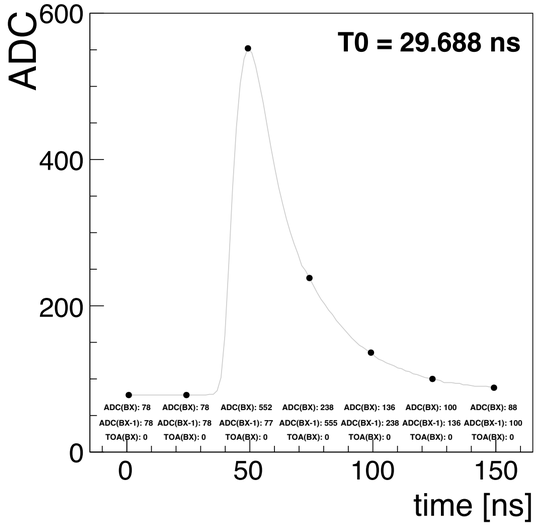
- This is real data, using the real shaper extracted from the ROC
- Each run was 5000 events:
  - Caveat = each point now is independent run
    - VHI10 problem, see slide 5
  - Then the ADC(BX), ADC(BX-1), TOA… etc means are extracted from 5000 measurements
  - This may result that the ADC(BX-1) != ADC(BX) - 25ns
- T0 = when the particle signal happened:
  - In EIC we expect ~10ns incident periods

How it would look in ePIC









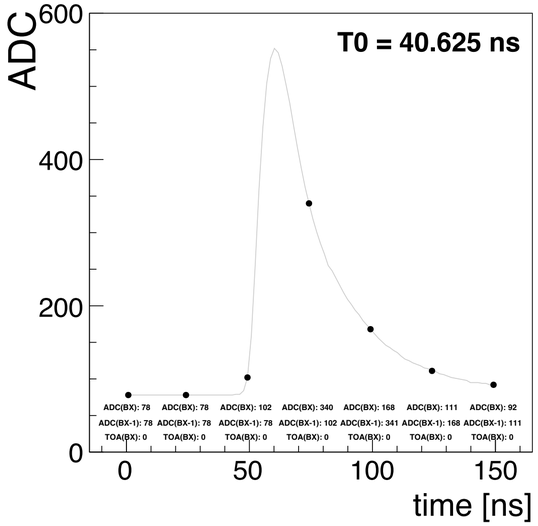


Illustration with real data:

- Each signal is shifted by about 10ns
- The points represent the samples we will obtain
- Numbers below the points show exactly the measurement

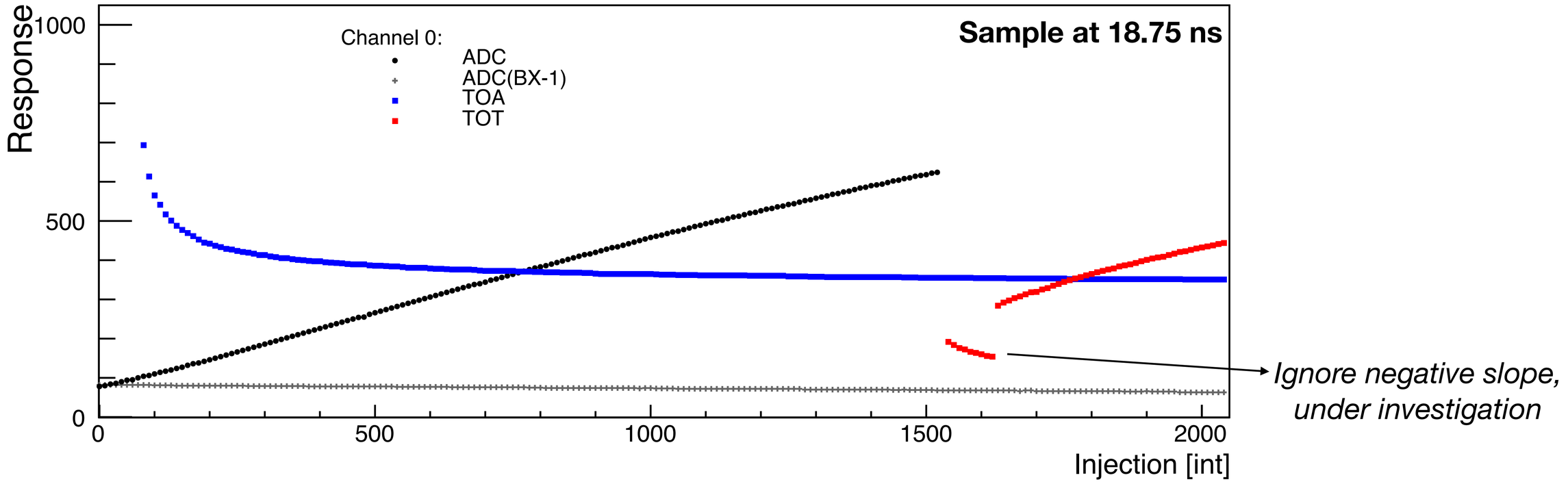
Reminder:
ADC(BX-1) != ADC(BX)-25ns,
because how the data is obtained

TOA and TOT calibration

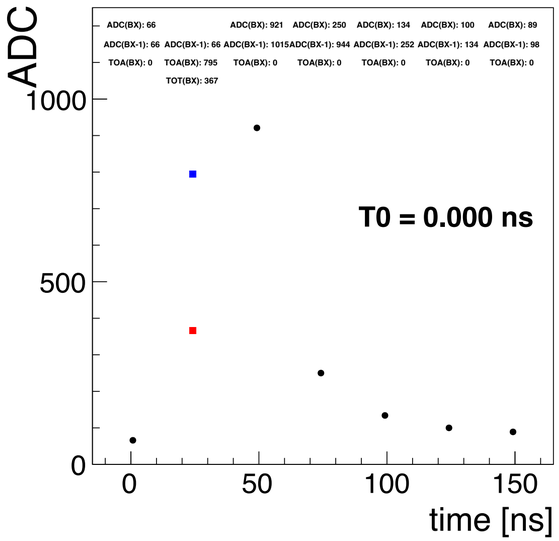
This is done with one fixed time for now (one sample from the whole shape)
Went through the lengthy calibration procedure for TOA and TOT:

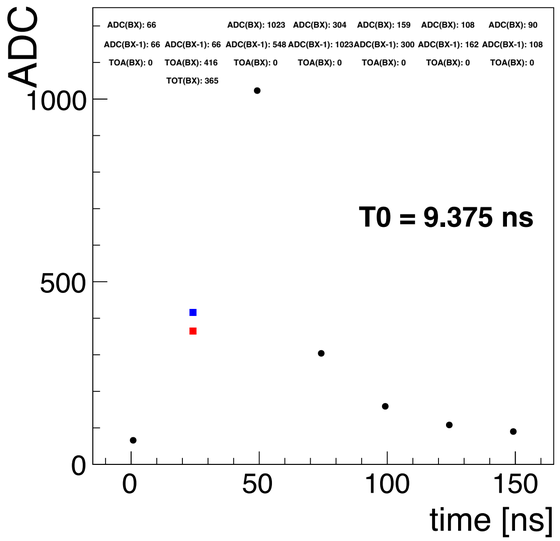
1. Set TOA global thresholds (for each side of the chip)
2. Set fixed injection large enough to pass TOA threshold
3. Scan channel-by-channel the TOA thresholds (5-bit 0..31)
4. Set channel-by-channel TOA for each channel, scan for two chip-halves
5. Set the global threshold so each half of the chip respond the same

… repeat again for TOT with larger injection, so it passes the desired TOT threshold



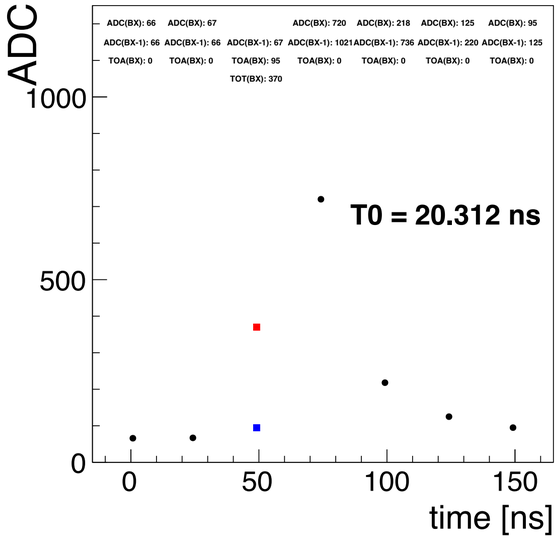
Sampling when reaching TOA/TOT

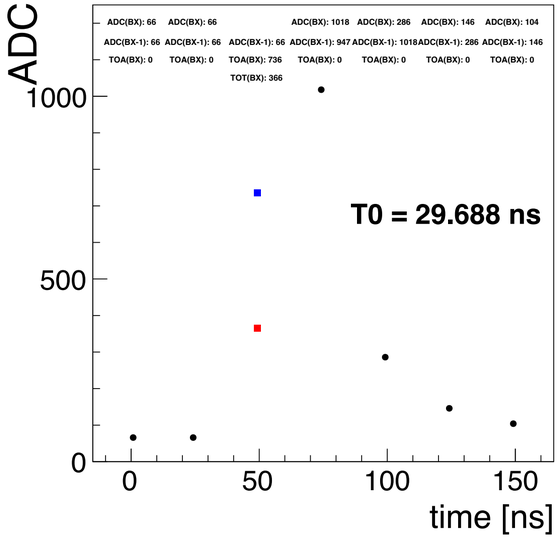


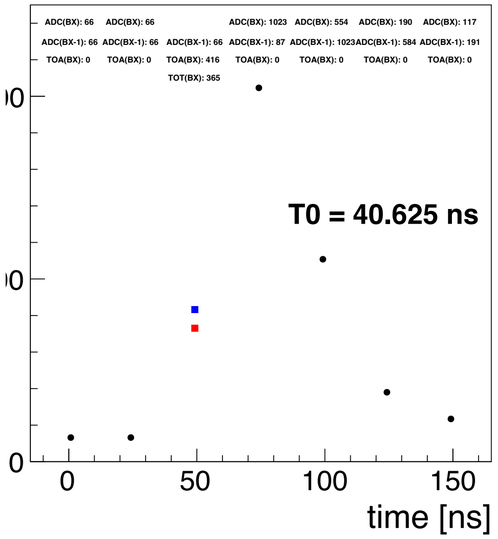


Same signal in different phases:

- TOA is changing - giving a clue in which phase we are
- TOT is constant
- Note the change of the data structure when the TOT is reached





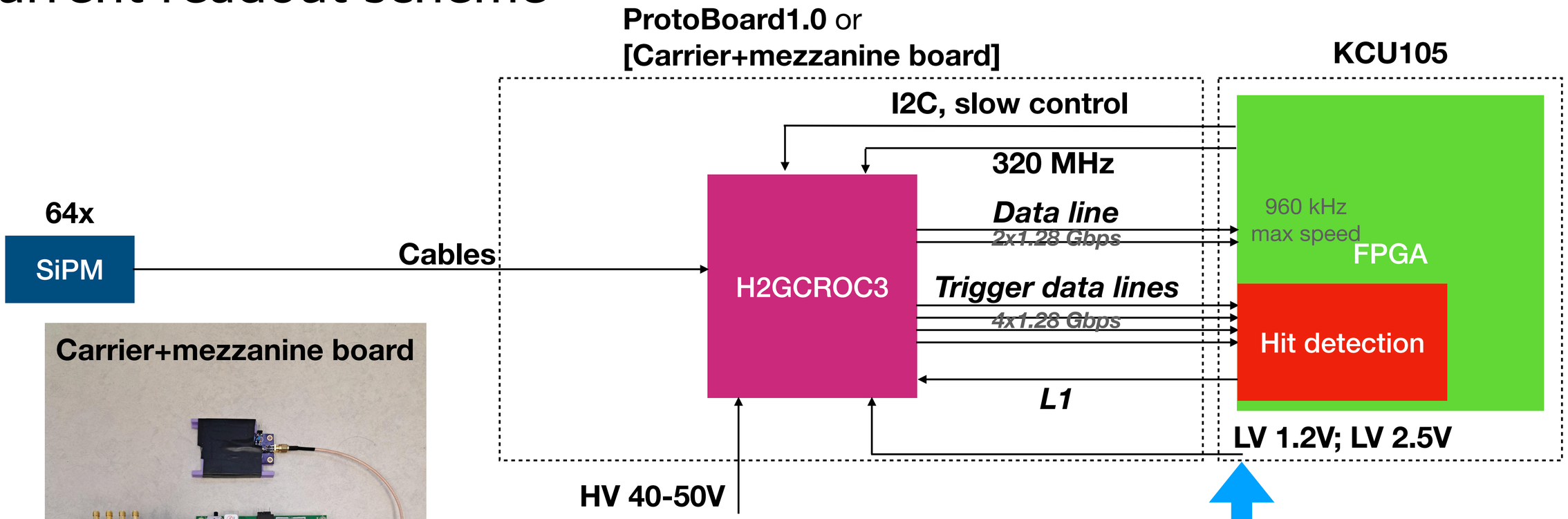


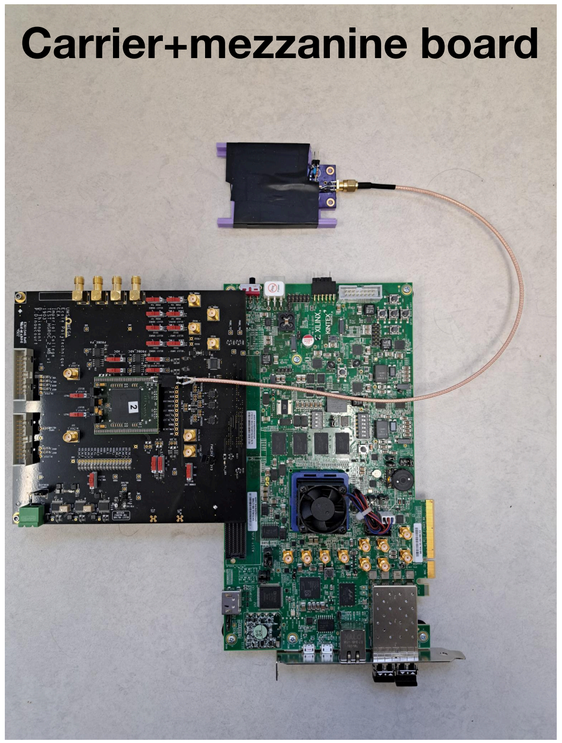
Using the TOT/ADC slope calibration, one can easily calculate the ADC_equivalent (as ADC is saturated) value

$$ADC_{\mathrm{eq}} = f_{\mathrm{adc}}\left[f_{\mathrm{tot}}^{-1}(TOT)\right]$$

$$ADC_{\mathrm{eq}} \sim 15\mathrm{bit\ value}$$

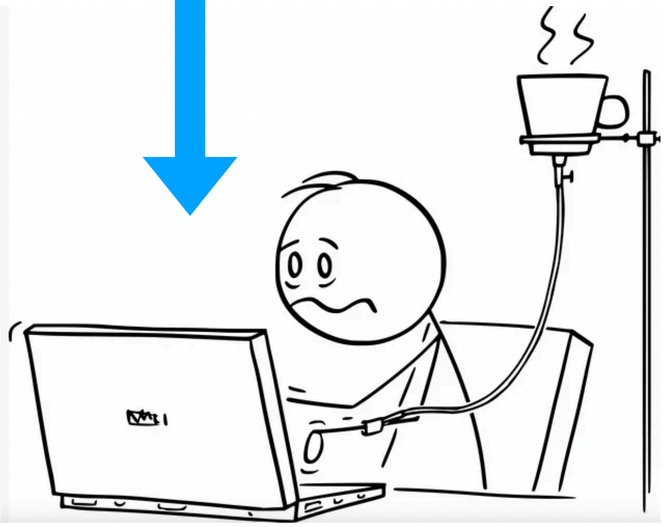
Current readout scheme





The firmware, software is set:

- Self triggering mode - we can decode the information in KCU and send a trigger signal (for now 1 usec dead-time is set)
- External triggering - any 1.8V signal can be accepted as trigger input



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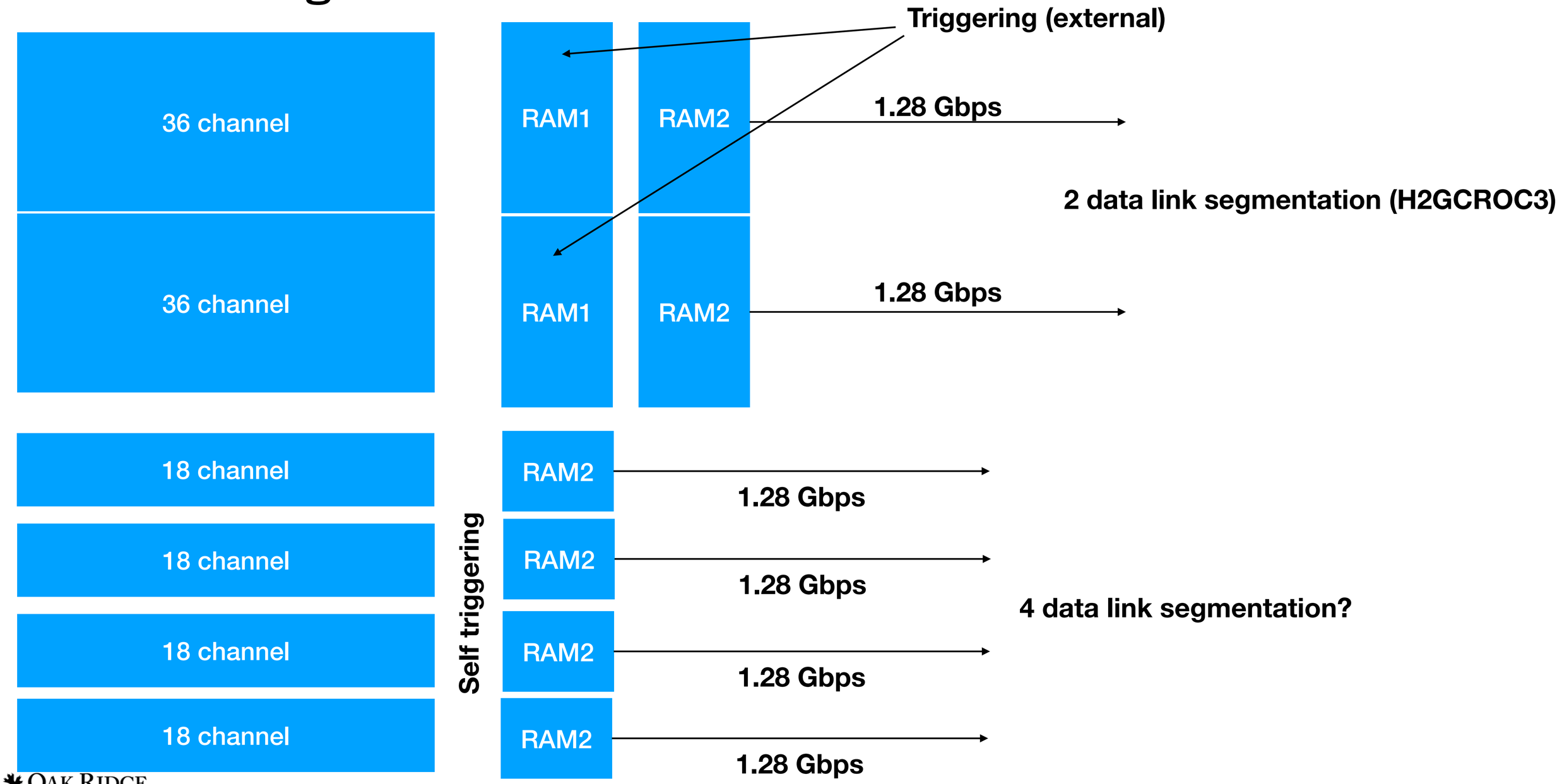
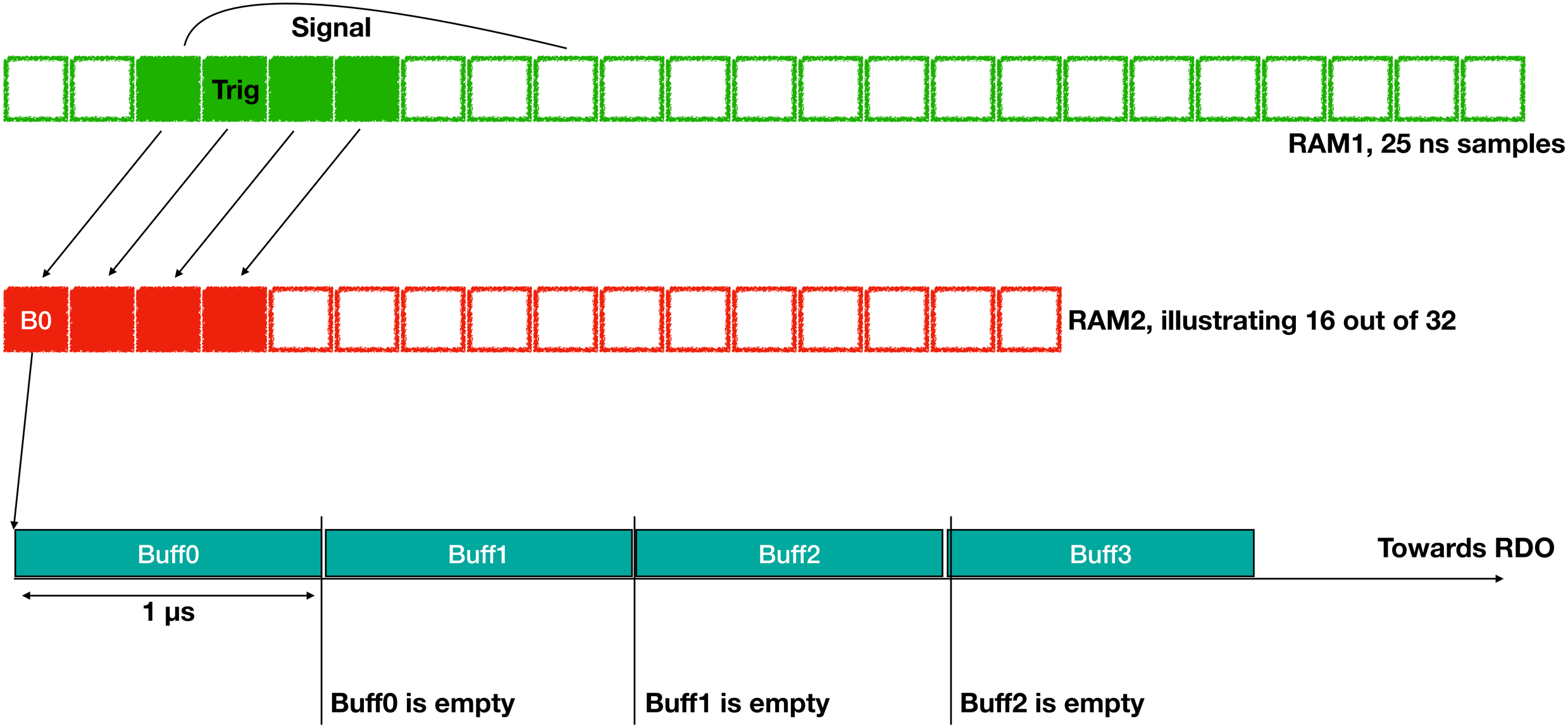
Backup

Illustration segmentation



Illustration



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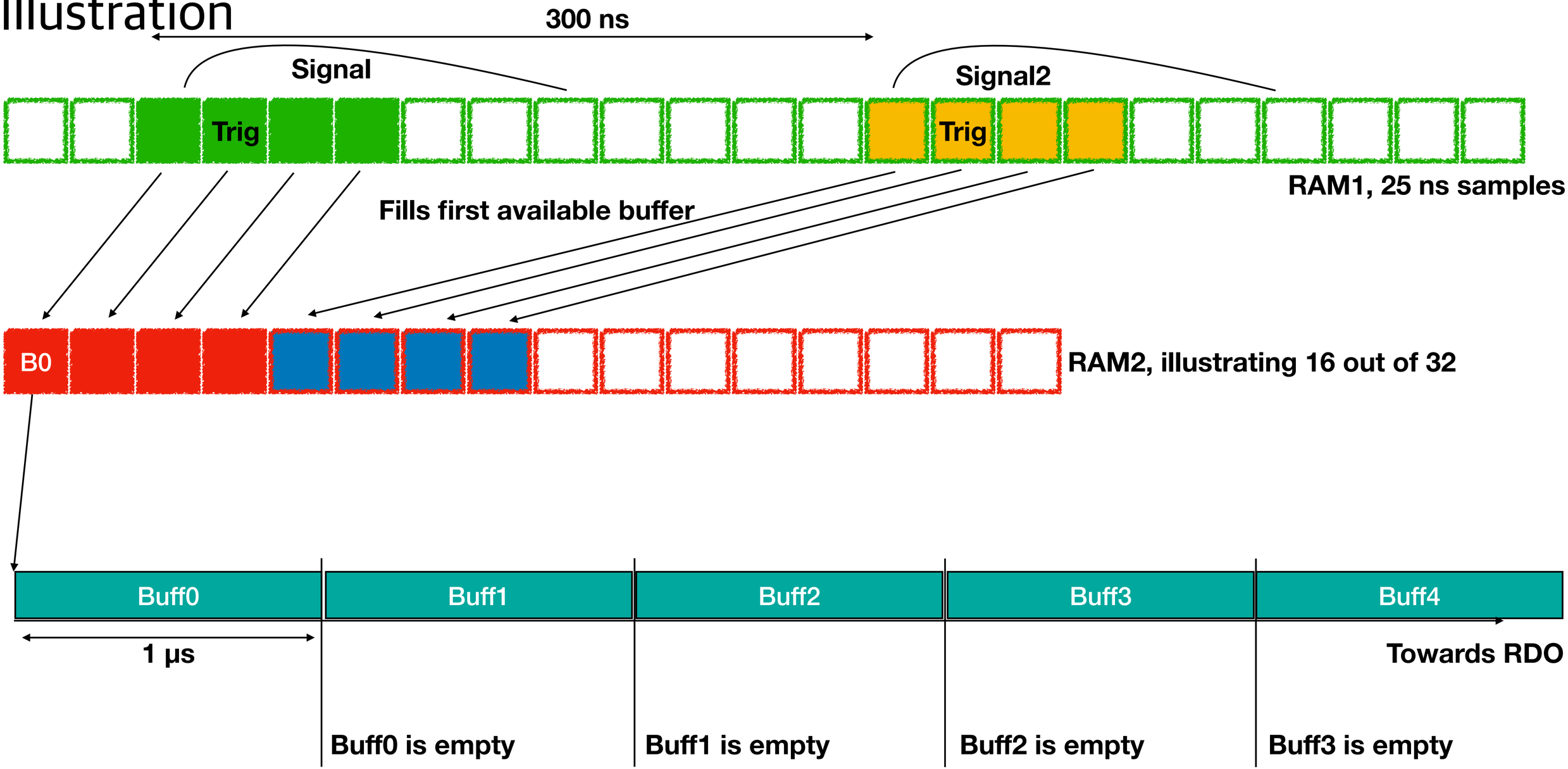
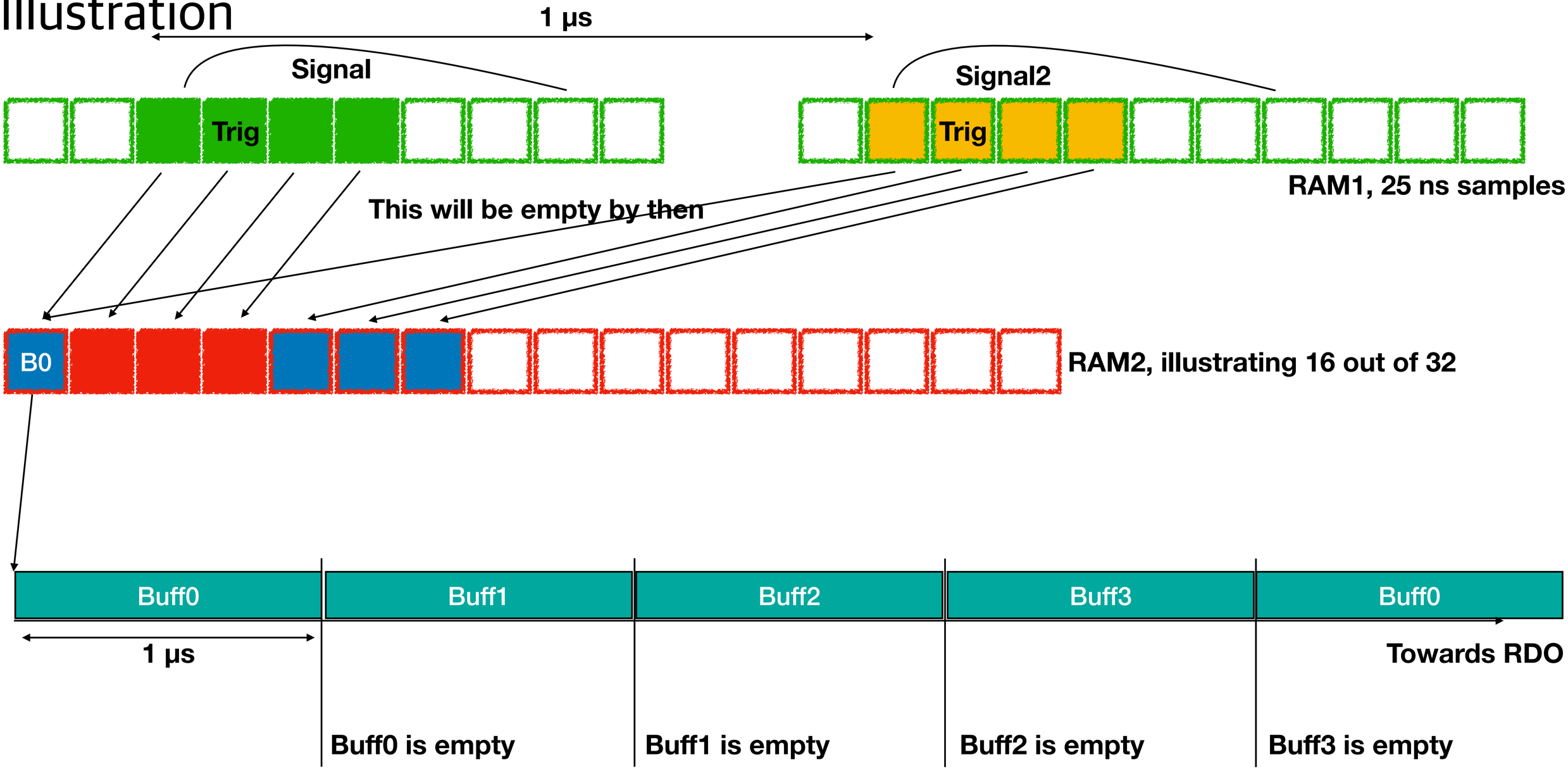
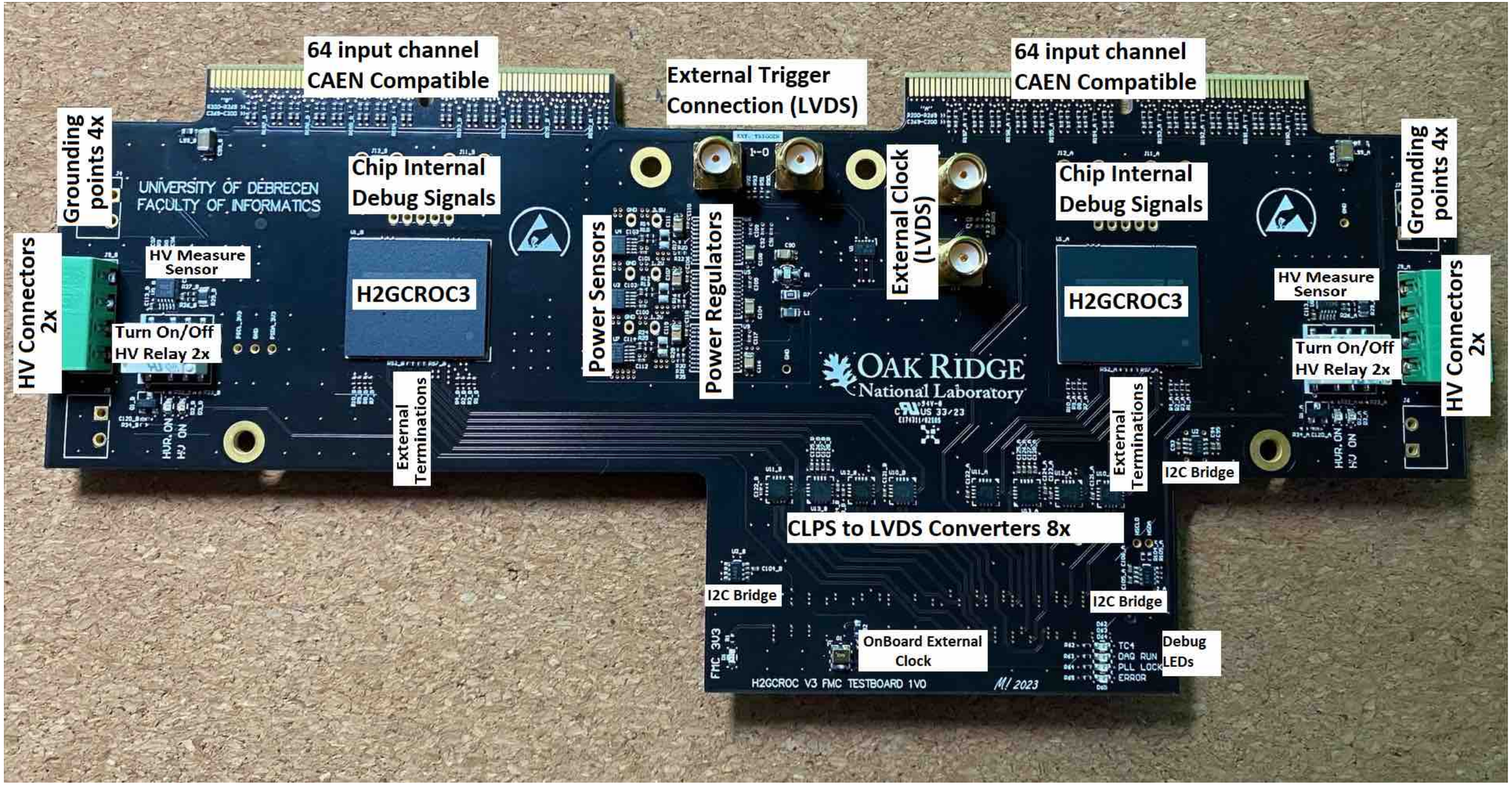


Illustration



ProtoBoard1.0 (we have 2 of these)



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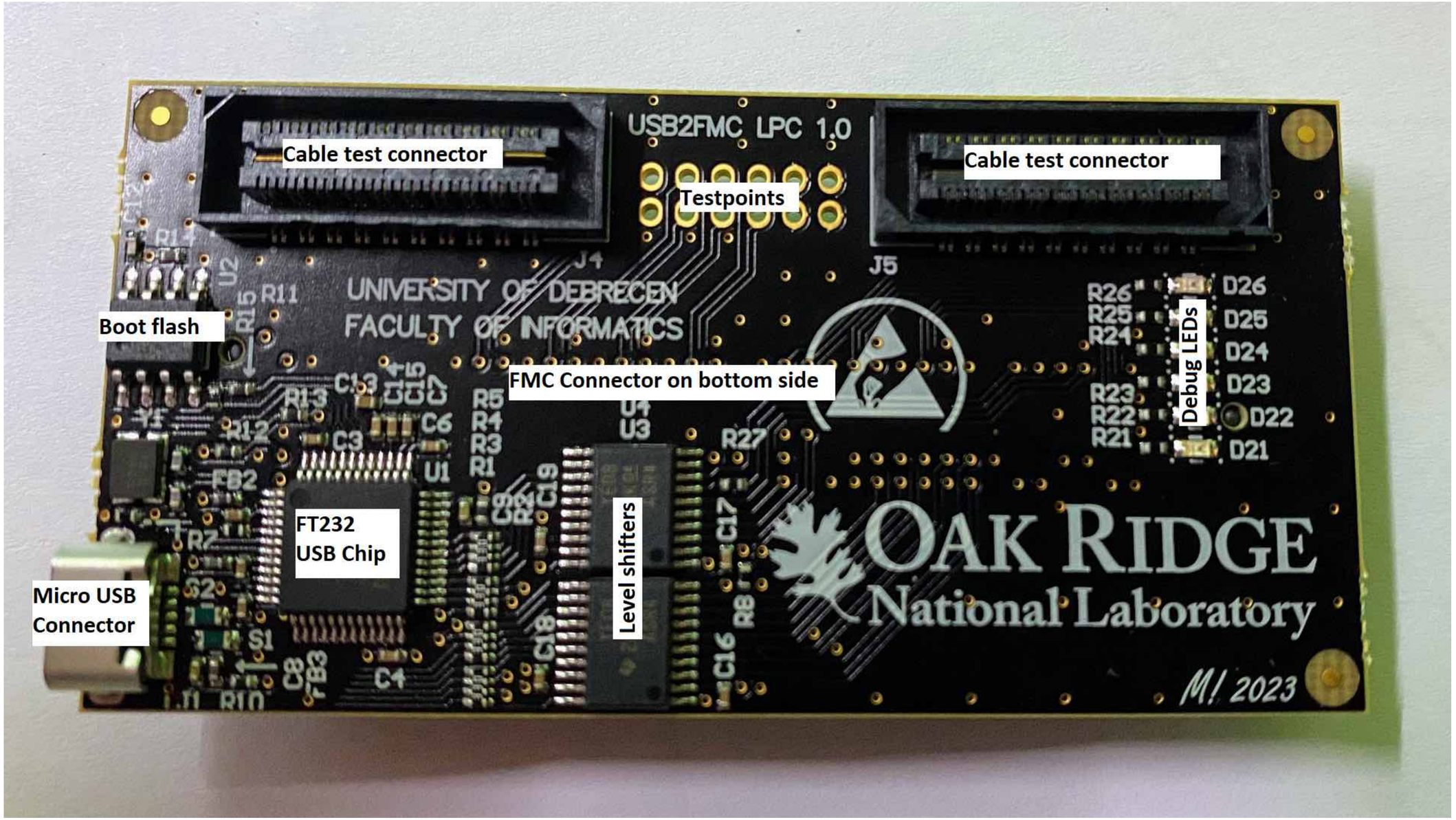
ComBoard1.0 (we have 5 of these)



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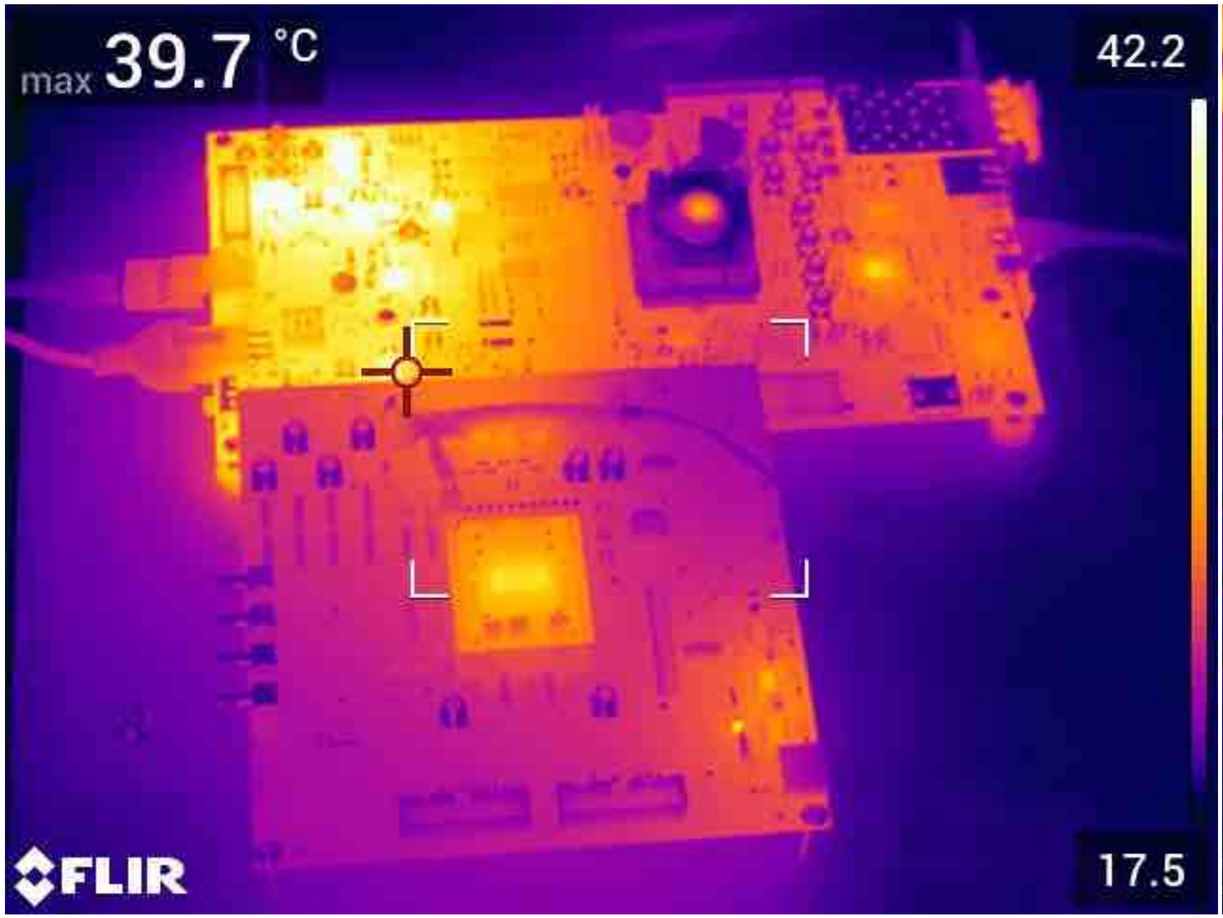
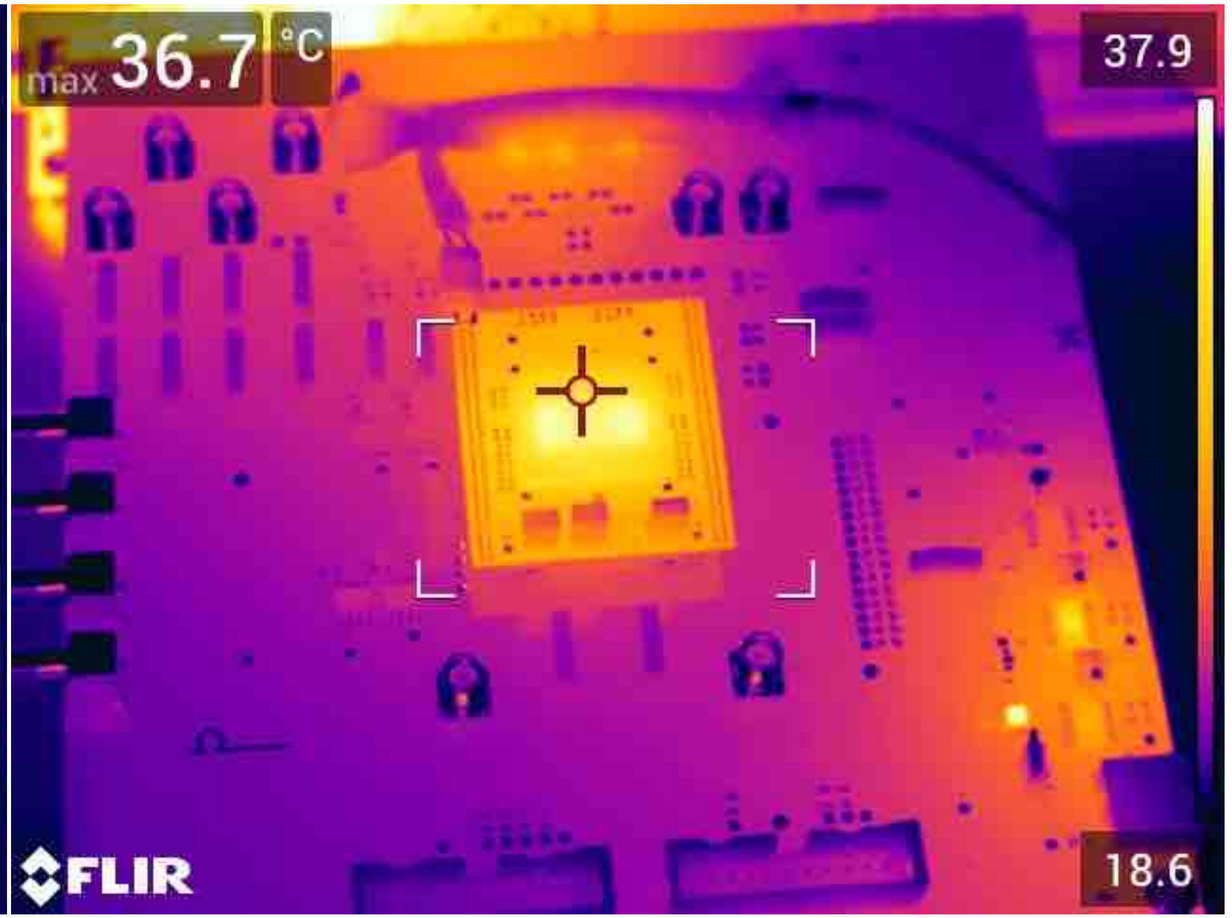
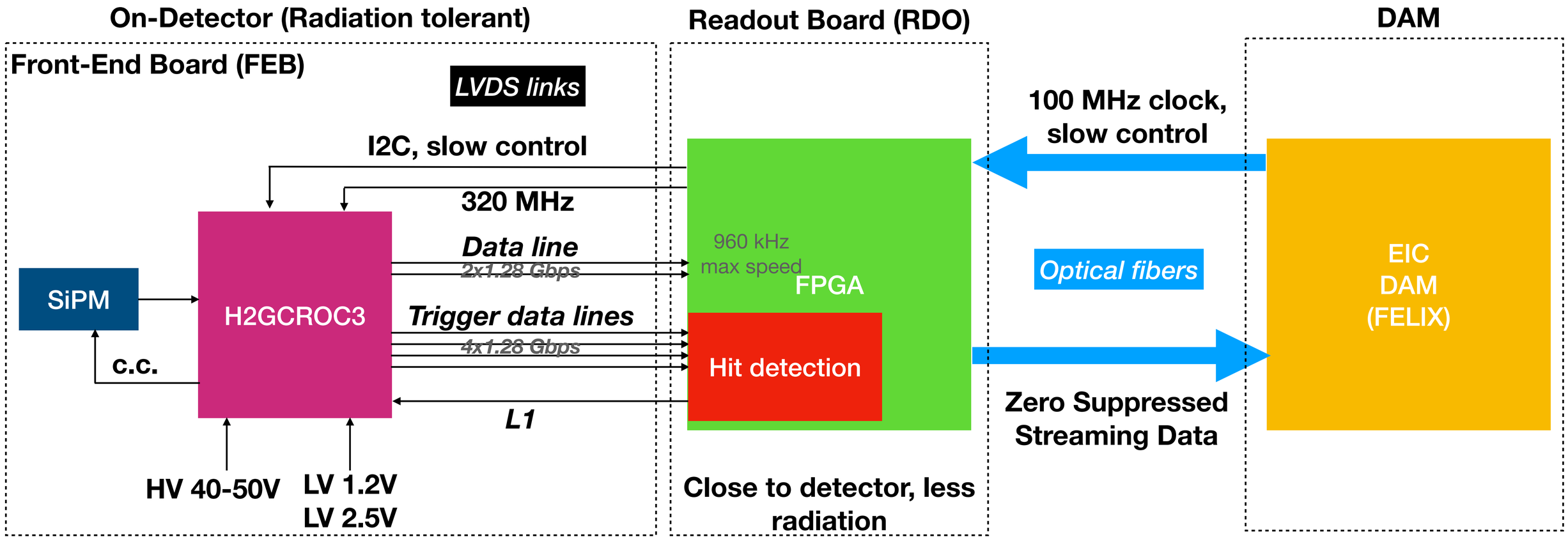
Some IR pictures while working





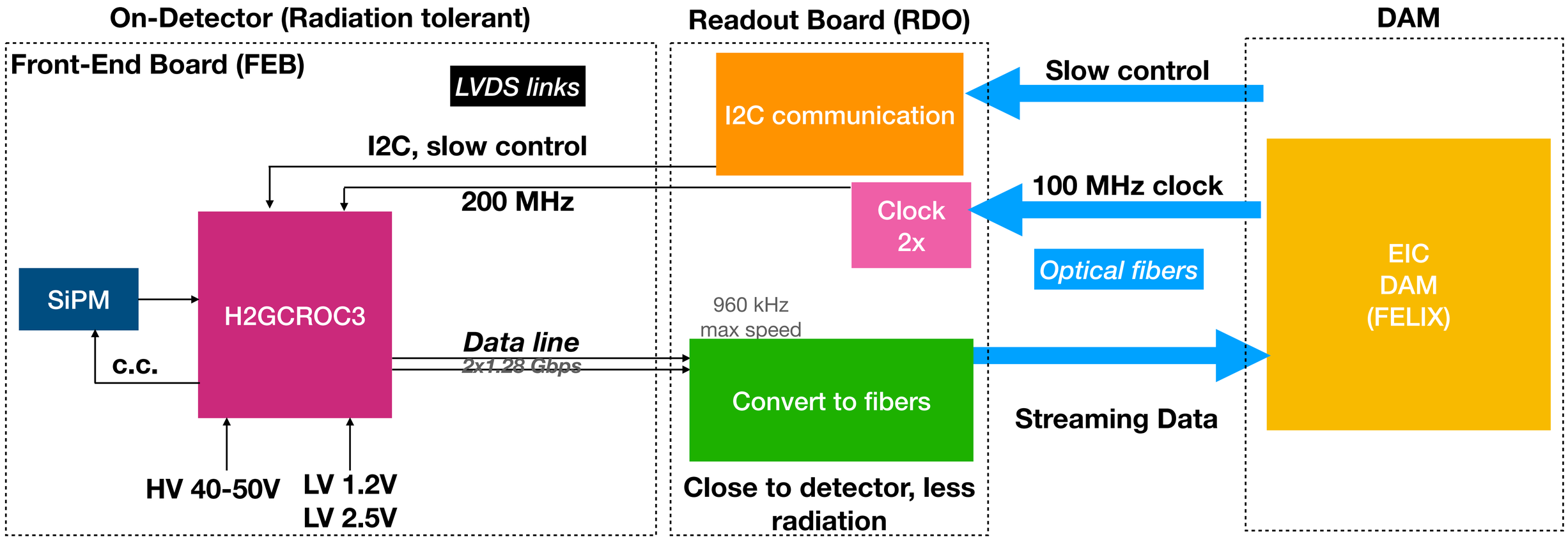
LFHCal readout hierarchy (as of now)



Data propagation from the detector to the EPIC DAQ system:

- The H2GCROC3 requires the L1 trigger for readout, with the maximum speed of 960 kHz
- The expected hit rate in **one channel of LFHCal** is up to 50 kHz:
  - With possible 4 sample readout we would reach a maximum of 200 kHz
  - Streaming readout towards the EPIC DAQ system

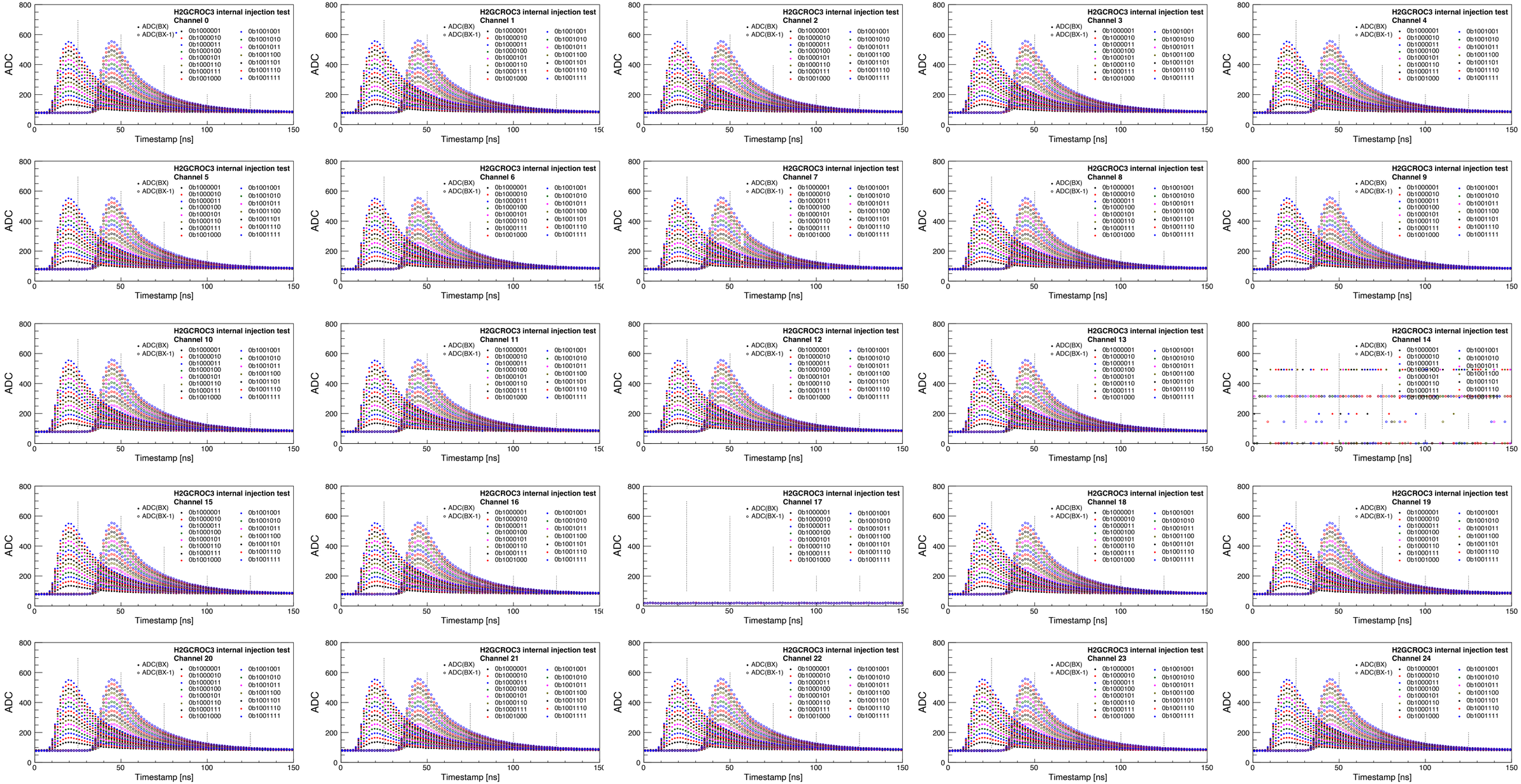
LFHCal readout hierarchy (after the upgrade)



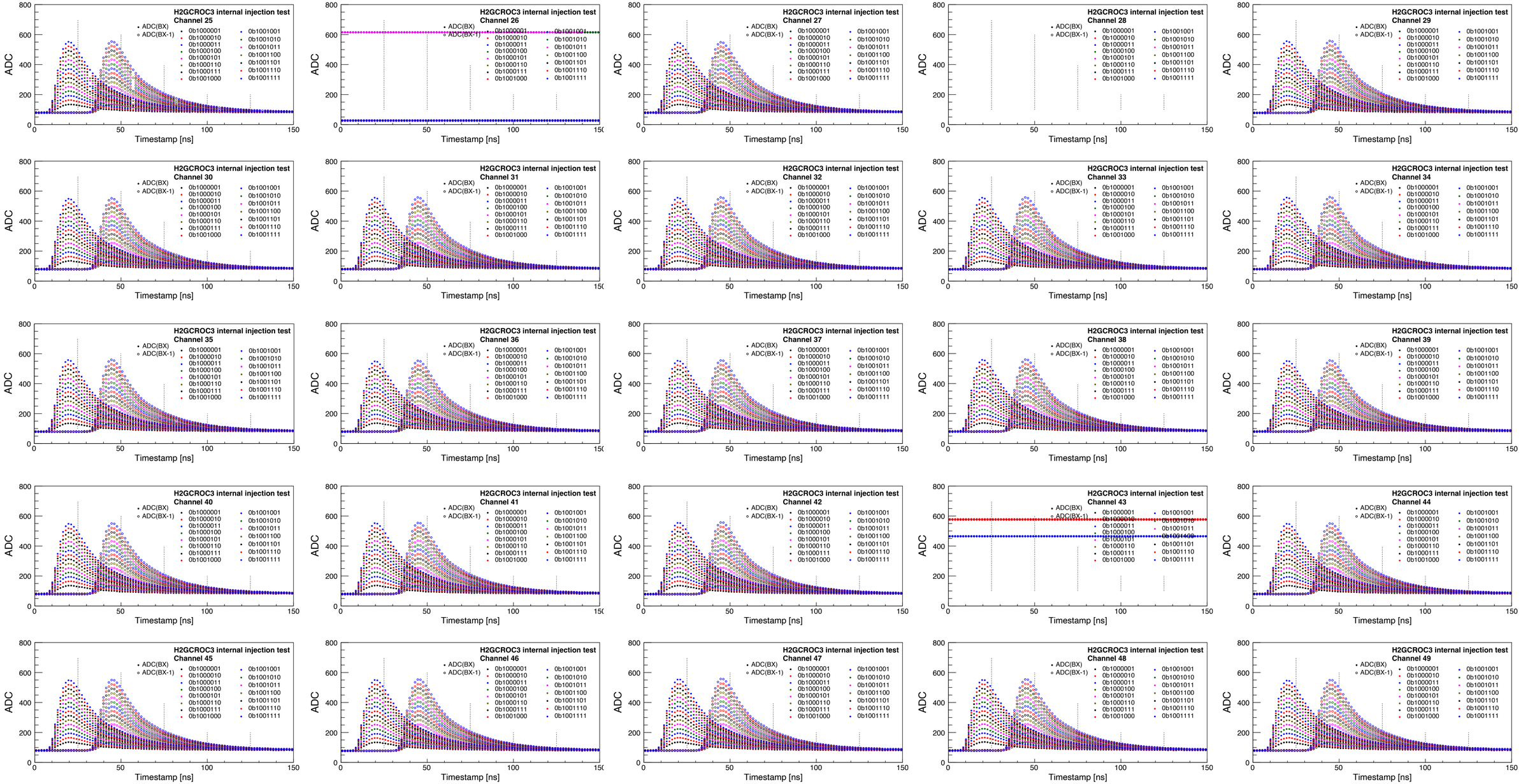
Data propagation from the detector to the EPIC DAQ system:

- The H2GCROC3 requires the L1 trigger for readout, with the maximum speed of 960 kHz
- The expected hit rate in **one channel of LFHCal** is up to 50 kHz:
  - With possible 4 sample readout we would reach a maximum of 200 kHz
  - Streaming readout towards the EPIC DAQ system

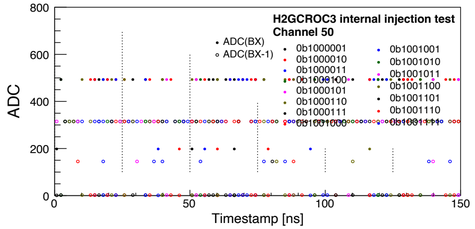
Injection

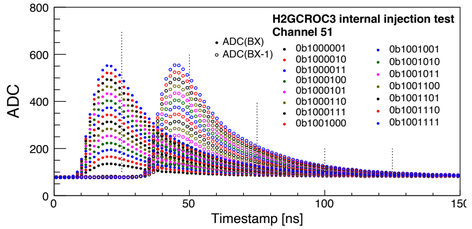

H2GCROC3 internal injection test
Channel 0
Channel 1
Channel 2
Channel 3
Channel 4
Channel 5
Channel 6
Channel 7
Channel 8
Channel 9
Channel 10
Channel 11
Channel 12
Channel 13
Channel 14
Channel 15
Channel 16
Channel 17
Channel 18
Channel 19
Channel 20
Channel 21
Channel 22
Channel 23
Channel 24
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

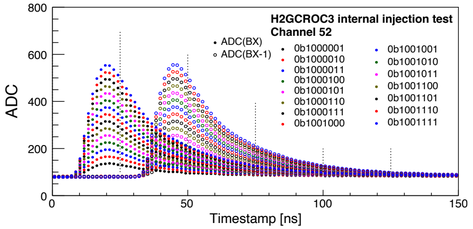
Injection

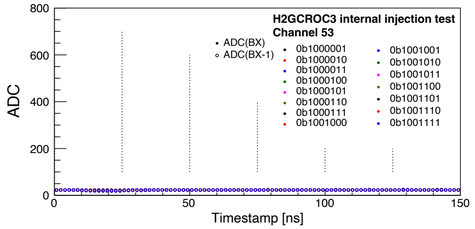

H2GCROC3 internal injection test
Channel 25
Channel 26
Channel 27
Channel 28
Channel 29
Channel 30
Channel 31
Channel 32
Channel 33
Channel 34
Channel 35
Channel 36
Channel 37
Channel 38
Channel 39
Channel 40
Channel 41
Channel 42
Channel 43
Channel 44
Channel 45
Channel 46
Channel 47
Channel 48
Channel 49
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

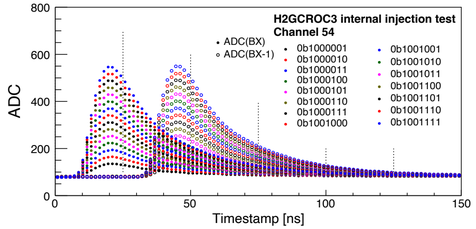
Injection

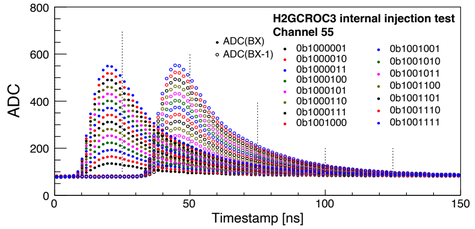

H2GCROC3 internal injection test
Channel 50
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

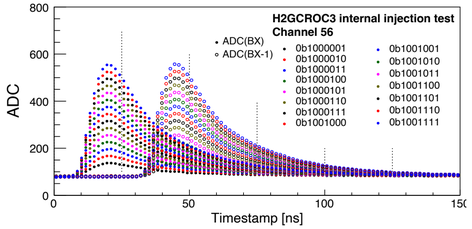

H2GCROC3 internal injection test
Channel 51
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

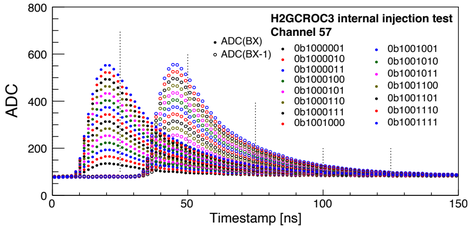

H2GCROC3 internal injection test
Channel 52
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

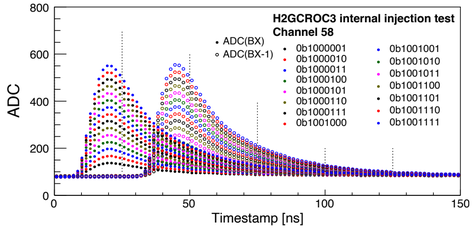

H2GCROC3 internal injection test
Channel 53
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

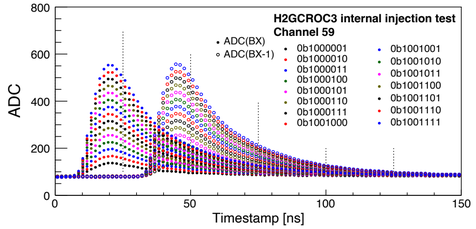

H2GCROC3 internal injection test
Channel 54
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

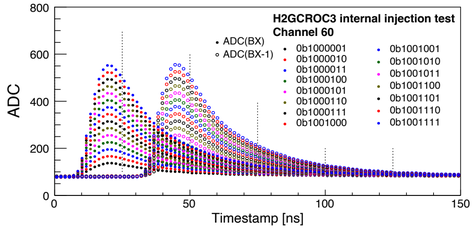

H2GCROC3 internal injection test
Channel 55
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

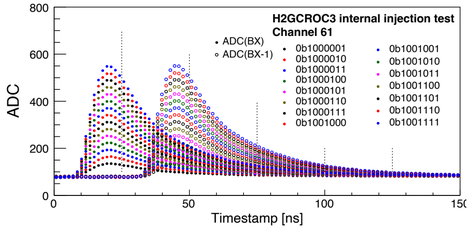

H2GCROC3 internal injection test
Channel 56
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

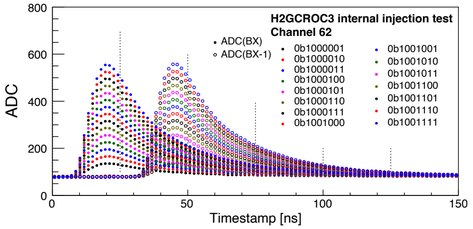

H2GCROC3 internal injection test
Channel 57
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

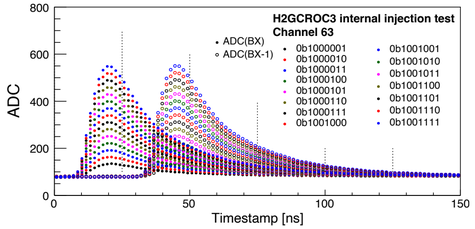

H2GCROC3 internal injection test
Channel 58
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

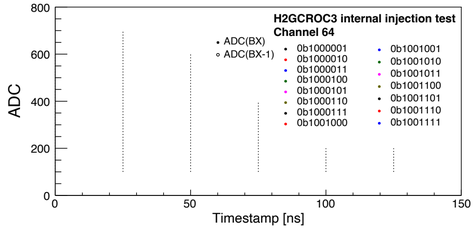

H2GCROC3 internal injection test
Channel 59
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

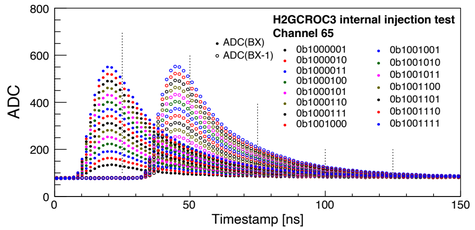

H2GCROC3 internal injection test
Channel 60
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

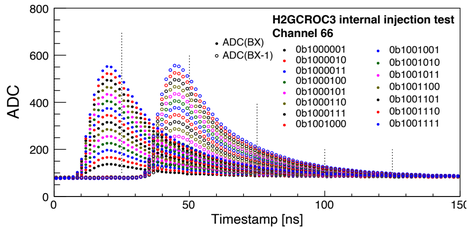

H2GCROC3 internal injection test
Channel 61
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

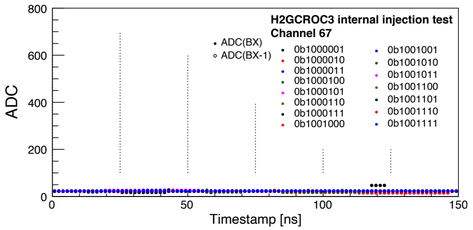

H2GCROC3 internal injection test
Channel 62
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

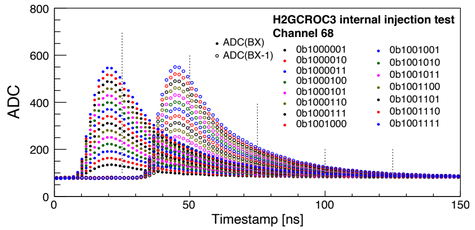

H2GCROC3 internal injection test
Channel 63
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

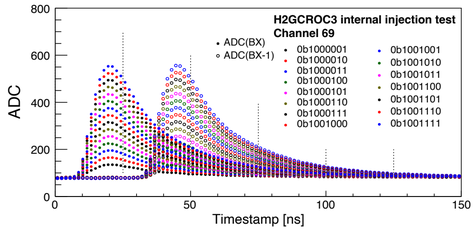

H2GCROC3 internal injection test
Channel 64
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

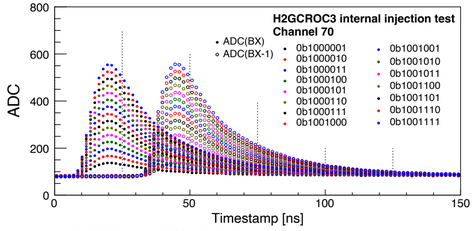

H2GCROC3 internal injection test
Channel 65
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

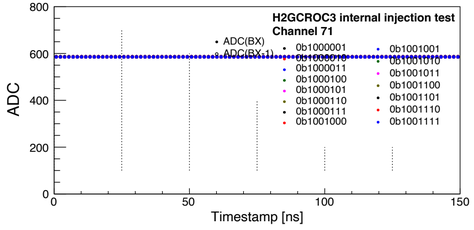

H2GCROC3 internal injection test
Channel 66
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]


H2GCROC3 internal injection test
Channel 67
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]


H2GCROC3 internal injection test
Channel 68
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]


H2GCROC3 internal injection test
Channel 69
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]


H2GCROC3 internal injection test
Channel 70
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]


H2GCROC3 internal injection test
Channel 71
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]