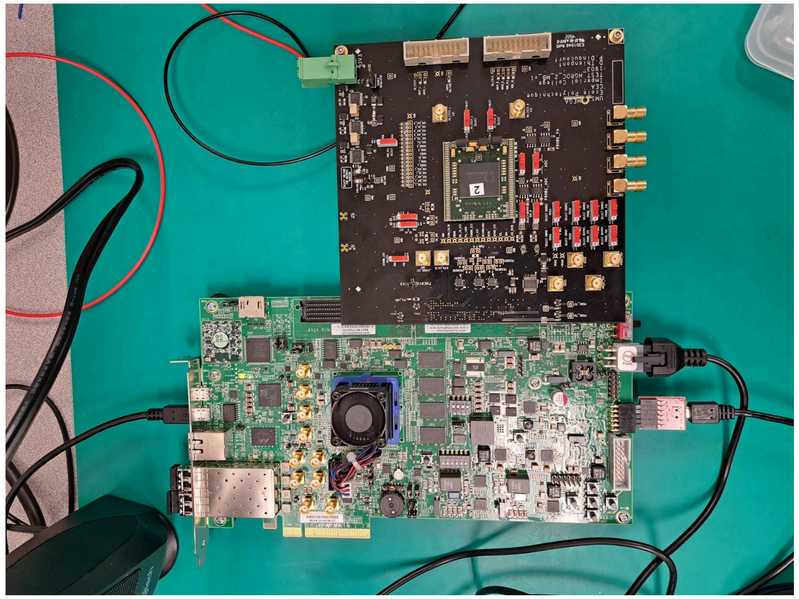
OAK RIDGE National Laboratory

H2GCROC3A testing

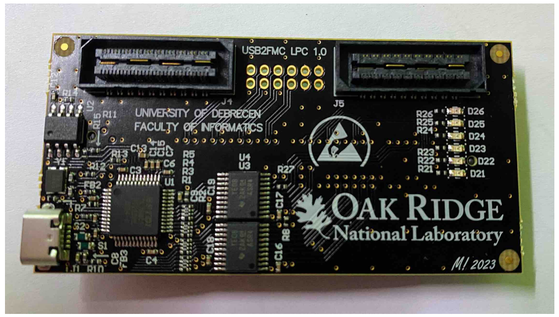
Norbert Novitzky
(ORNL)
Miklos Czeller, Gabor Nagy
(Debrecen)
Nov 1st, 2023

What do we have? What we produced so far



First mezzanine + carrier board designed by Omega:

- Received the chip and produced couple of mezzanines and carrier boards for testing
- Understanding the communication, setup of the chip
- We can physically solder inputs (SiPM) on channels, but this is more for single-channel testing



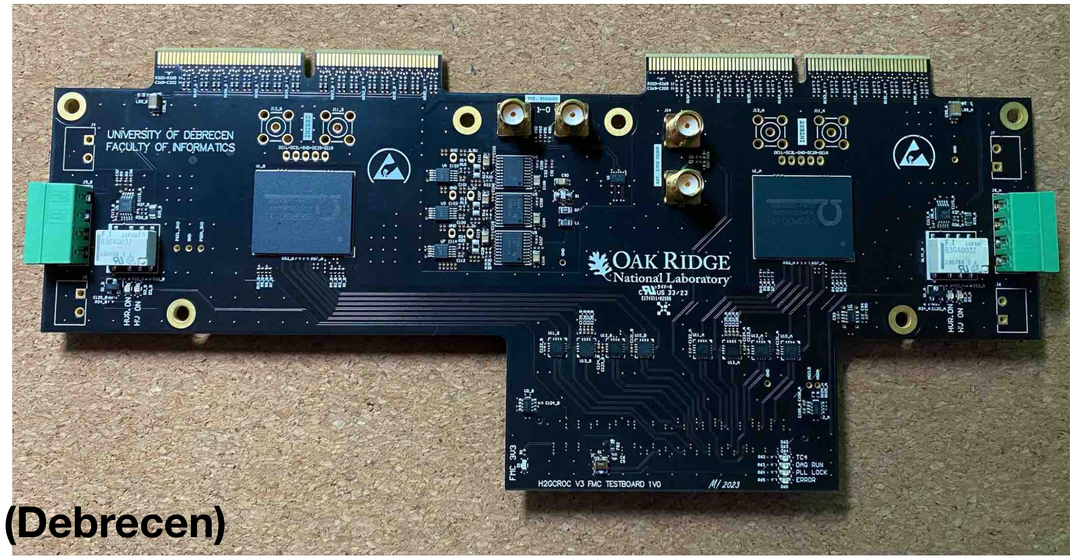
ComBoard1.0:

- USB3 readout communication
- Testing the Samtec Cables (connectors attached)

ProtoBoard1.0:

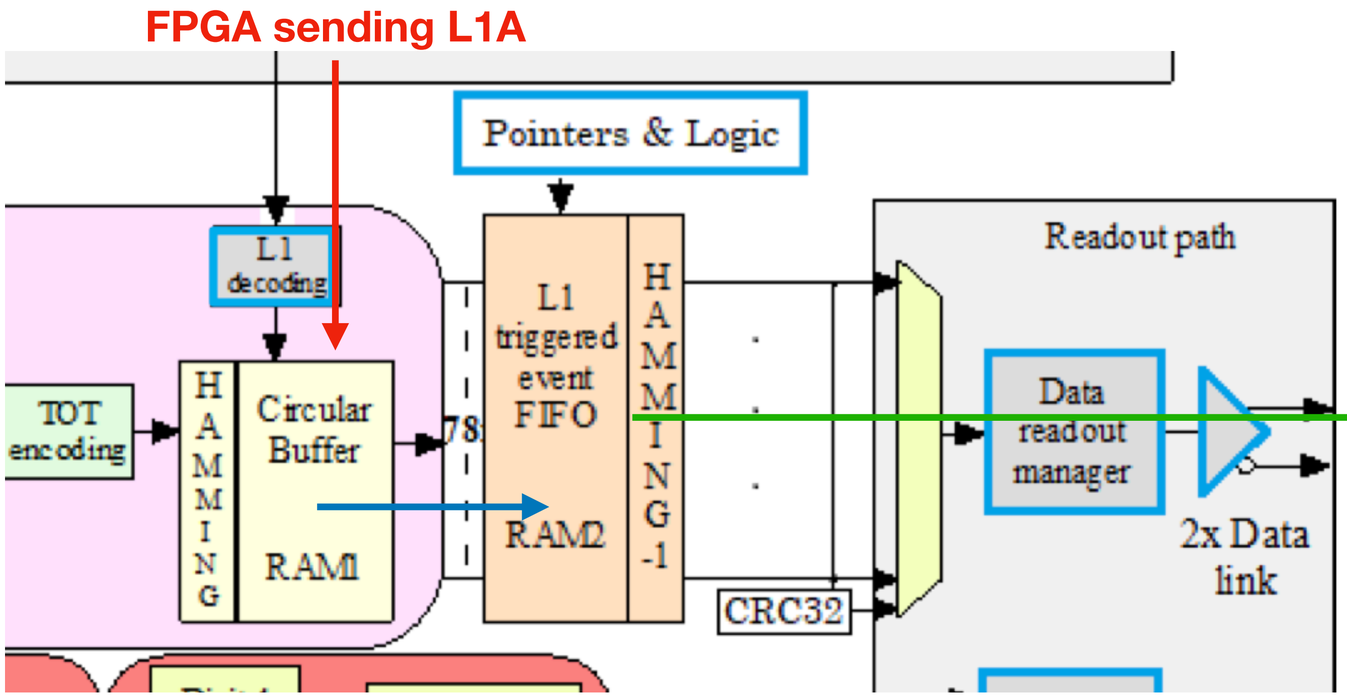
- Produced 2 of these boards so far with H2GCROC3A
- Made so it is compatible with the CAEN commercial readout
  - The upper golden pins can accept the CAEN backboards (2x)
- 64x2 = 128 channel readout - not every of the 72 channel is connected
- LVDS readout via the FMC connector
- Compatible with the KCU105 (firmware, software done):
  - Still work-in-progress, there are improvements coming as we speak

ProtoBoard1.0



Thanks a lot to Miklos Czeller and Gabor Nagy (Debrecen)

One known problem quickly discovered – this is only H2GCROC3A



How we see it working:

1. **FPGA sends an L1A trigger signal**
2. **RAM1->RAM2 moving data**
3. **RAM2 trickles down the data as they come in**

Problem arrises in step 2:

- **When RAM1—>RAM2 move is done, the power can decrease**
- **If the next L1A comes quickly, then it might flip 1—>0 bit**
- **Depends on the frequency of the L1A coming in**

Problem fix:

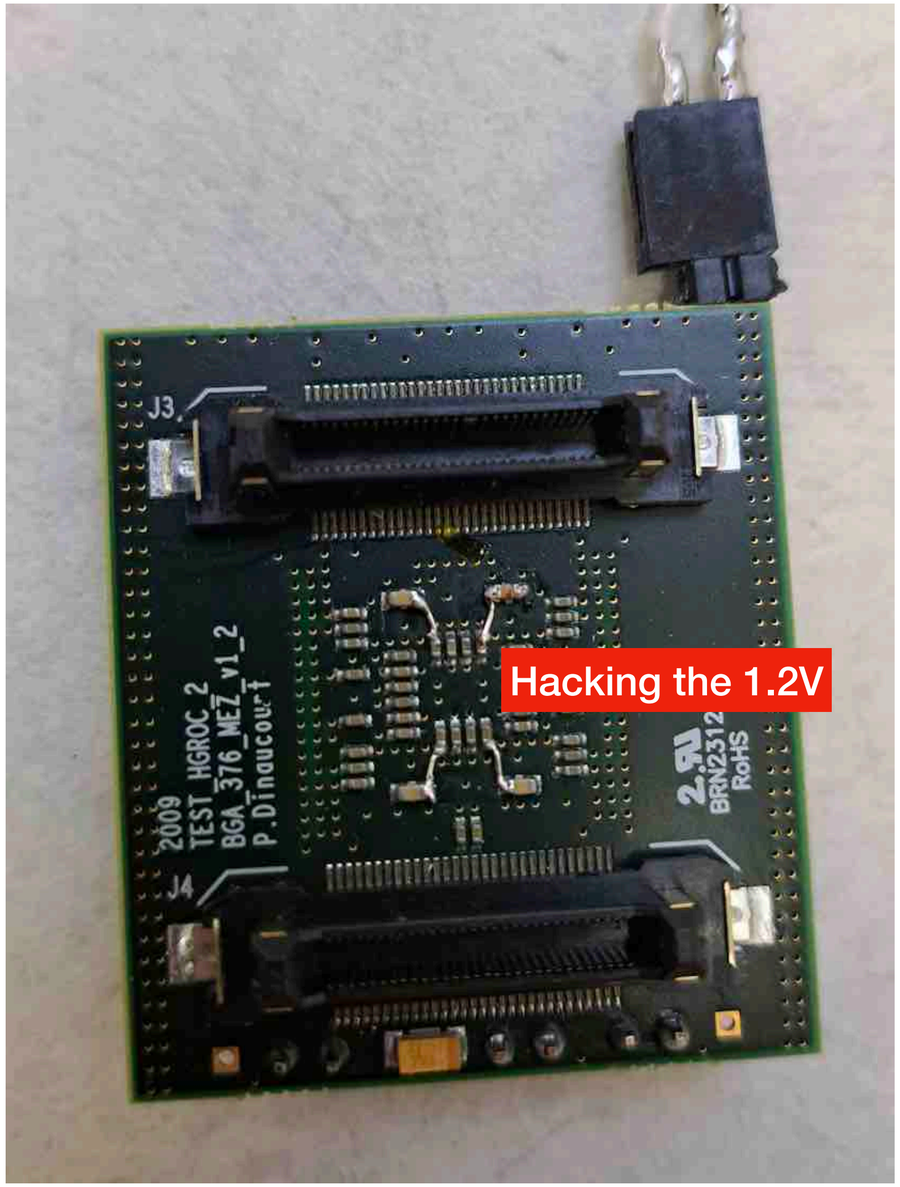
- Connect the VH10 pin to the 1.2 V
- This prevents the drop of power and corruption of the data
- Hamming code has to be ==0 in order to see no corruption

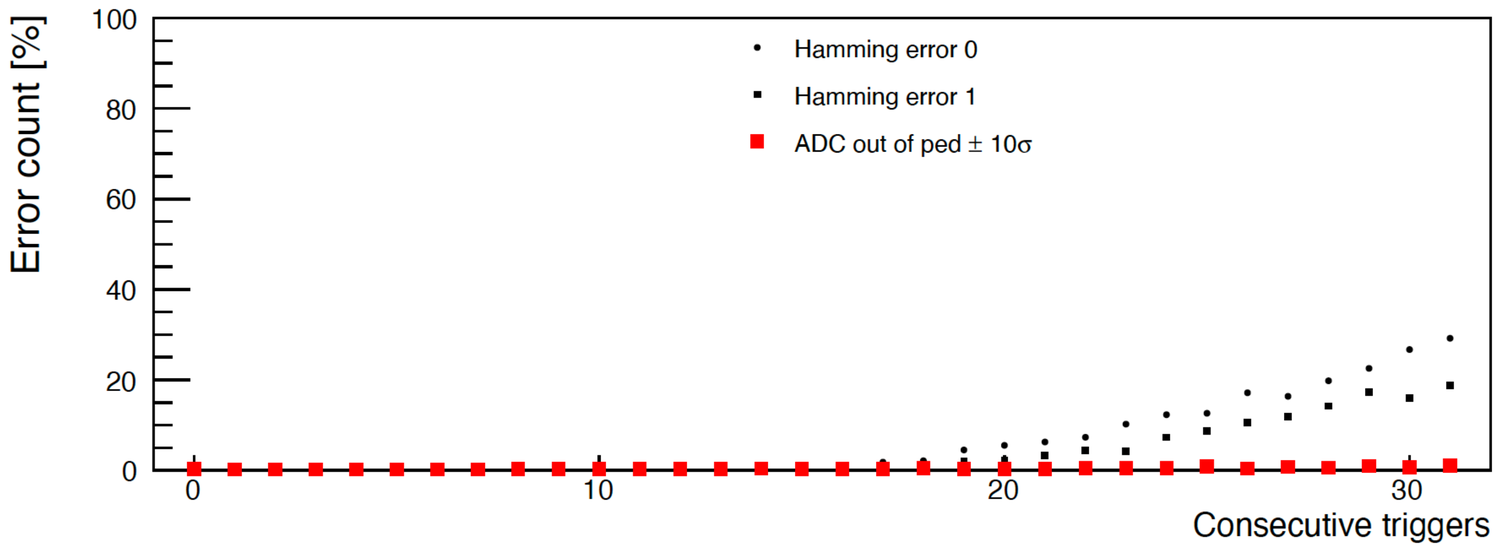
This problem is annoying, we fix it with implementation of dead time. We found 1 μs is sufficient for see no significant Hamming code errors

We connected the 1.2V and will retest

This bug is fixed in the H2GCROC3B - available in early November

Fixed

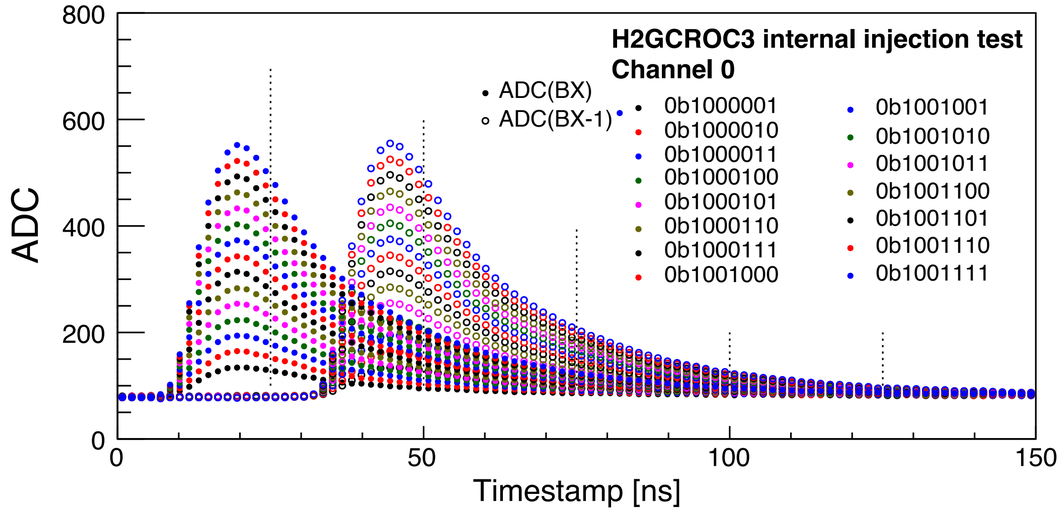




The depth of RAM2 is 32:

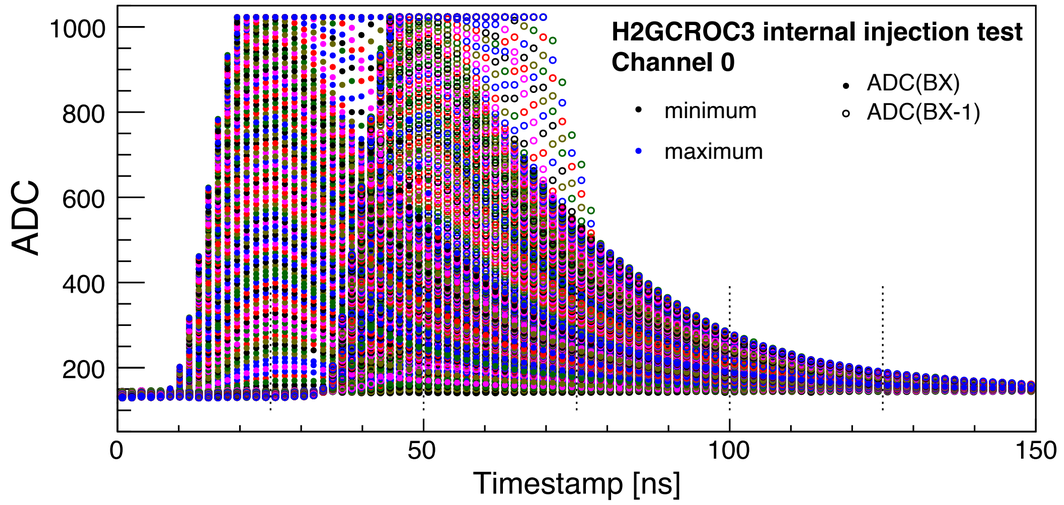
- Implemented machine-gun trigger (consecutive bunch crossing)
- Up to 32 triggers to fill completely the secondary RAM:
  - 800 ns long sampling
- Checking Hamming Errors on both sides of the ROC:
  - Tells us the bit flip errors
  - Run each setup for 1k events
- We see no problem up to 18 consecutive triggers. Then there are some corrupted ones up to 30% of events at 32.

Signals!



Low injection test:

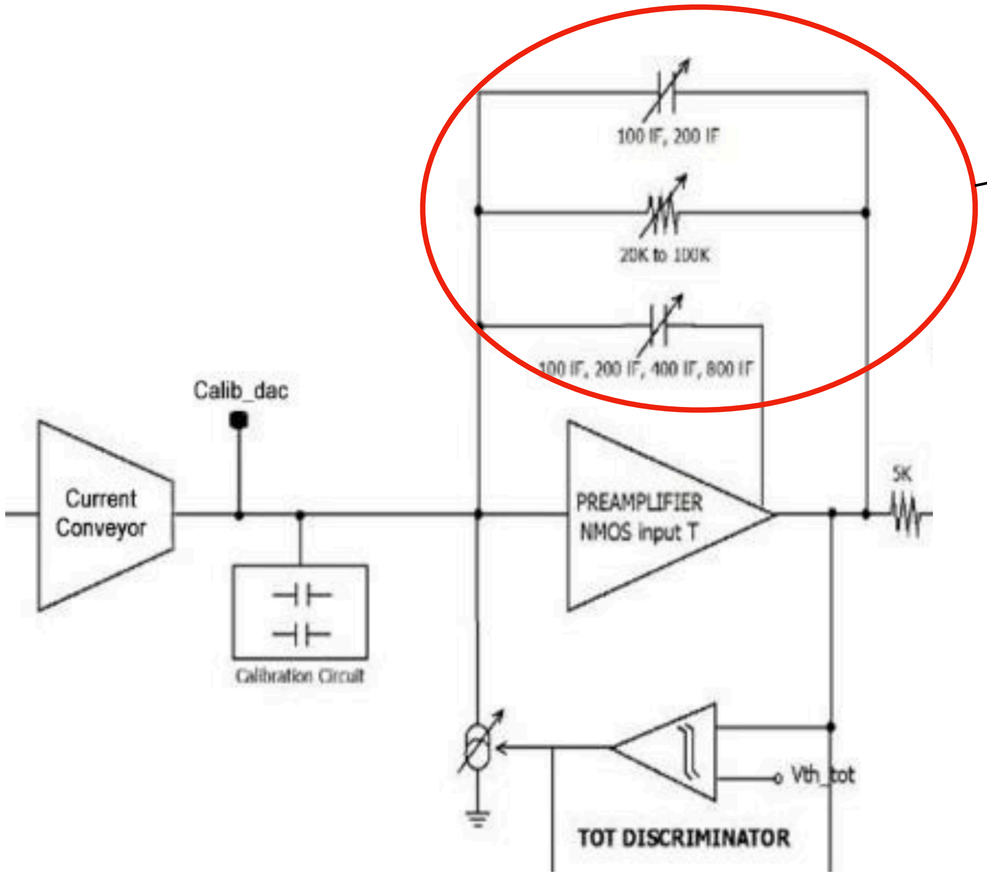
- The legend is different injections:
- 0b1001111 = low injection + “F00” = 3840 (almost maximum)
- Scanned the full shape of the signal:
  - The ADC and ADC(BX-1) is shown
- TOA and TOT purposefully turned off
- All channels were tested, in the backup



High injection test:

- TOA and TOT purposefully turned off
- Tested from lowest to higher signals
- Let the ADC saturate
- Shape is very consistent, does not change with the height

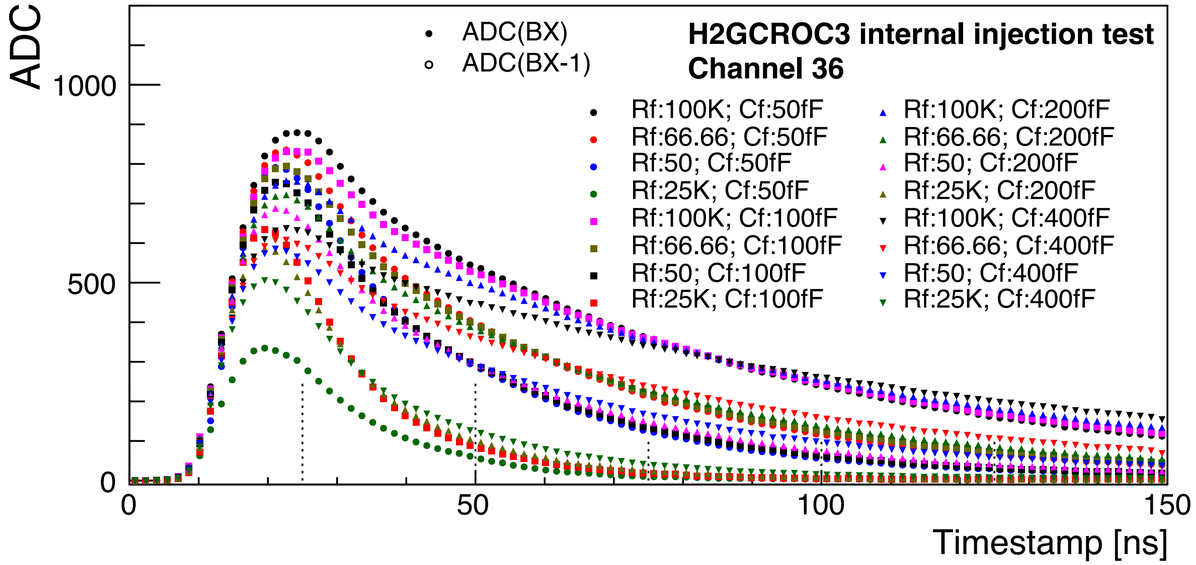
Gain checks



Cd (pF)	5, 10, 20	At the conveyor output and at the preamp input. To ensure the preamp stability.
Rf (Ω)	25K, 50K, 66.66K, 100K	In parallel, these resistors provide 15 values to be adjusted with the Cf and Cf_comp values to get the desired decay time constant.
Cf (fF)	50, 100, 200, 400	Combined with the Cf_comp capacitors, provide the gain of the preamplifier.
Cf_comp (fF)	50, 100, 200, 400	Same purpose than Cf capacitors but connected differently to improve the preamplifier stability. From gain point-of-view can be considered in parallel with Cf capacitors.

Table 1.1: Values for Rf, Cf and Cd

Same injection in the same channel

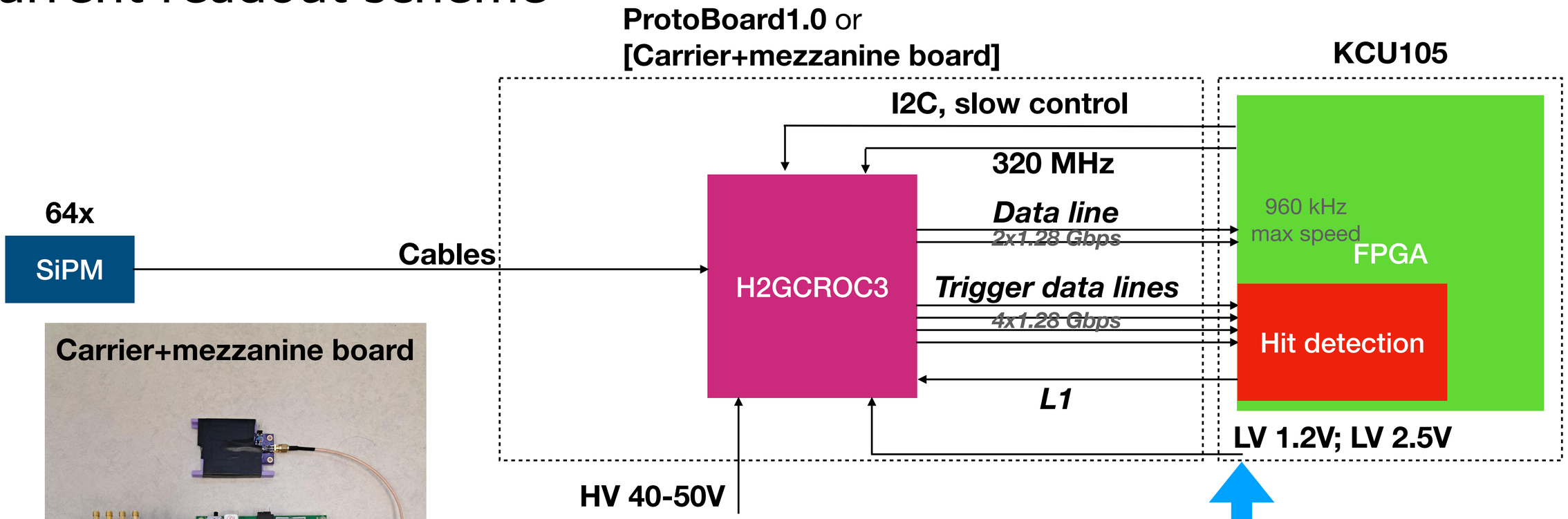


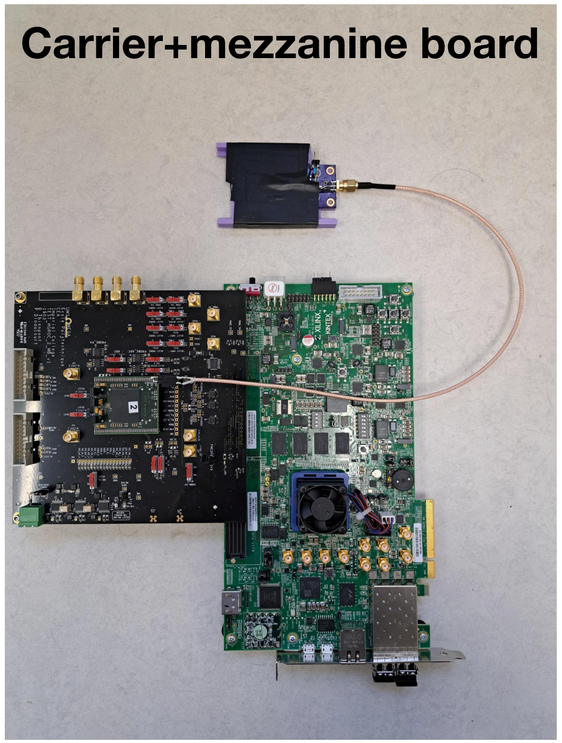
Pre-amp gains can be changed in the ASIC anytime, built-in setup can be further tuned to our needs (EIC)

With the quick test, 16 different gains were explored:

- Dynamic range can change a factor of 3!
- More setups can be added

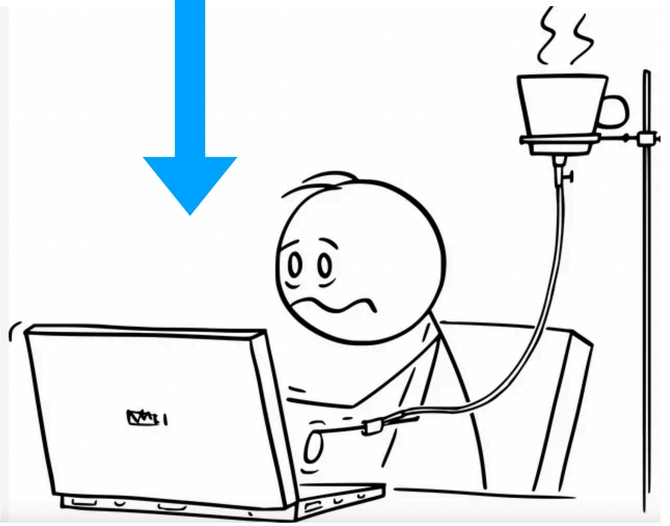
Current readout scheme



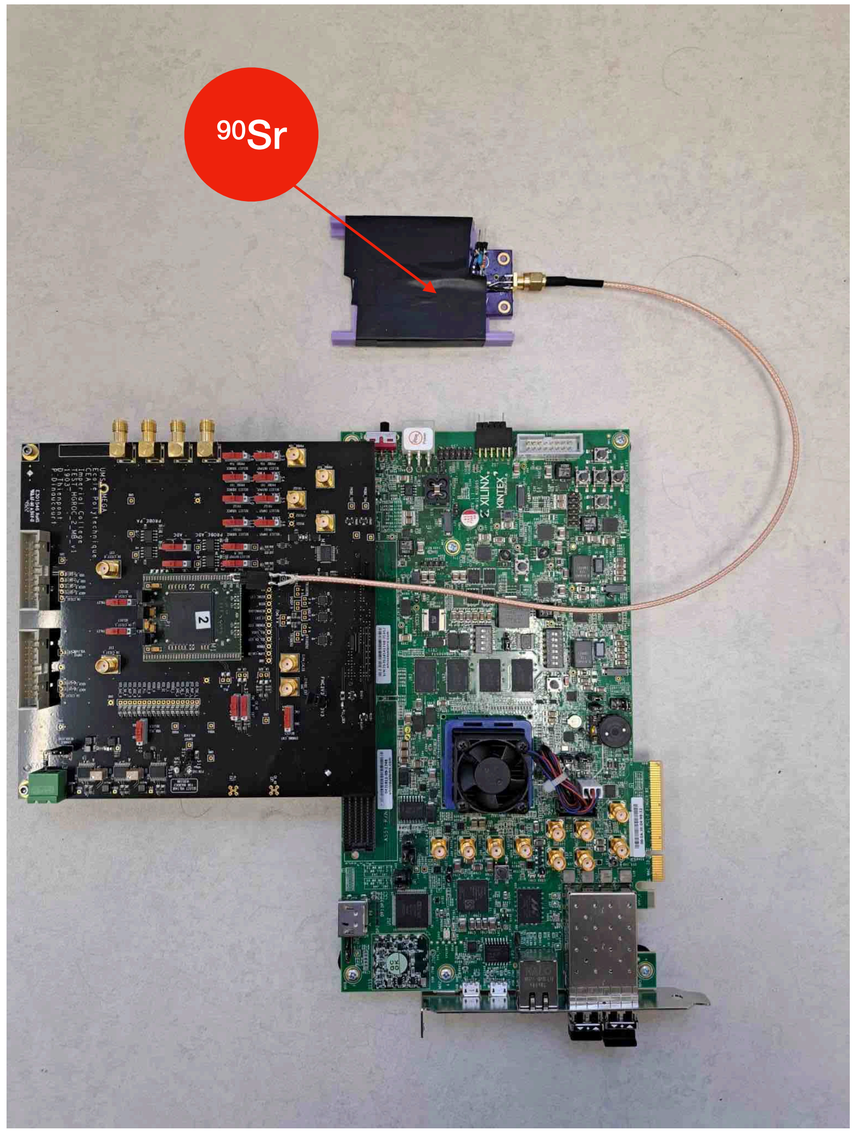


The firmware, software is set:

- Self triggering mode - we can decode the information in KCU and send a trigger signal (for now 1 usec dead-time is set)
- External triggering - any 1.8V signal can be accepted as trigger input

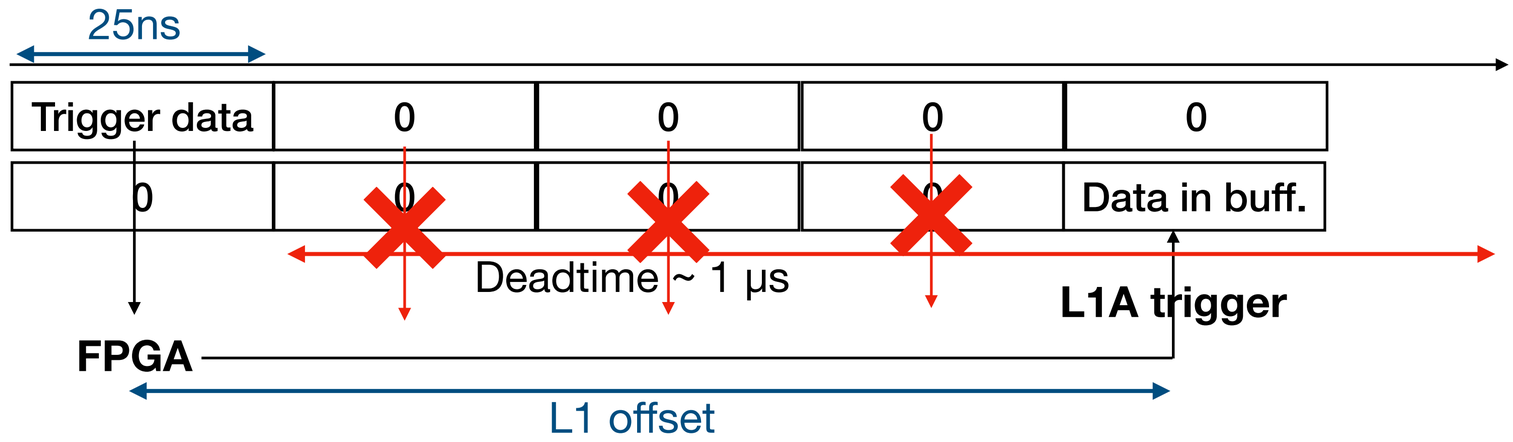


^{90}Sr source test



Self triggering test:

- We put the source directly on the 5x5 cm^2 scintillator
- External triggering is not possible, we utilize the self-triggering mode:
  - First 4 channels are summed up in the trigger line 0
  - Pedestals are loaded to the I2C of the chip
  - Compare the outgoing trigger data to a threshold:
    - If threshold is reached—> send the L1A trigger
    - The L1Offset sets how many clock cycles we wait



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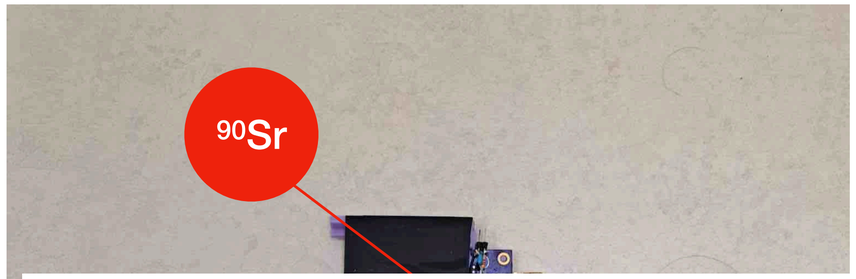

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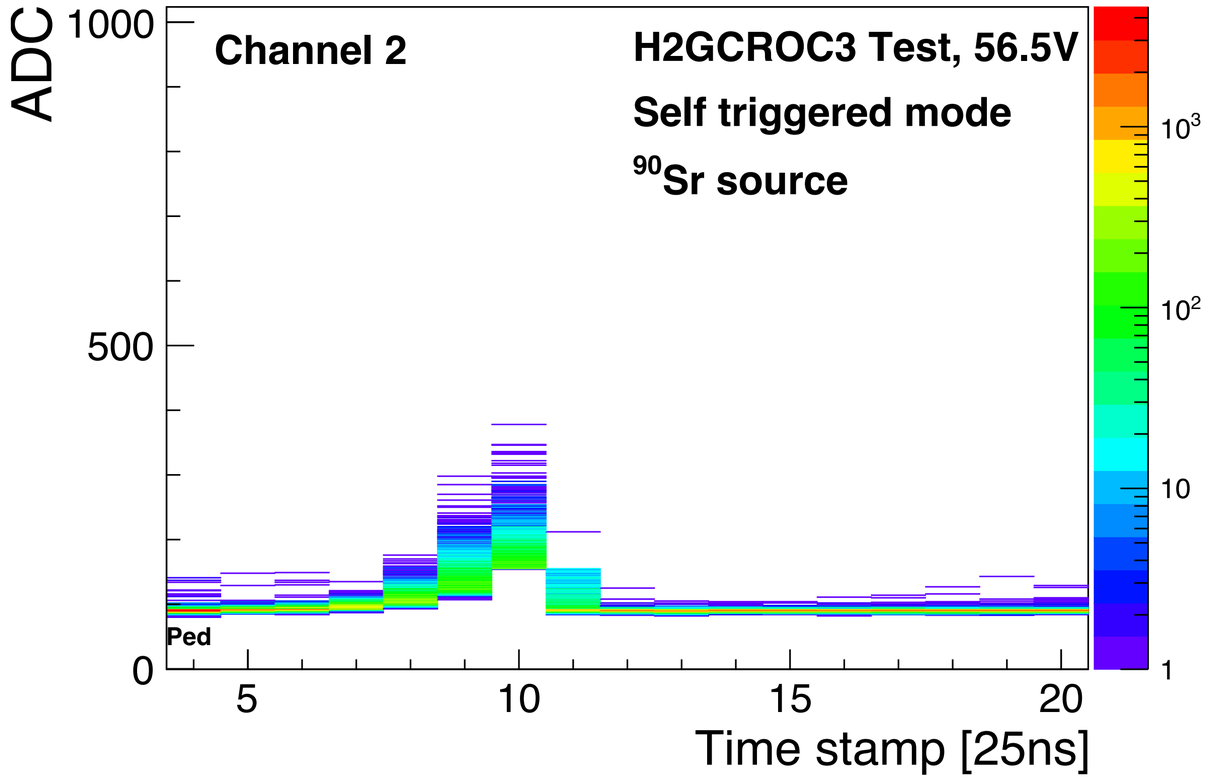
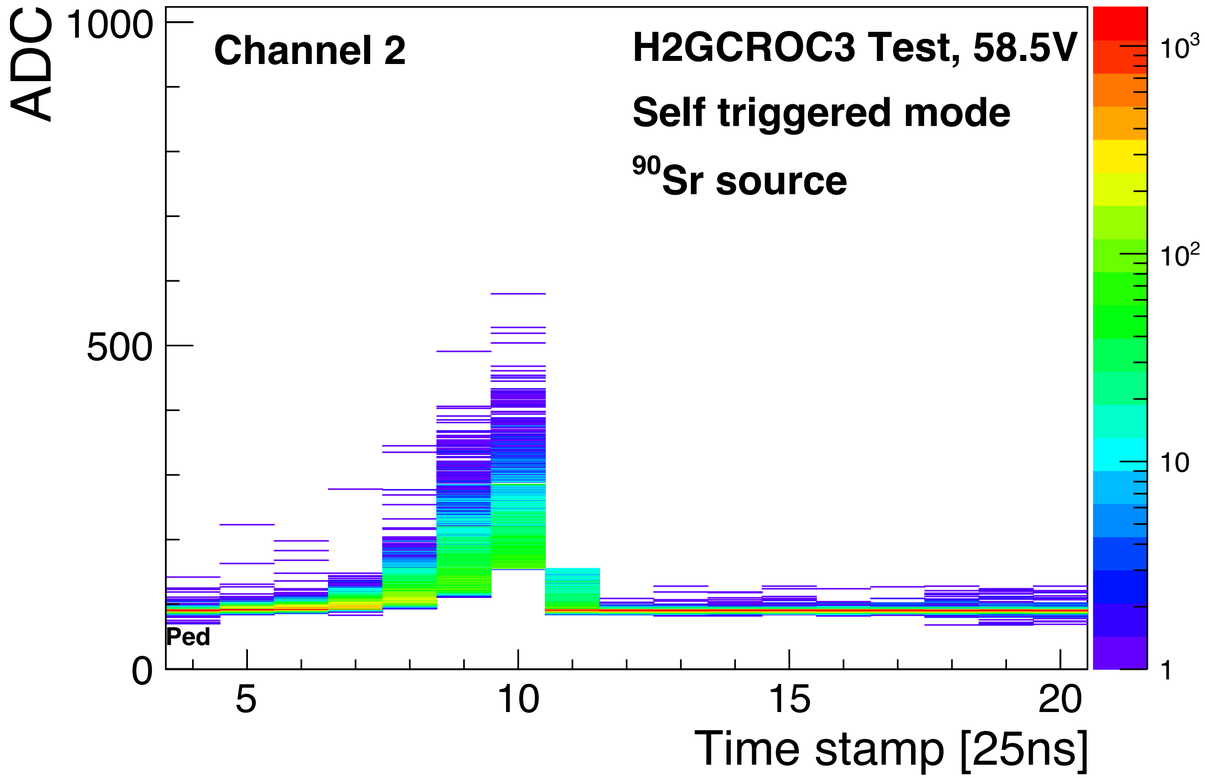
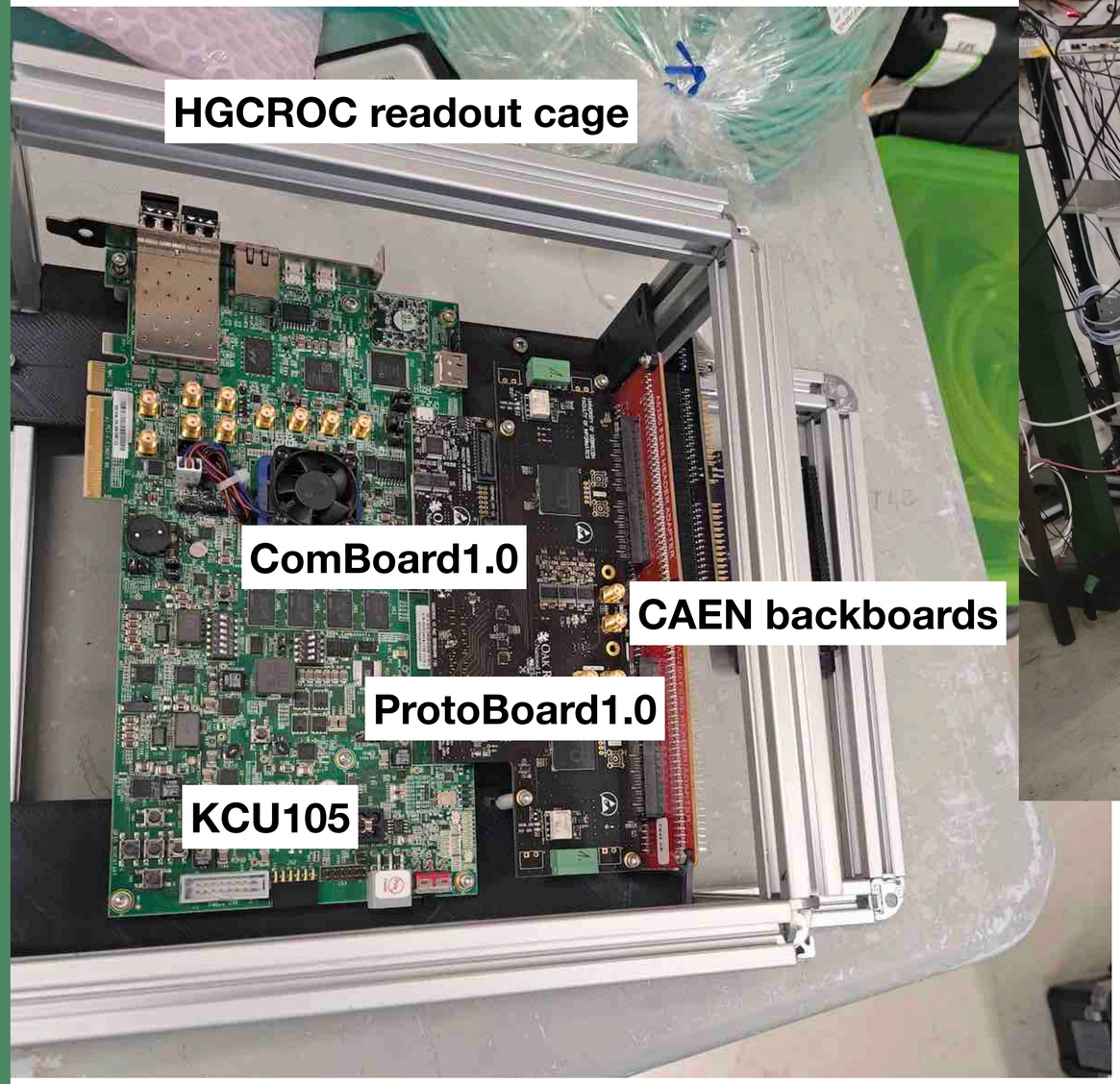
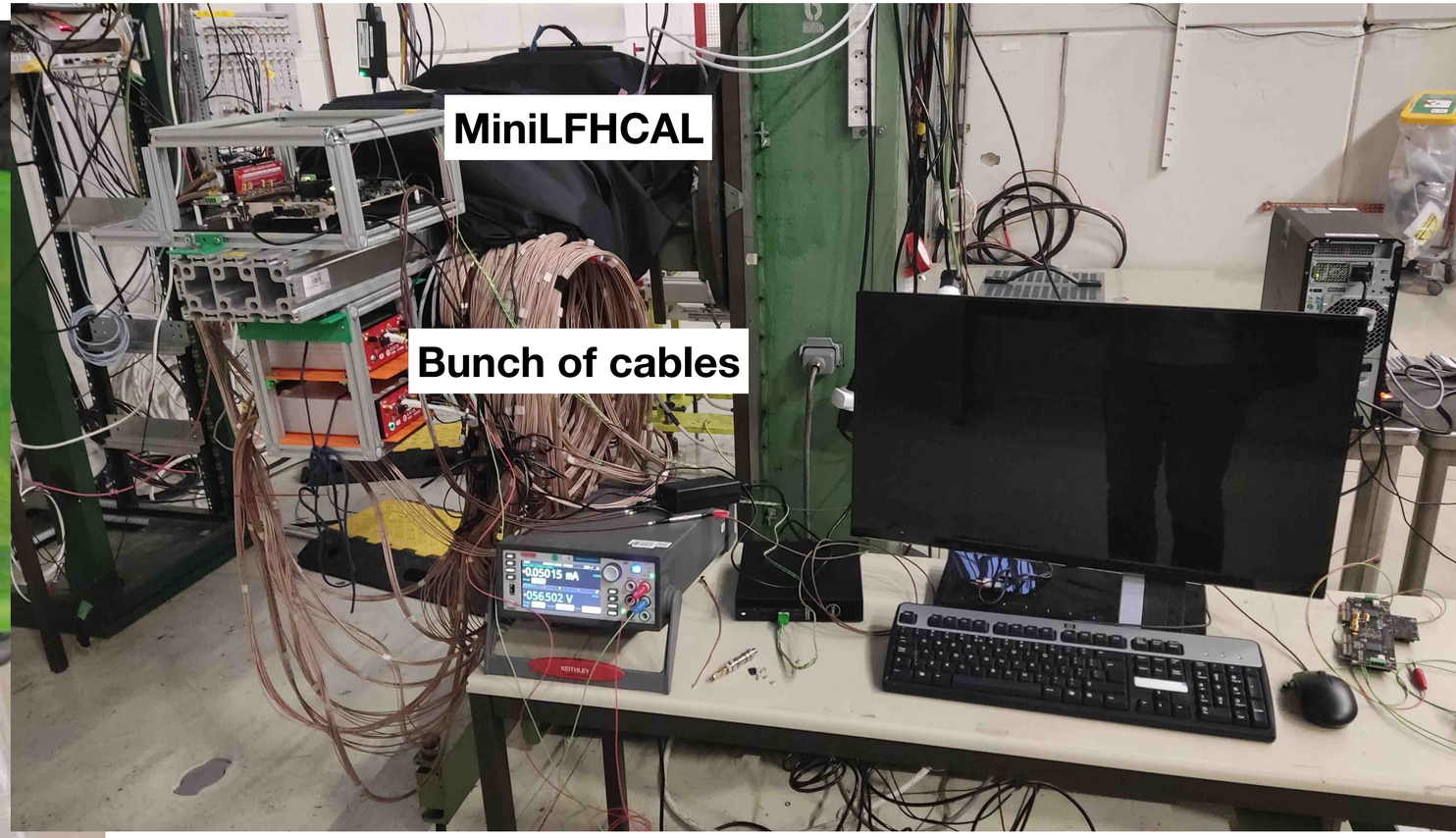




Testbeam setup



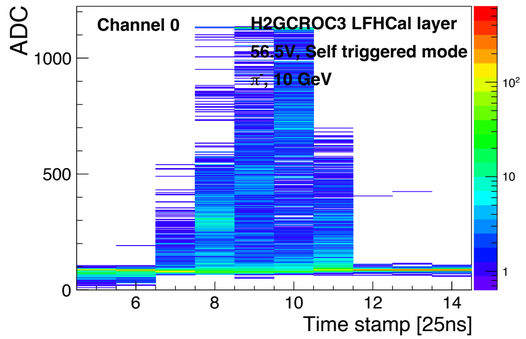


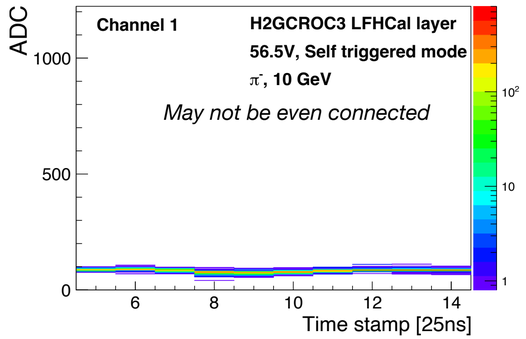
After a lot of debugging and searching for signal, we moved for a testbeam at PS with the MiniLFHCal

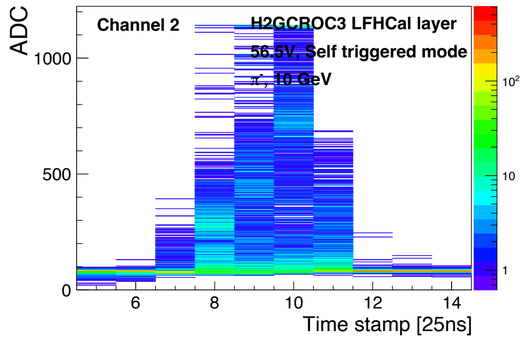
Testbeam results

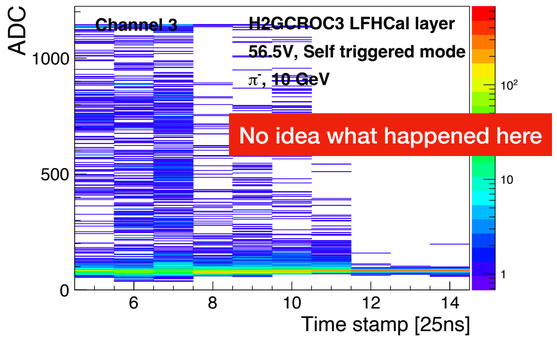
We first tried to see the signal:

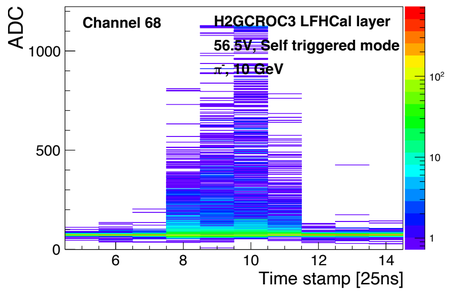
- Self triggering (the sum of first 4 channels for simplicity)
- Vary the L1offset to search for response

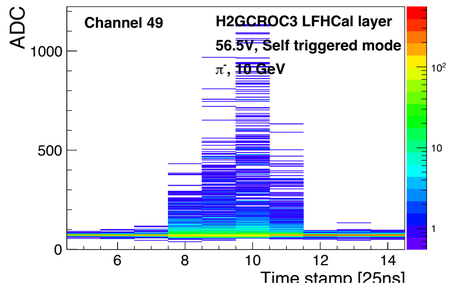


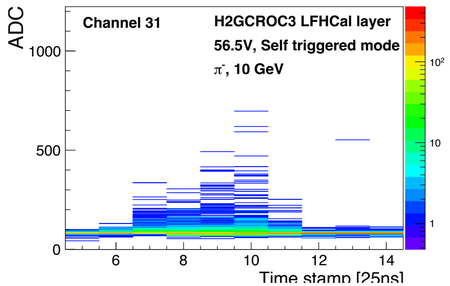


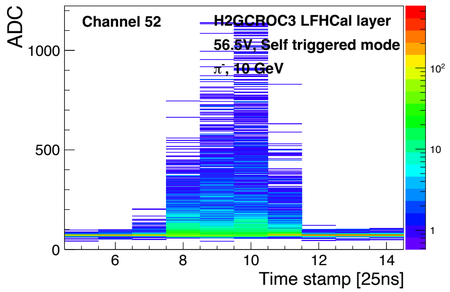


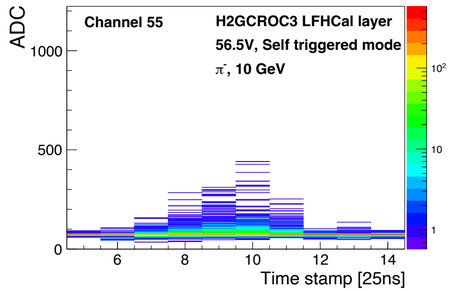


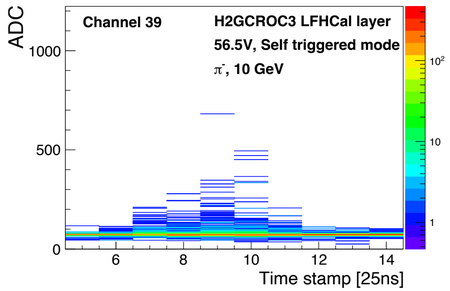








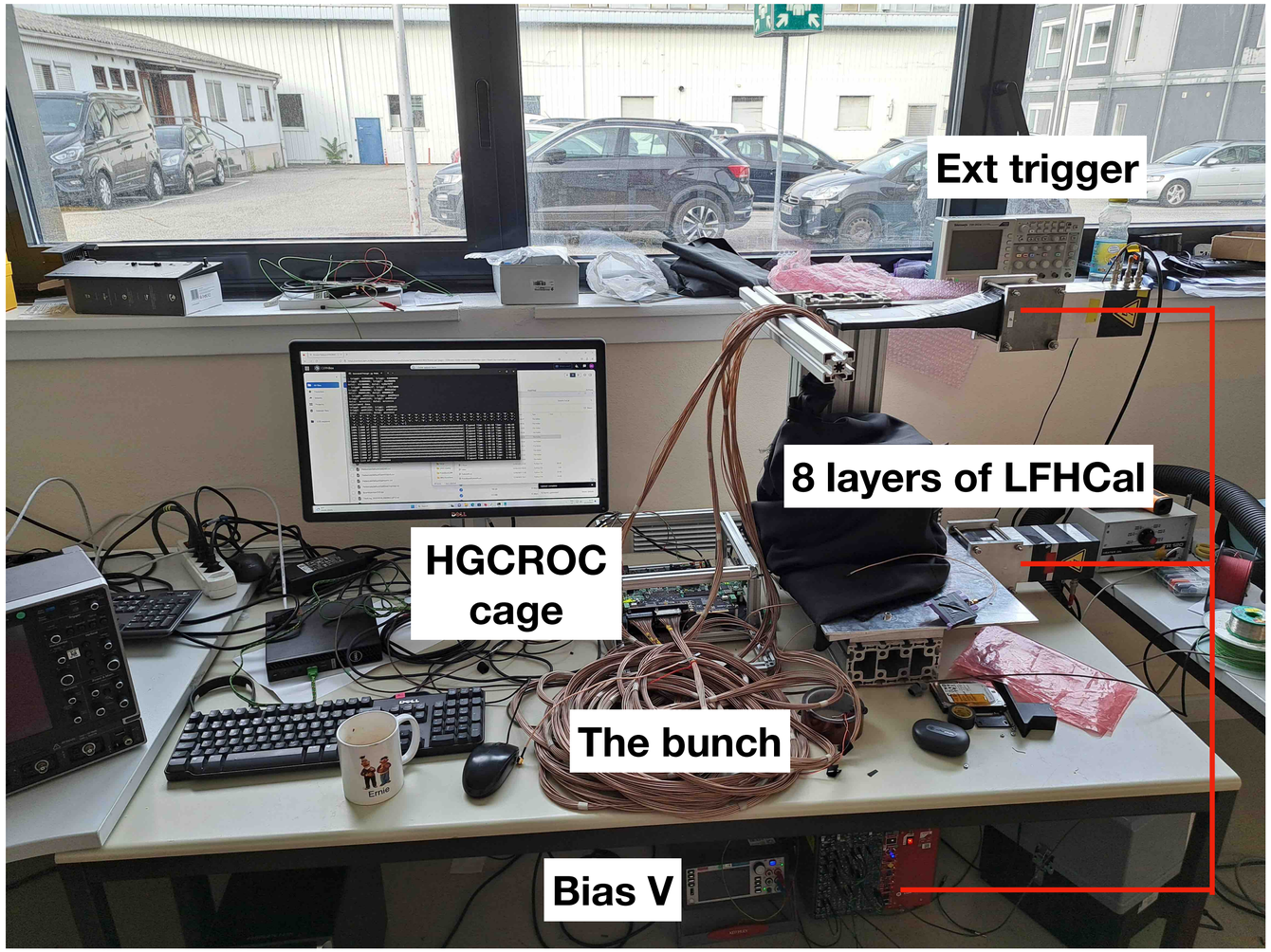




In all 40 channels responded some quite visible, some medium, some small

Unfortunately, then Linac got broken for the night and they could not restore the beam until we had to move out

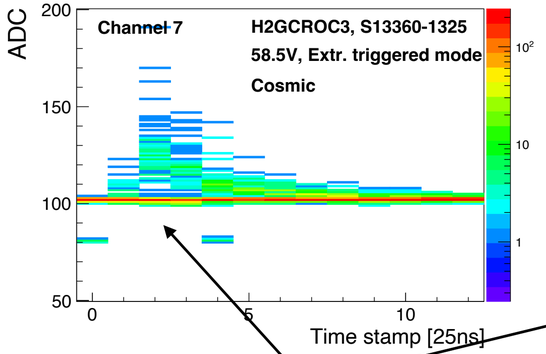
Not yet the end!



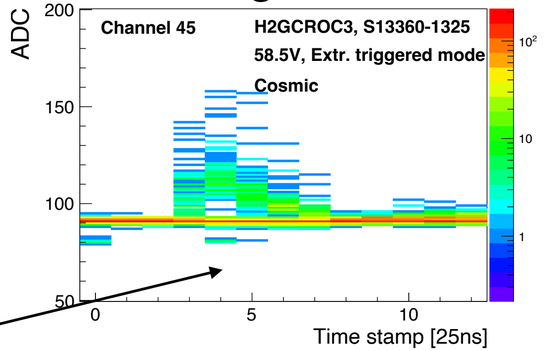
Never-give-up cosmic setup:

- Quickly done after the testbeam setup was removed
- 10x10cm^2 scintillator for external trigger
  - This is different, dropped the self triggering now

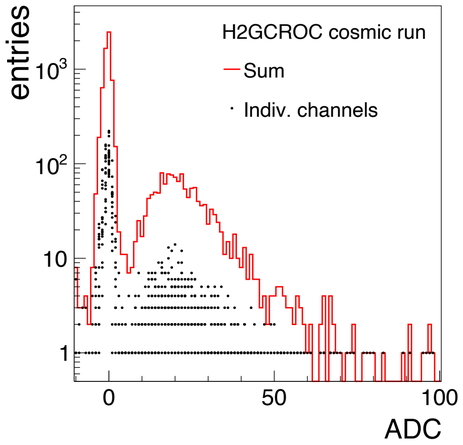
Shorter cable



Longer cable



Check the max for responding channels

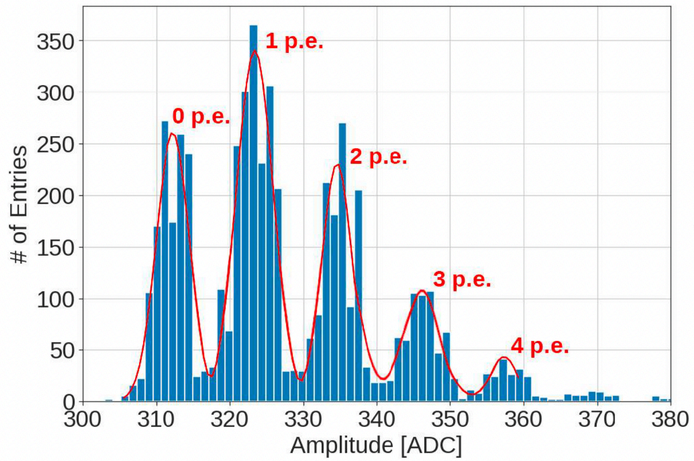


We see the MIP peak from the cosmic runs

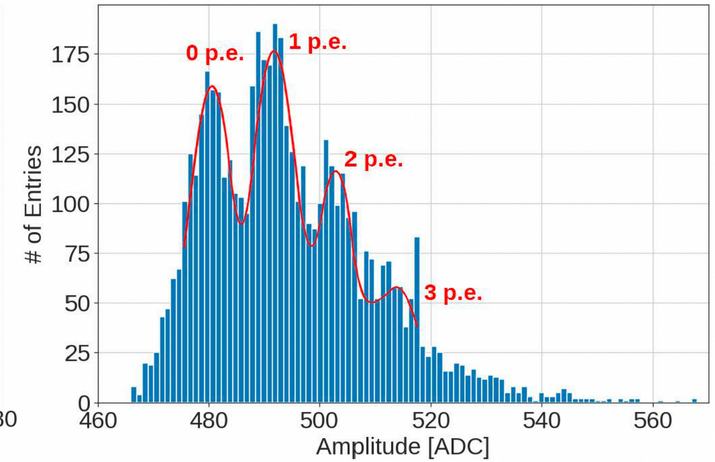
Extra stuff from Omega

Calibration: Single-photon-spectrum

- **2mm²:**



- **9mm²:**

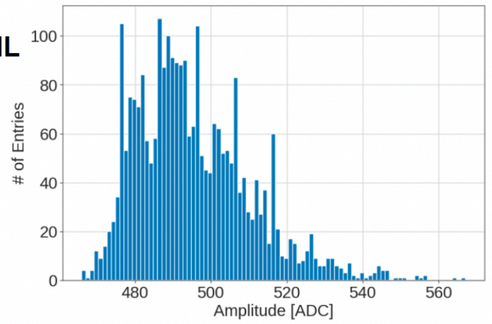


***Extra step for 9mm² SiPM calibration:**

The large C_{det} of the 9mm² SiPM produce an increment of DNL and make it harder to see the photon separation.

The DNL can be mitigated taking data with different pedestal levels using the ASIC to move the pedestals (*Trim_inv* parameter). SPS is clearer after aligning the data.

Without DNL correction:



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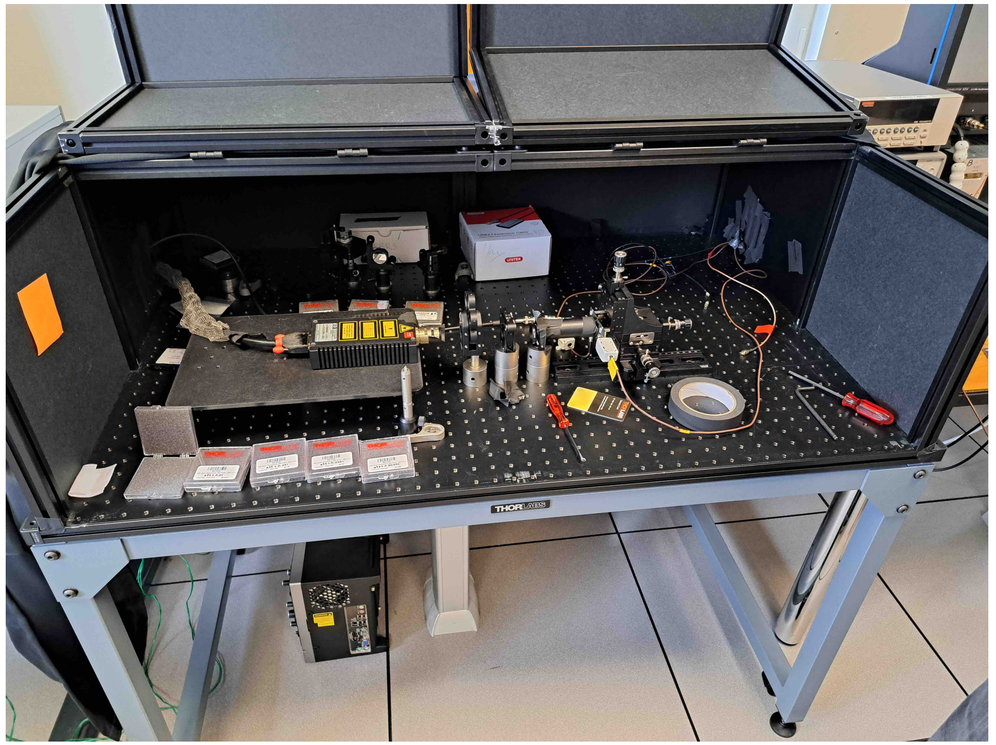
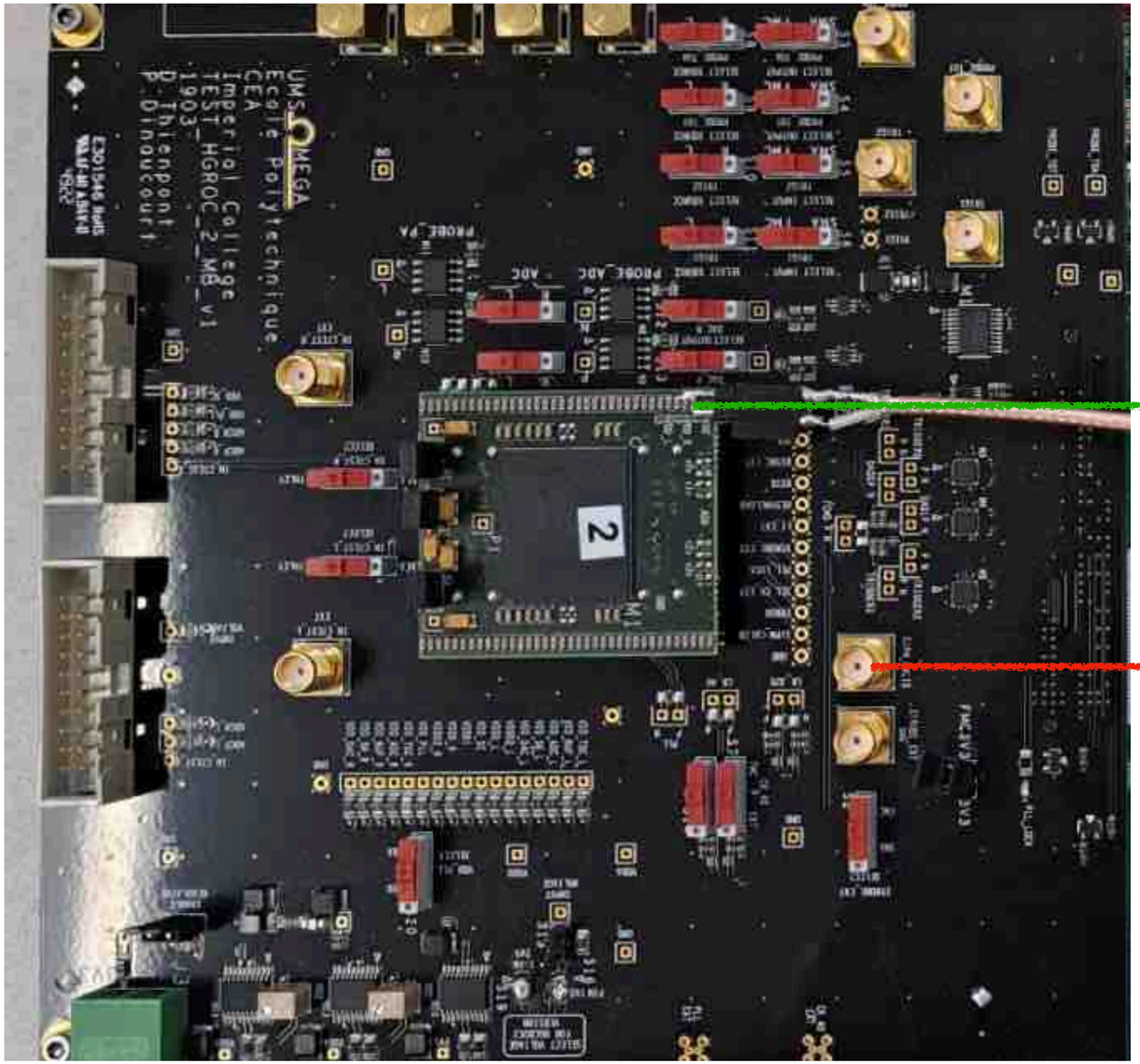
*Thanks to **Jose Gonzales** et al*

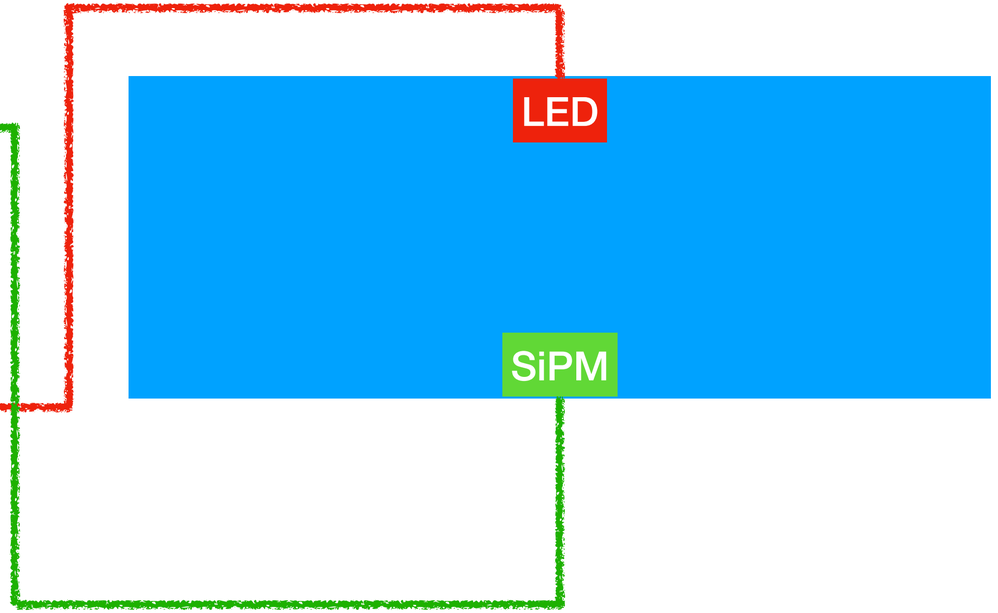


Some single photon spectra using the H2GCROC from the Omega test setup

- Small SiPM is clearly visible
- Larger ones are getting less visible (larger capacitance)
- They will also check the 36 mm² SiPM

Calibration Circuit Plan





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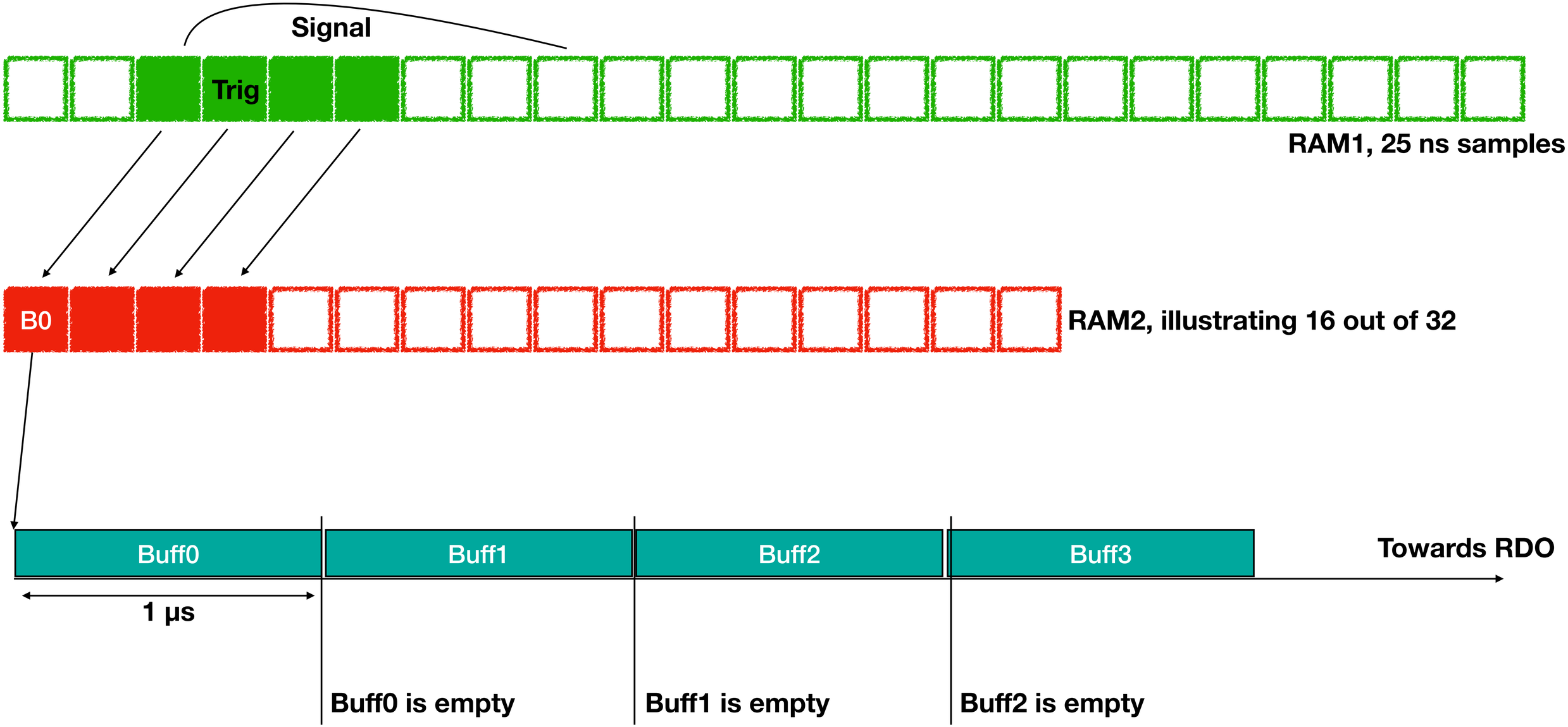
Backup

Illustration



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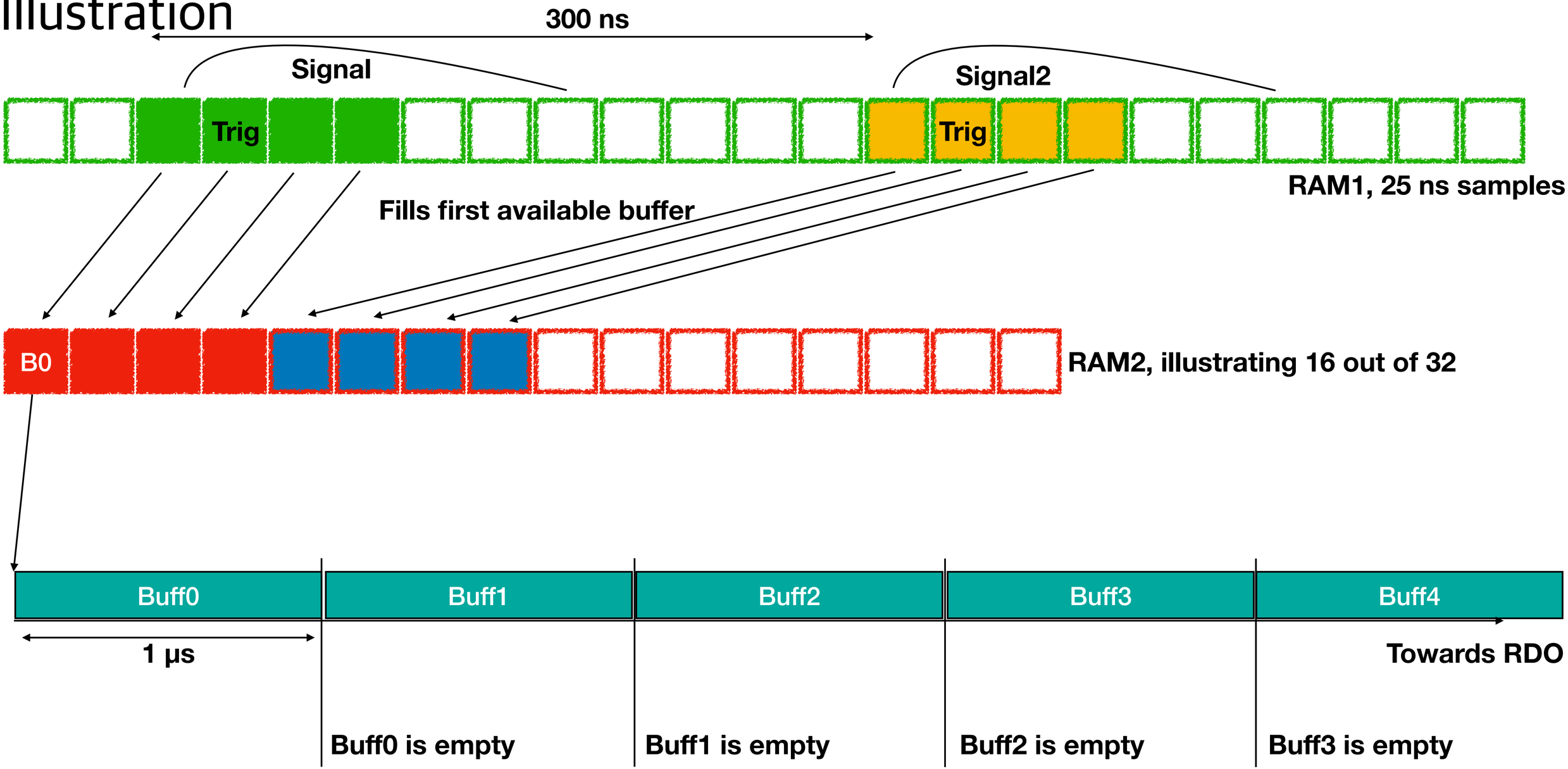

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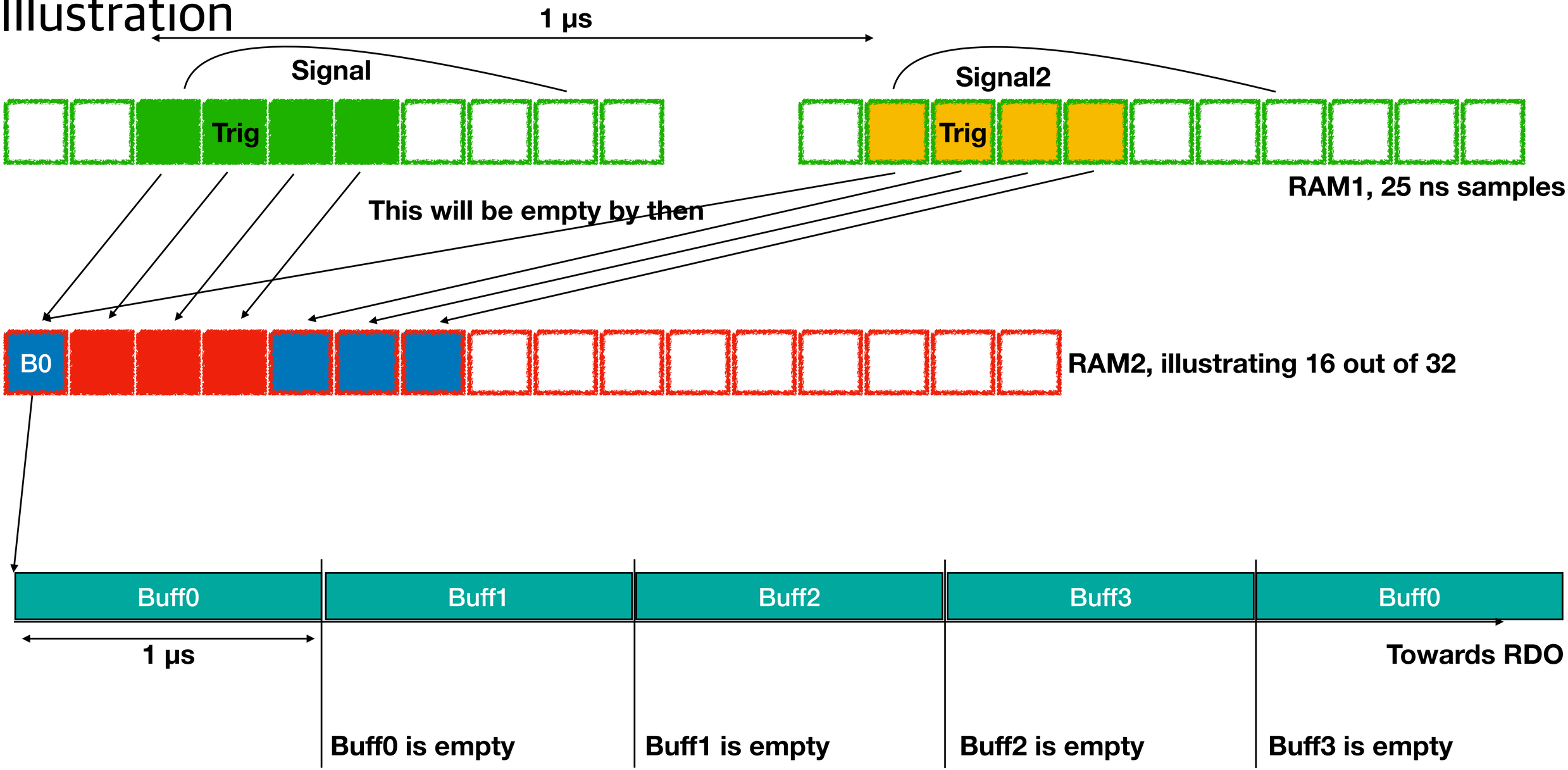
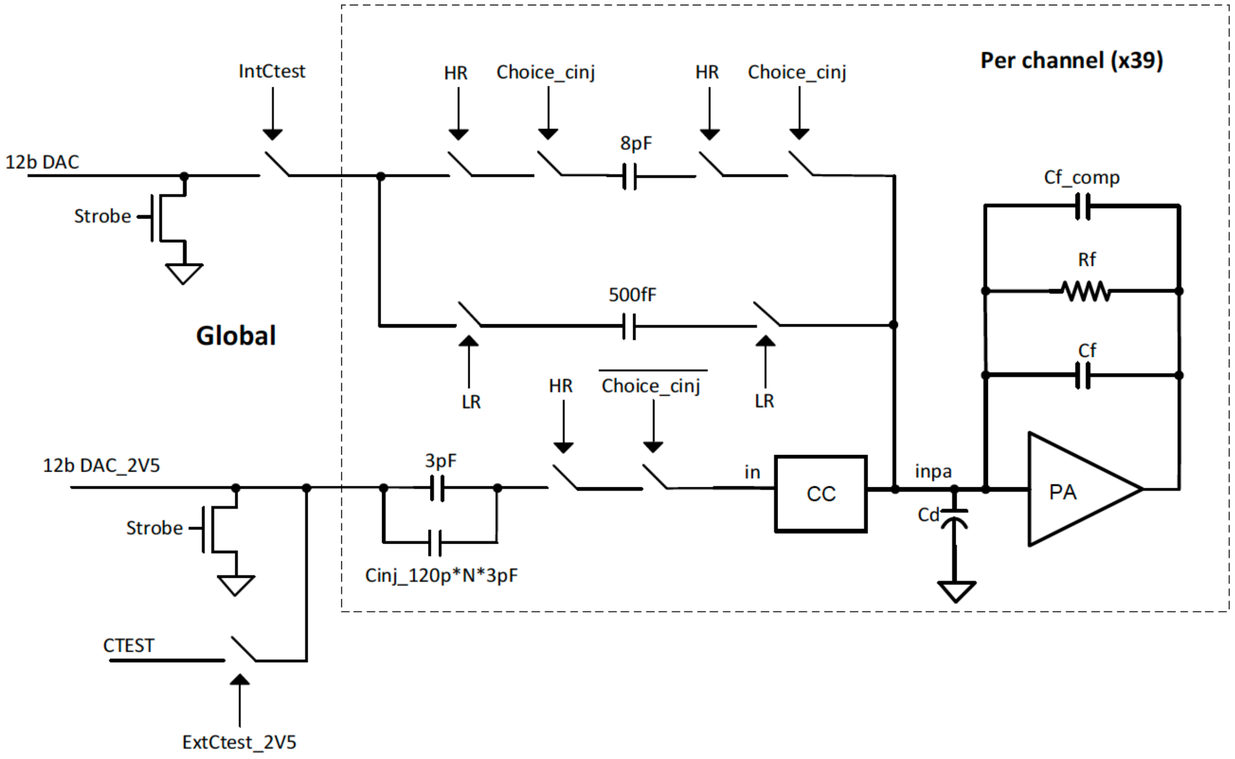
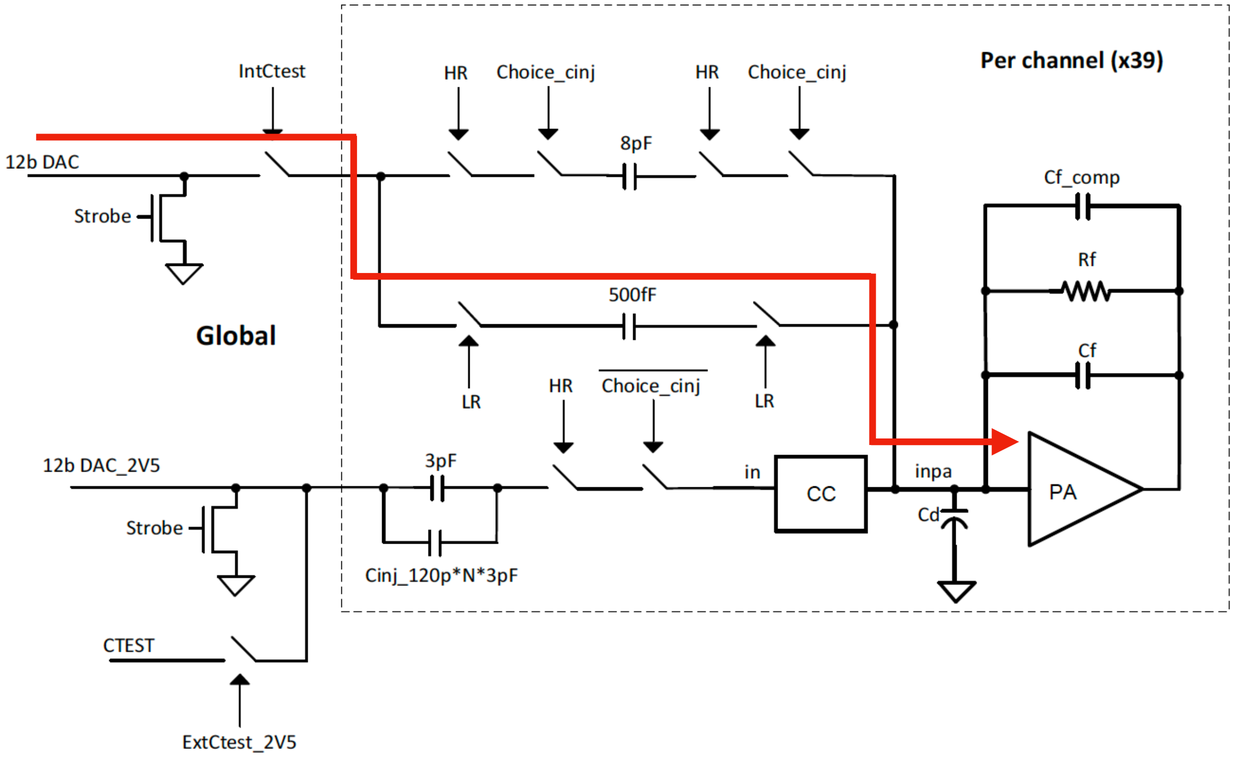


Internal injection circuit



Three different internal injection path:
(There is no need to connect any channels, all is inside the chip):
All of them have a 12-bit range as input value, can be setup via I2C

Internal injection circuit

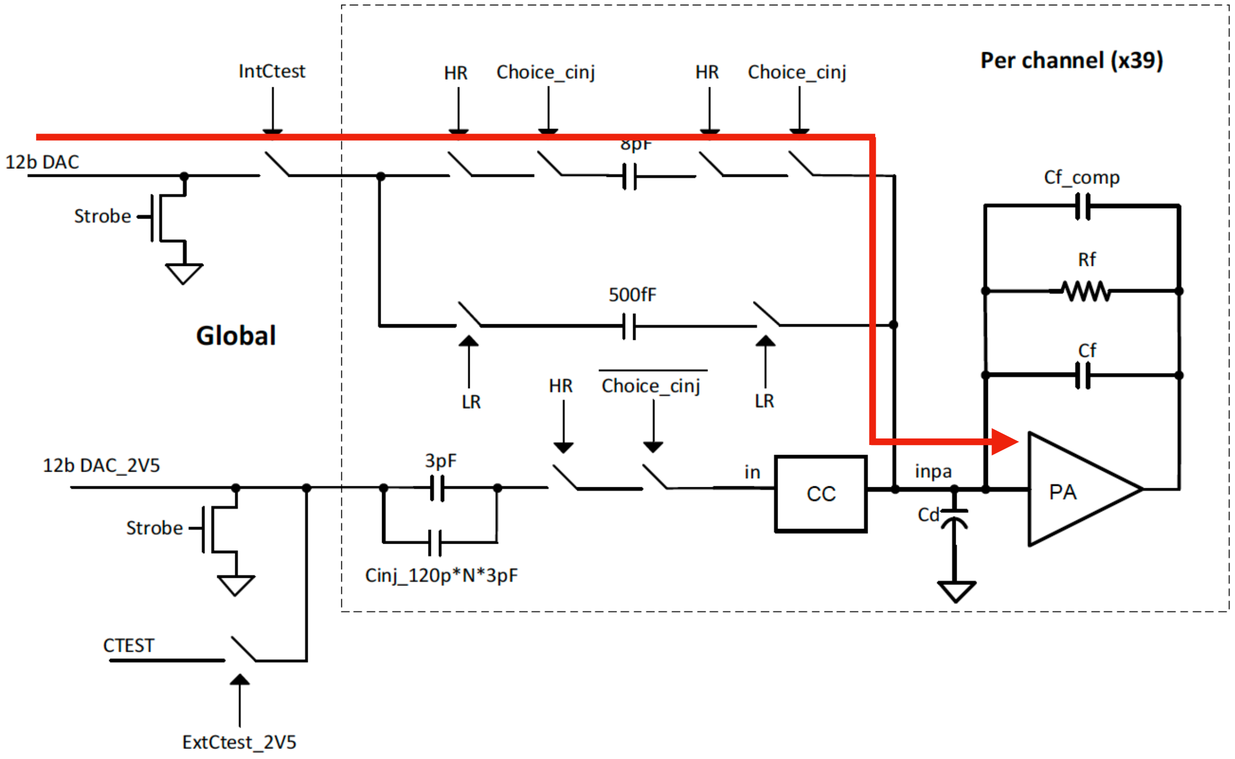


Three different internal injection path:
(There is no need to connect any channels, all is inside the chip):
All of them have a 12-bit range as input value, can be setup via I2C

Low injection path:

- Goes through the 500fF capacitor, directly to the pre-amp
- Circumvents the current conveyor
- Testing mostly the ADC range in small steps
- TOA threshold setup

Internal injection circuit

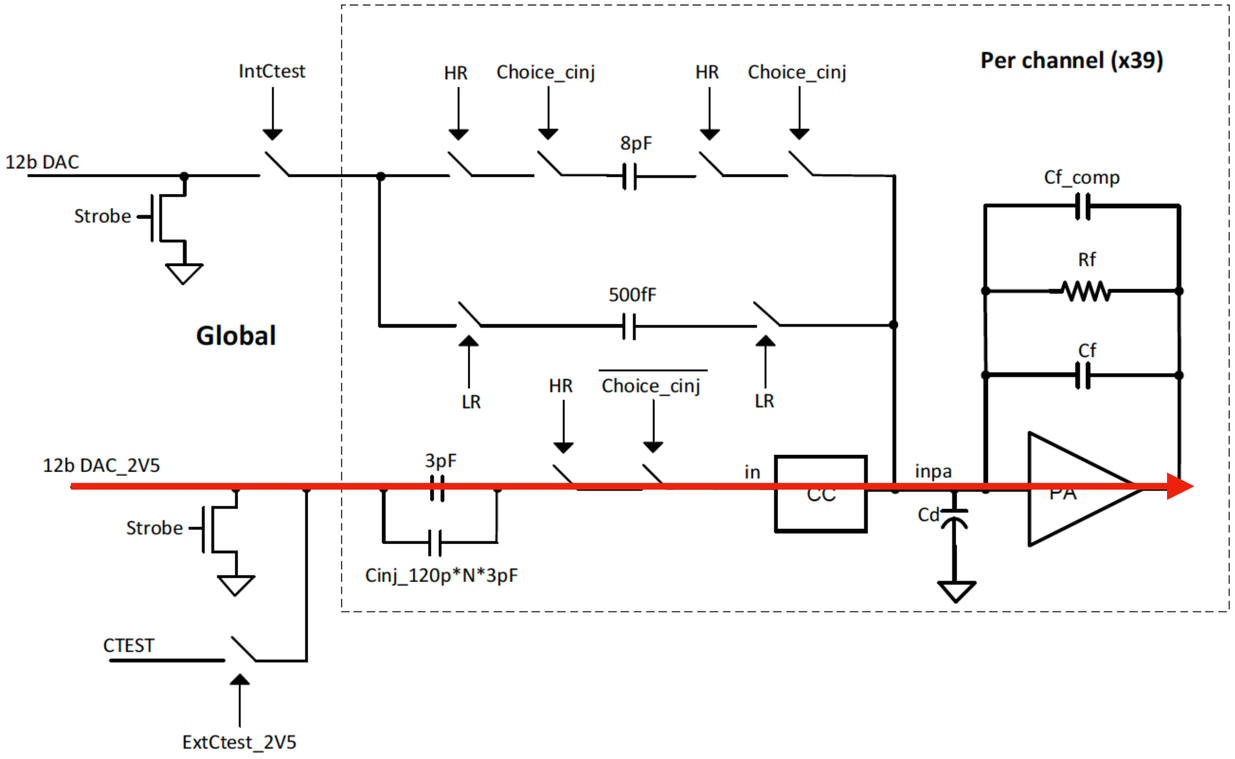


Three different internal injection path:
(There is no need to connect any channels, all is inside the chip):
All of them have a 12-bit range as input value, can be setup via I2C

High injection path:

- Goes through the 8pF capacitor, directly to the pre-amp
- Circumvents the current conveyor
- Testing mostly the TOT threshold
- Linearity on entire dynamic range

Internal injection circuit



Three different internal injection path:
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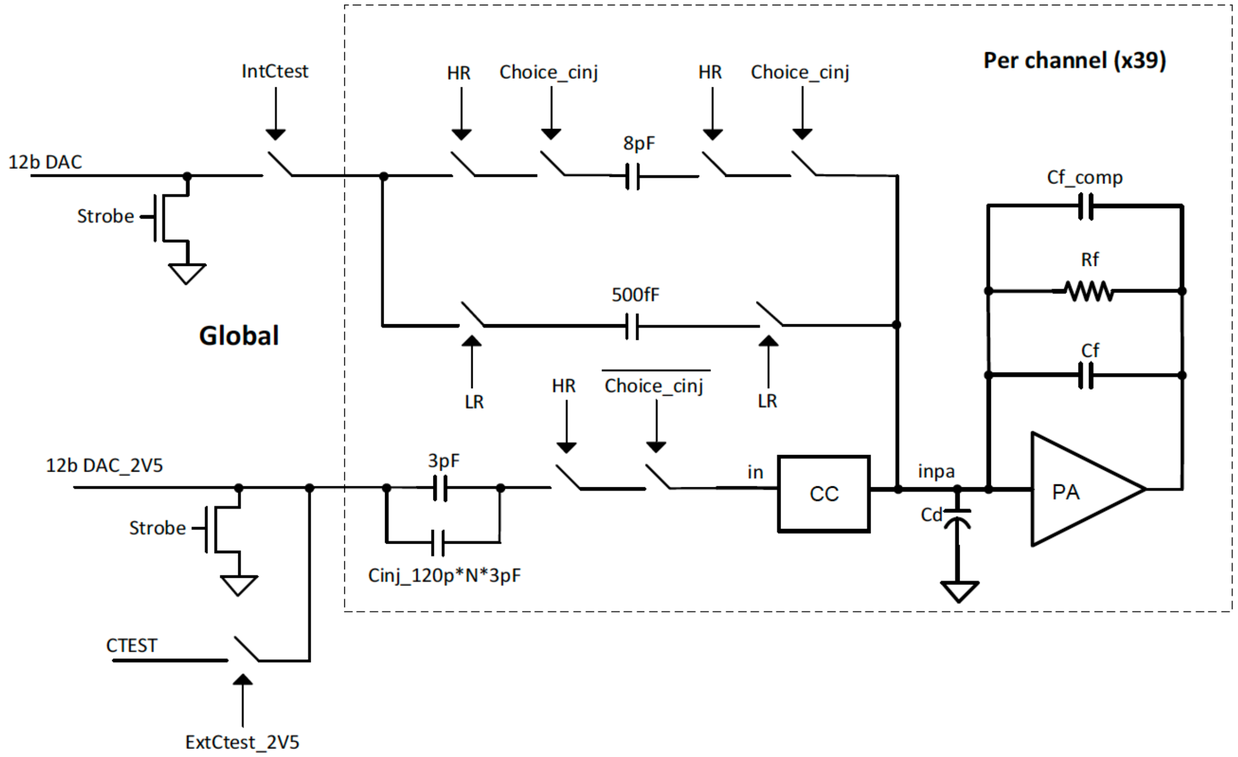
All of them have a 12-bit range as input value, can be setup via I2C

2V5 injection

- Same as an external signal (mimics the SiPM input)
- Setup the current conveyor attenuation of the signal

Internal injection circuit



The following tables show how to select the different configurations for internal/external calibration:

	DAC LR	DAC HR	CINJ 3pF	CINJ 3pF*N	CTEST 3pF	CTEST 3pF*N
HighRange	0	1	1	1	0	0
LowRange	1	0	0	0	0	0
Choice_cinj	X	1	0	0	0	0
Cinj_120p	0	0	0	1	0	1
IntCtest	1	1	0	0	0	0
ExtCtest_2V5	0	0	0	0	1	1
Calib INPA	0 - 500fC	0 - 8pC	-	-	-	-
Calib IN	-	-	0 – 3pC	0 – 3pC*N	-	-
Calib Ext Inj	-	-	-	-	CTEST * (0 – 3pC)	CTEST * (0 – 3pC*N)

This is the map of I2C registers to set each injection path

Three different internal injection path:
(There is no need to connect any channels, all is inside the chip):
All of them have a 12-bit range as input value, can be setup via I2C

Low injection path:
- Goes through the 500fF capacitor, directly to the pre-amp
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- TOA threshold setup

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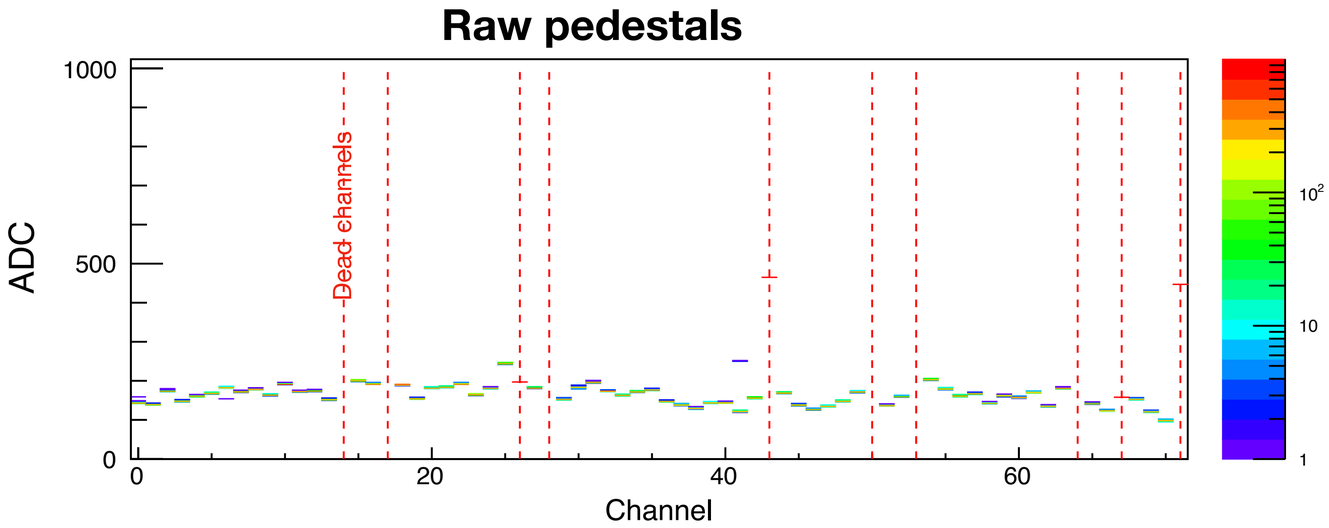
- Linearity on entire dynamic range

2V5 injection
- Same as an external signal (mimics the SiPM input)
- Setup the current conveyor attenuation of the signal

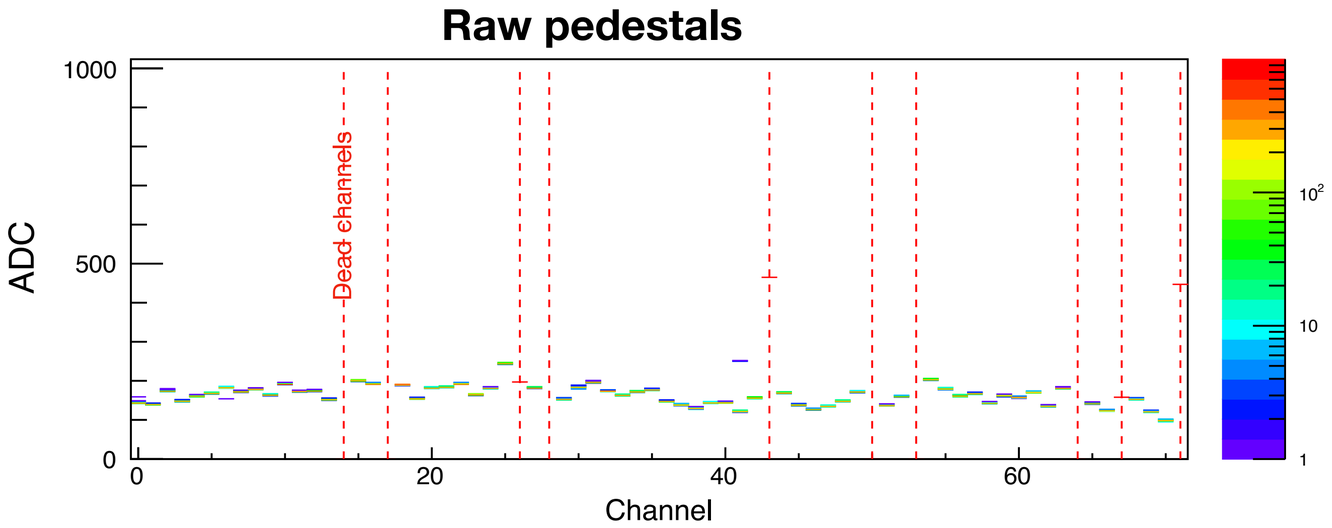
First test, pedestals



Pedestals as we turn-on the chip:

- This is a CMS leftover chip, so it had 10 dead channels
- This is also a H2GCROC3A chip

First test, pedestals

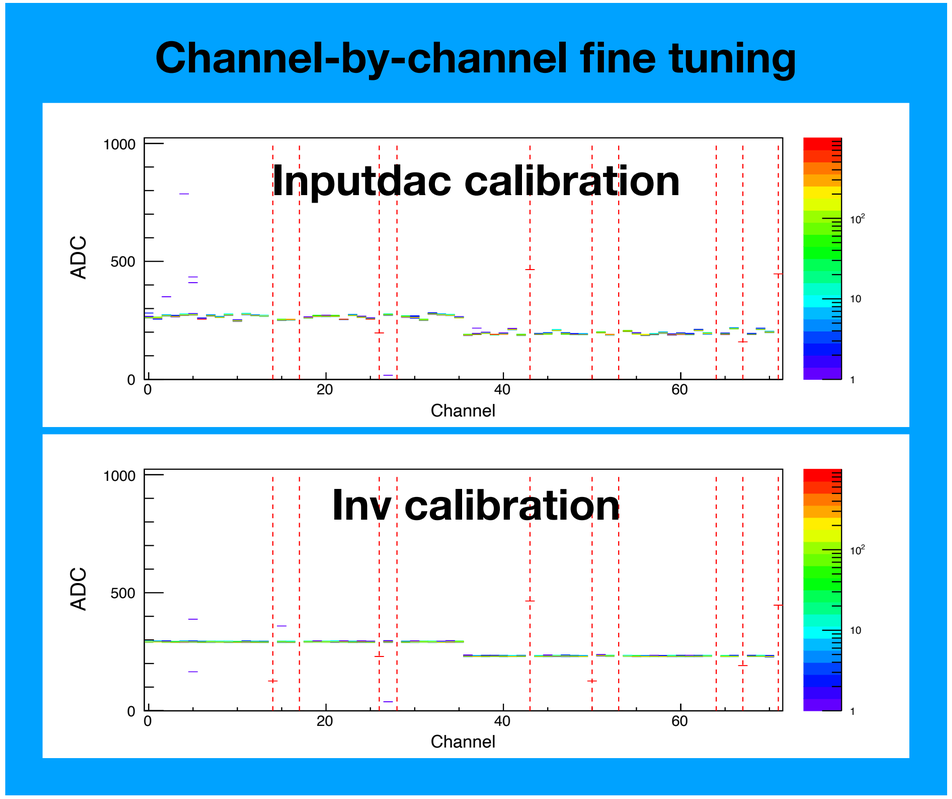


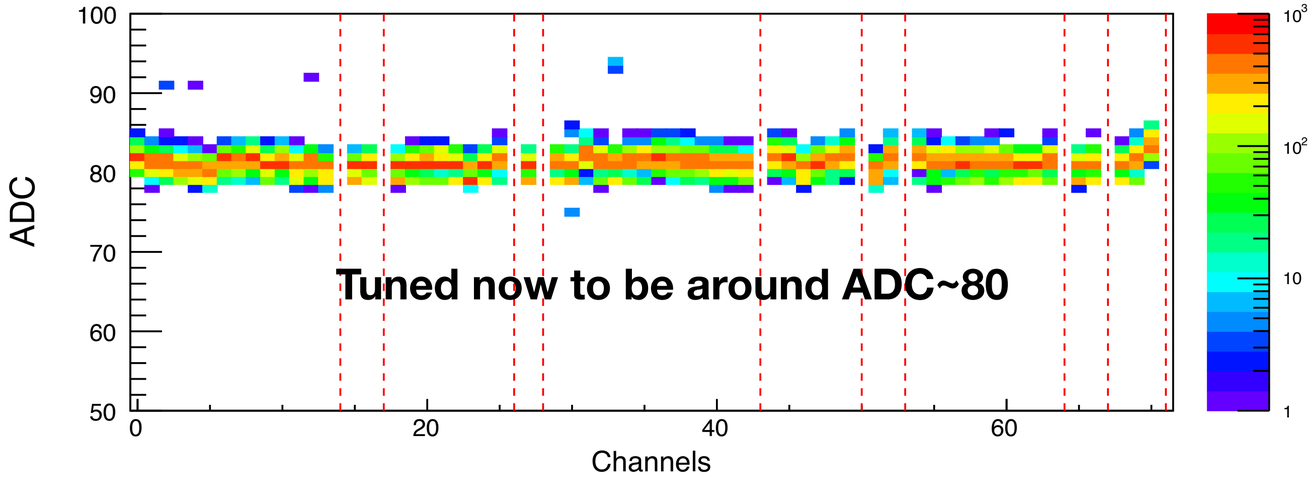
Pedestals as we turn-on the chip:

- This is a CMS leftover chip, so it had 10 dead channels
- This is also a H2GCROC3A chip

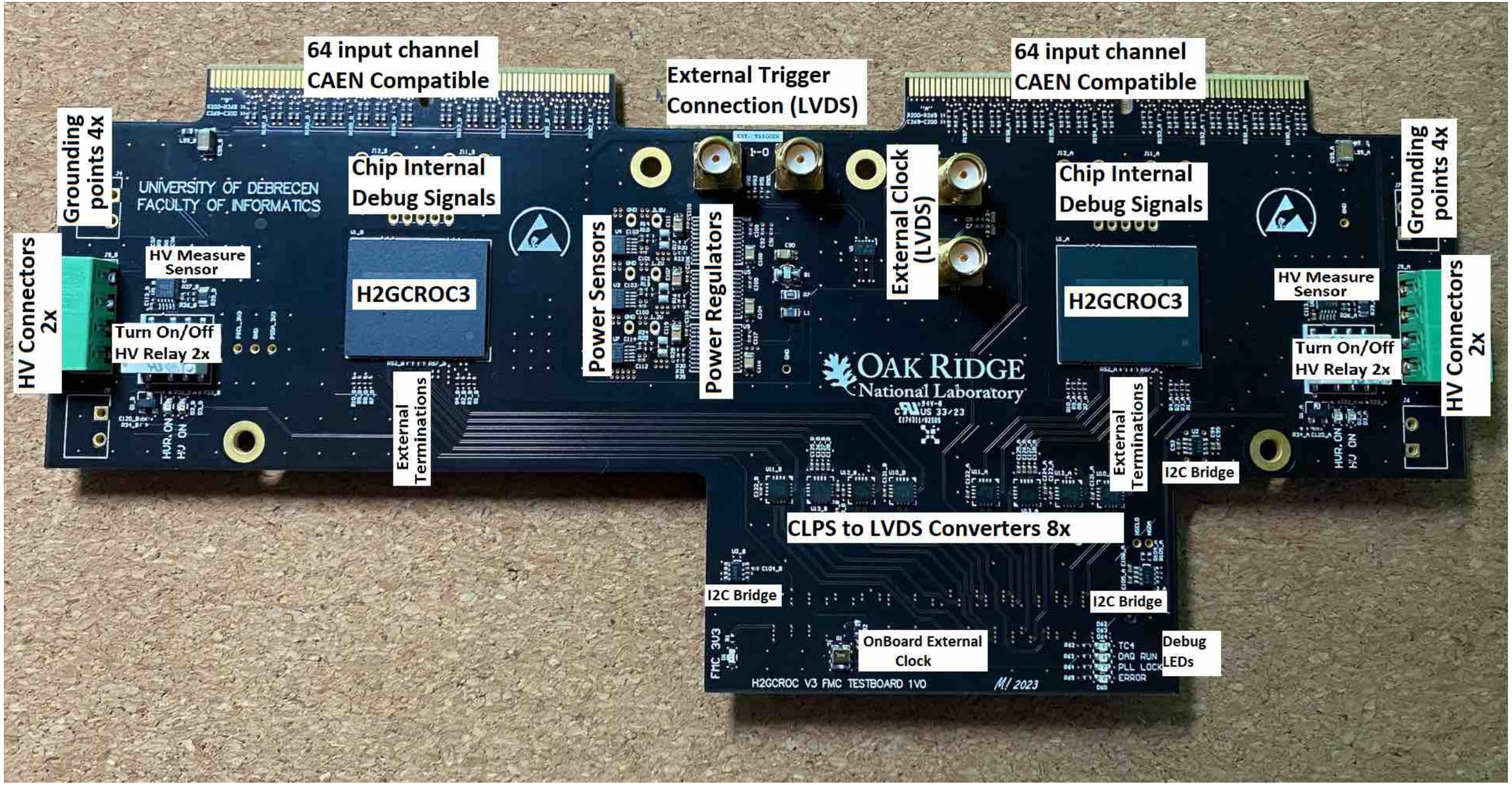
Pedestals after calibration:

- Channel-by-channel calibration is done:
  - Register_0 inputdac
  - Register_3 trim_inv
- We can set the global pedestals by half-chip:
  - Register_4 Inv_vref
  - Register_5 Noinv_vref

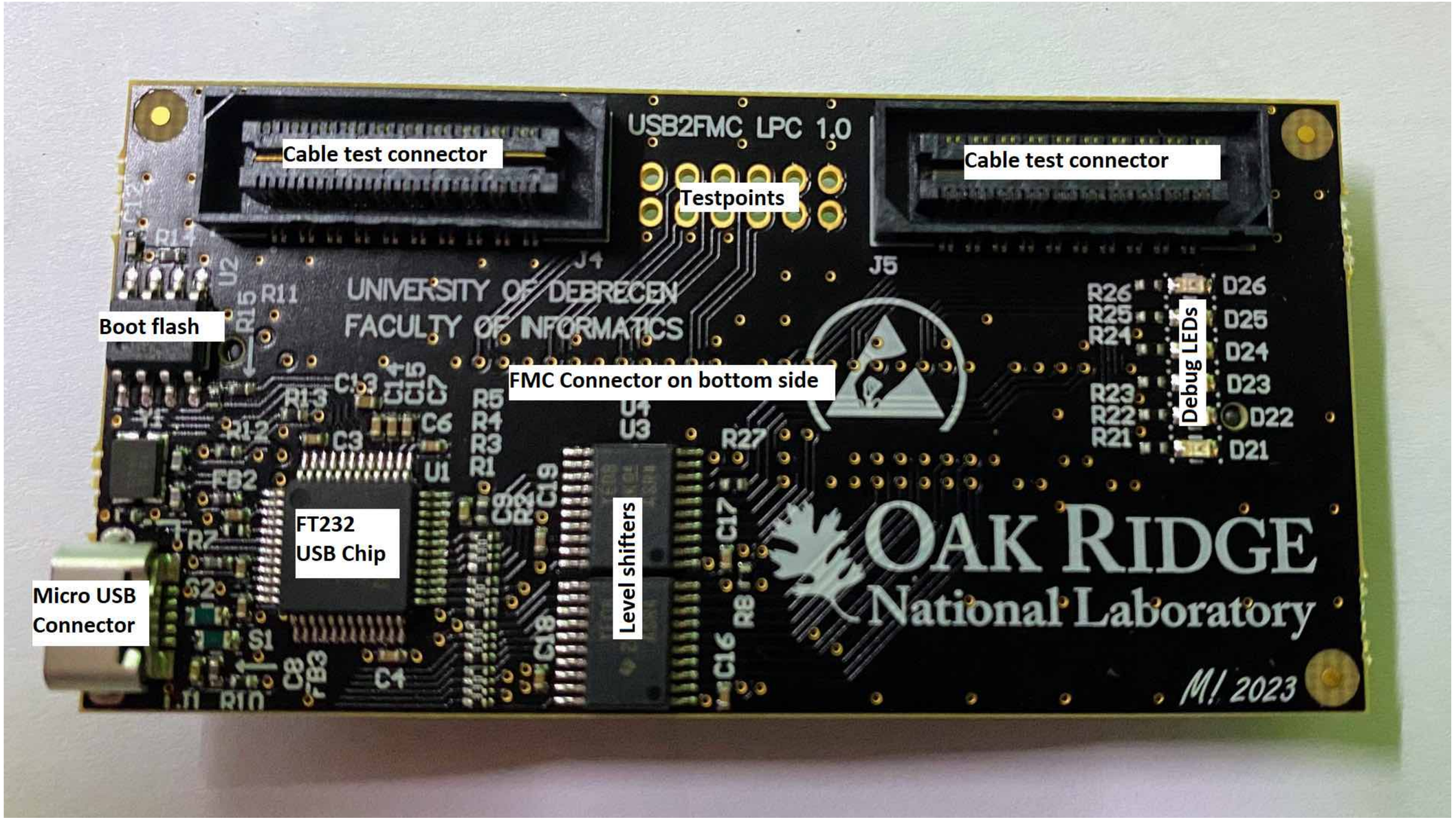




ProtoBoard1.0 (we have 2 of these)



ComBoard1.0 (we have 5 of these)



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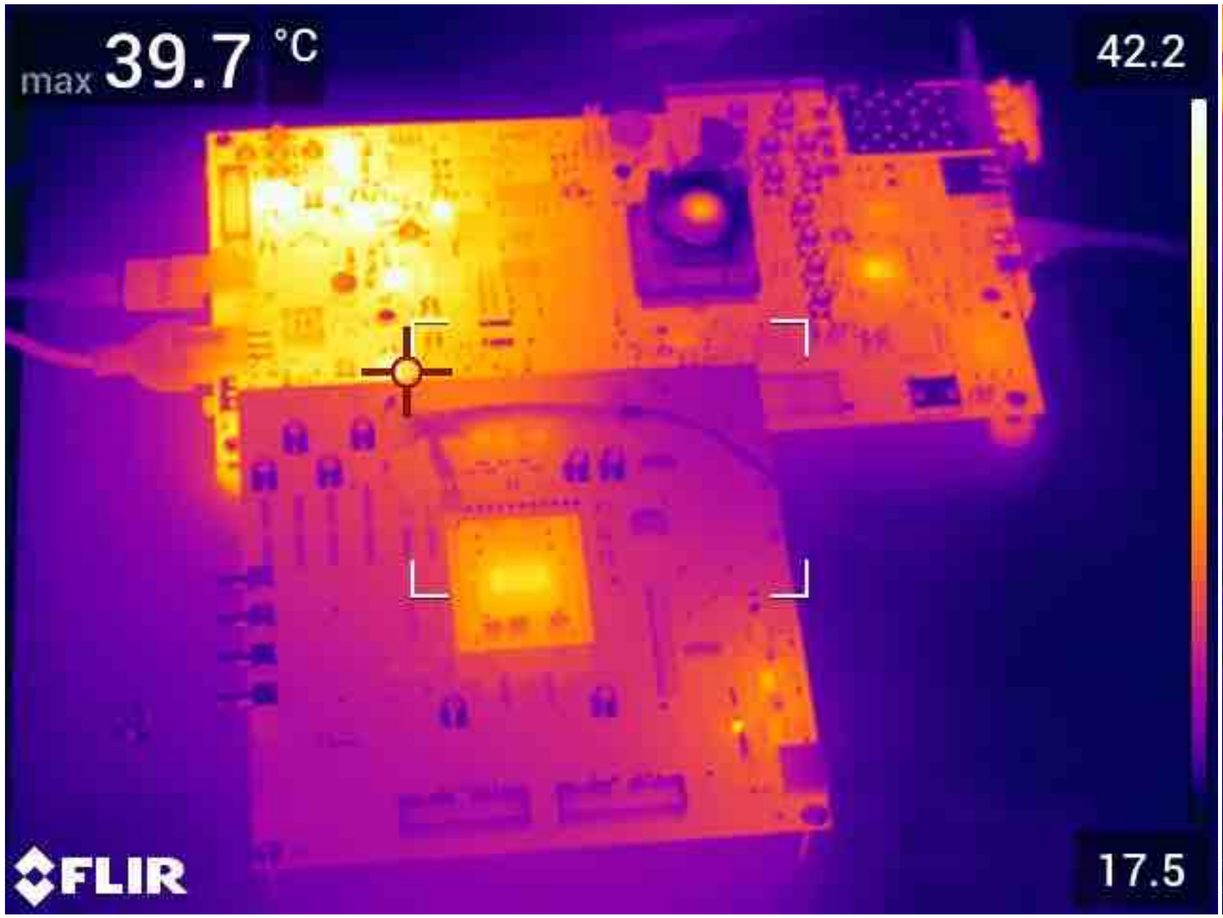
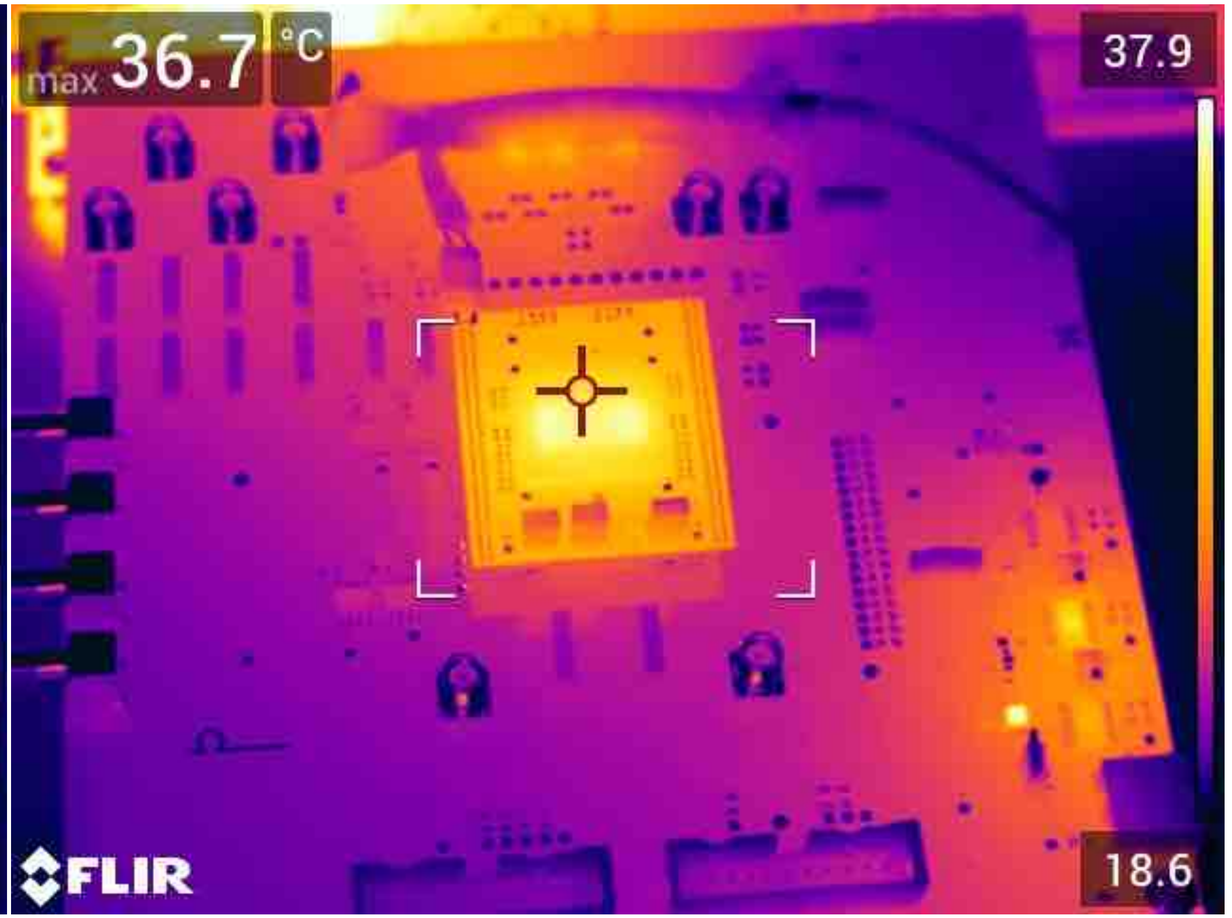
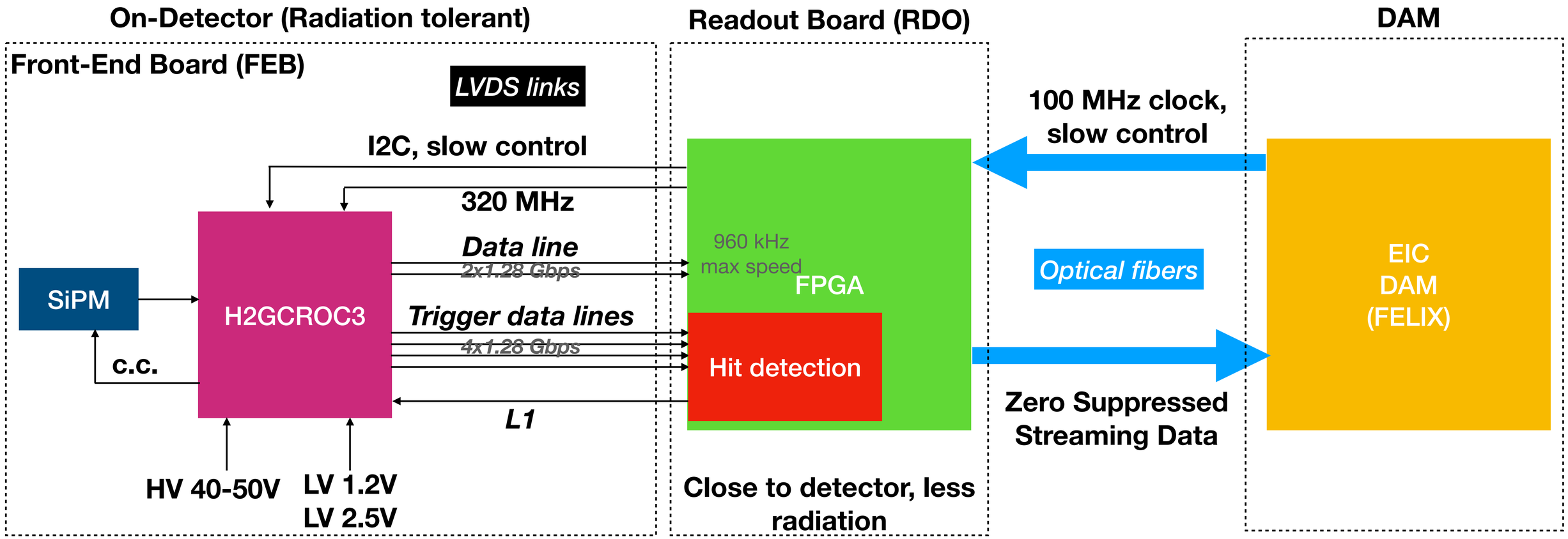
Some IR pictures while working





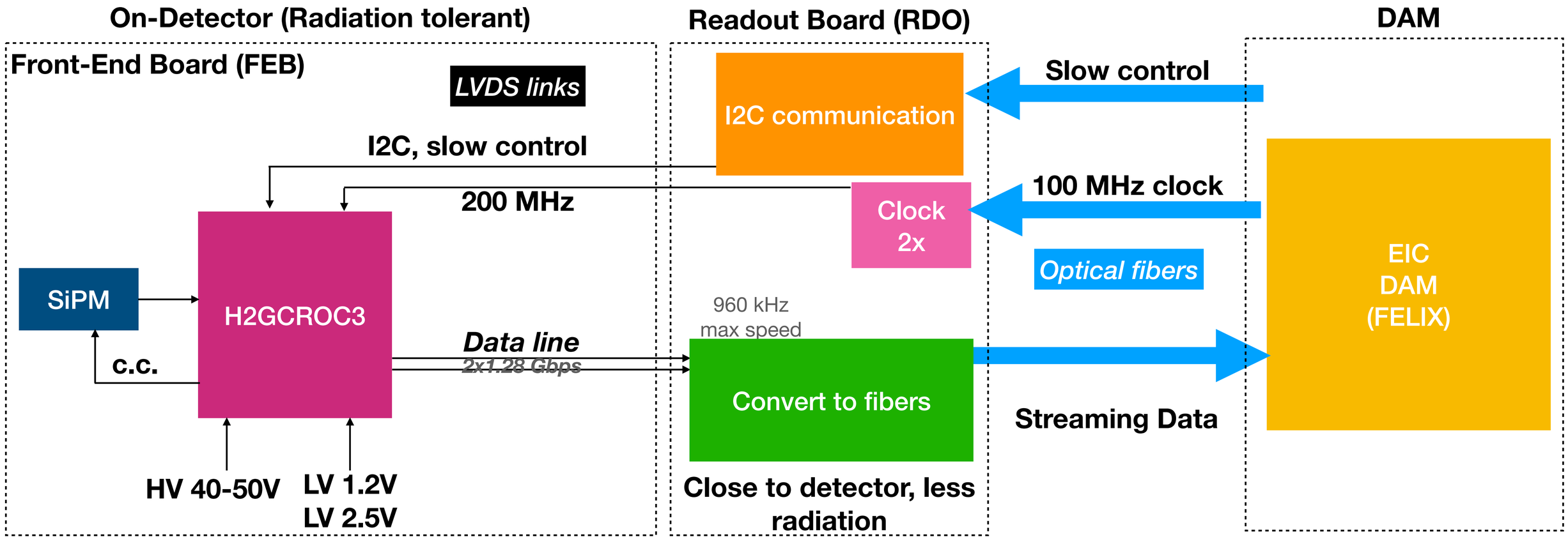
LFHCal readout hierarchy (as of now)



Data propagation from the detector to the EPIC DAQ system:

- The H2GCROC3 requires the L1 trigger for readout, with the maximum speed of 960 kHz
- The expected hit rate in **one channel of LFHCal** is up to 50 kHz:
  - With possible 4 sample readout we would reach a maximum of 200 kHz
  - Streaming readout towards the EPIC DAQ system

LFHCal readout hierarchy (after the upgrade)



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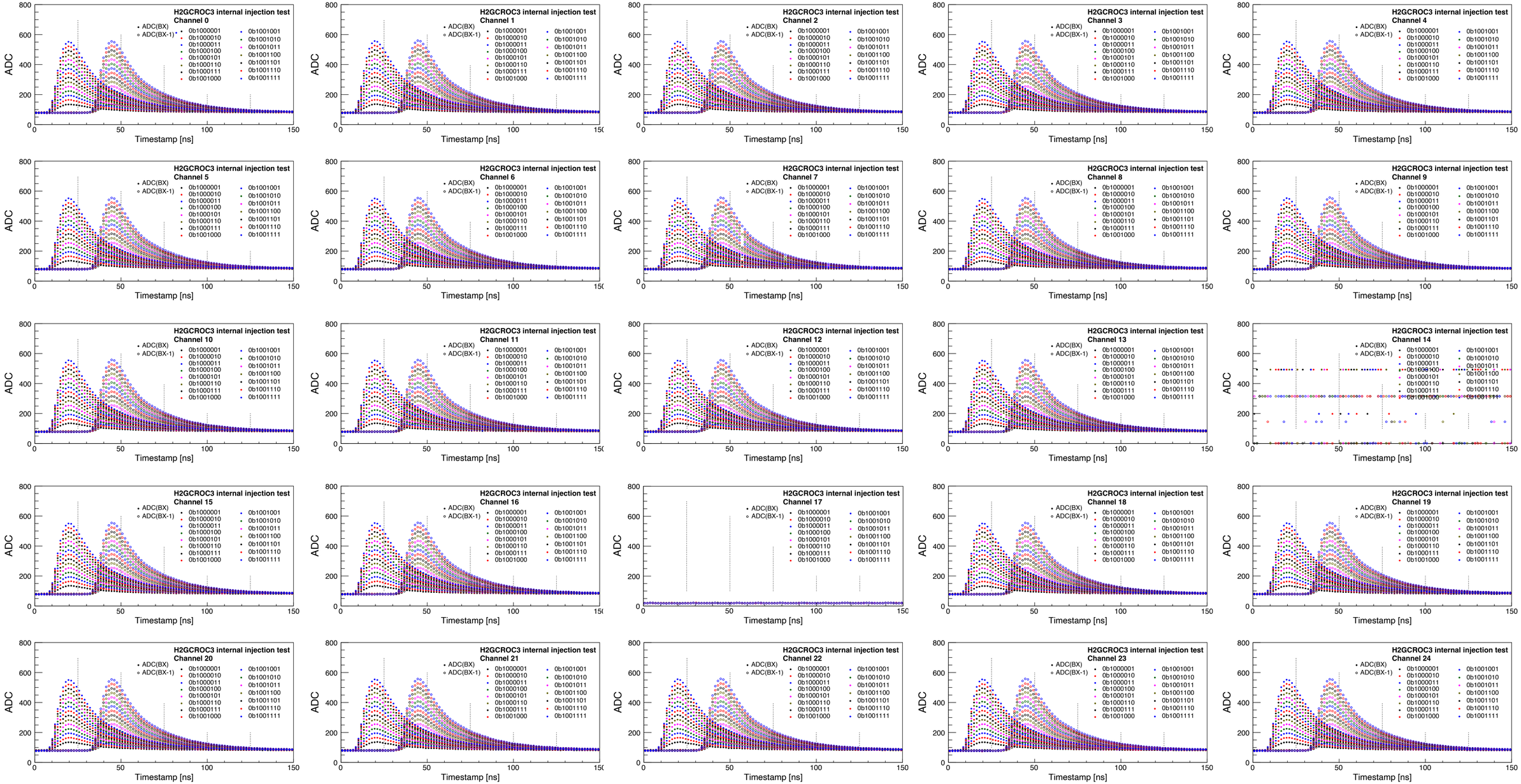
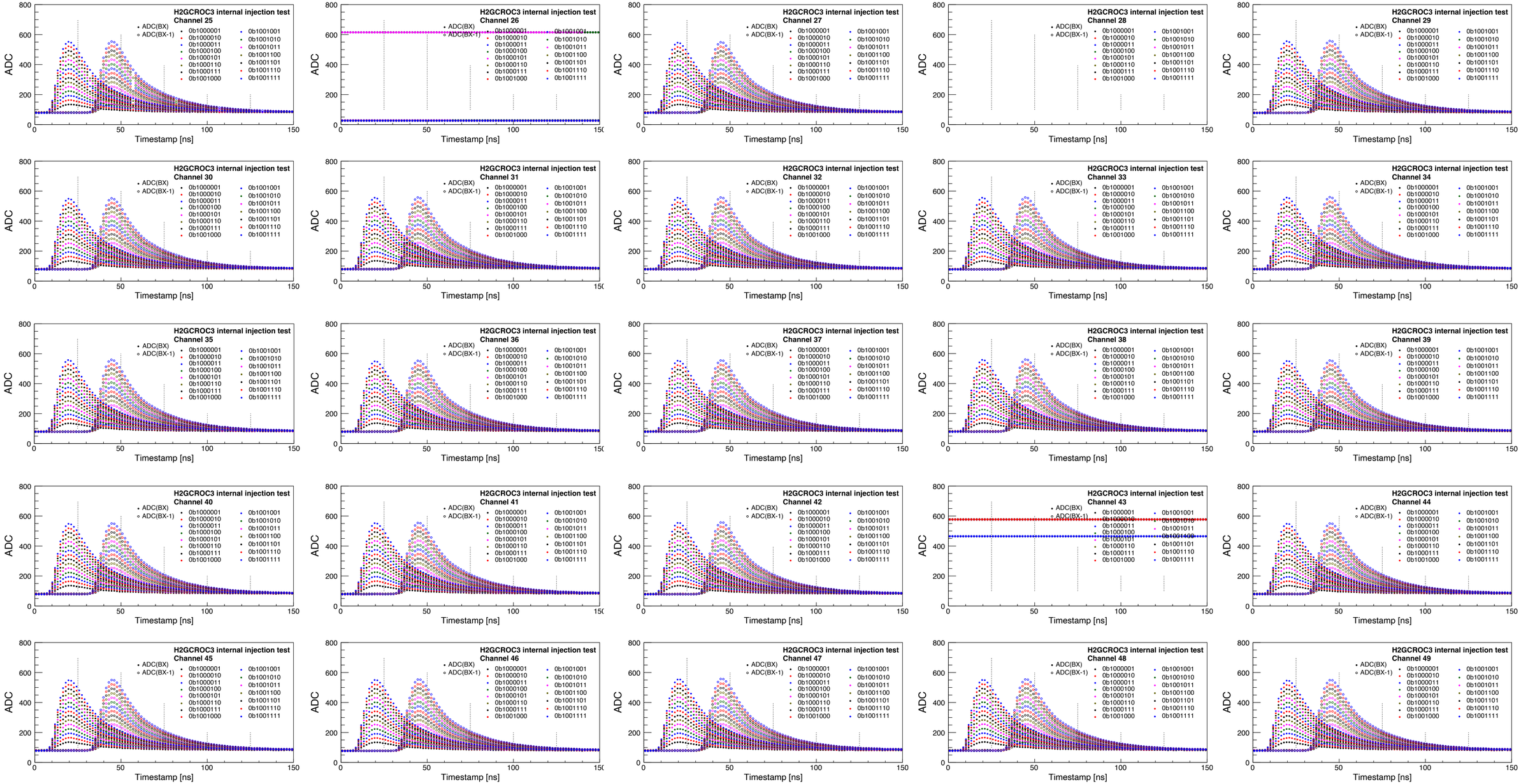
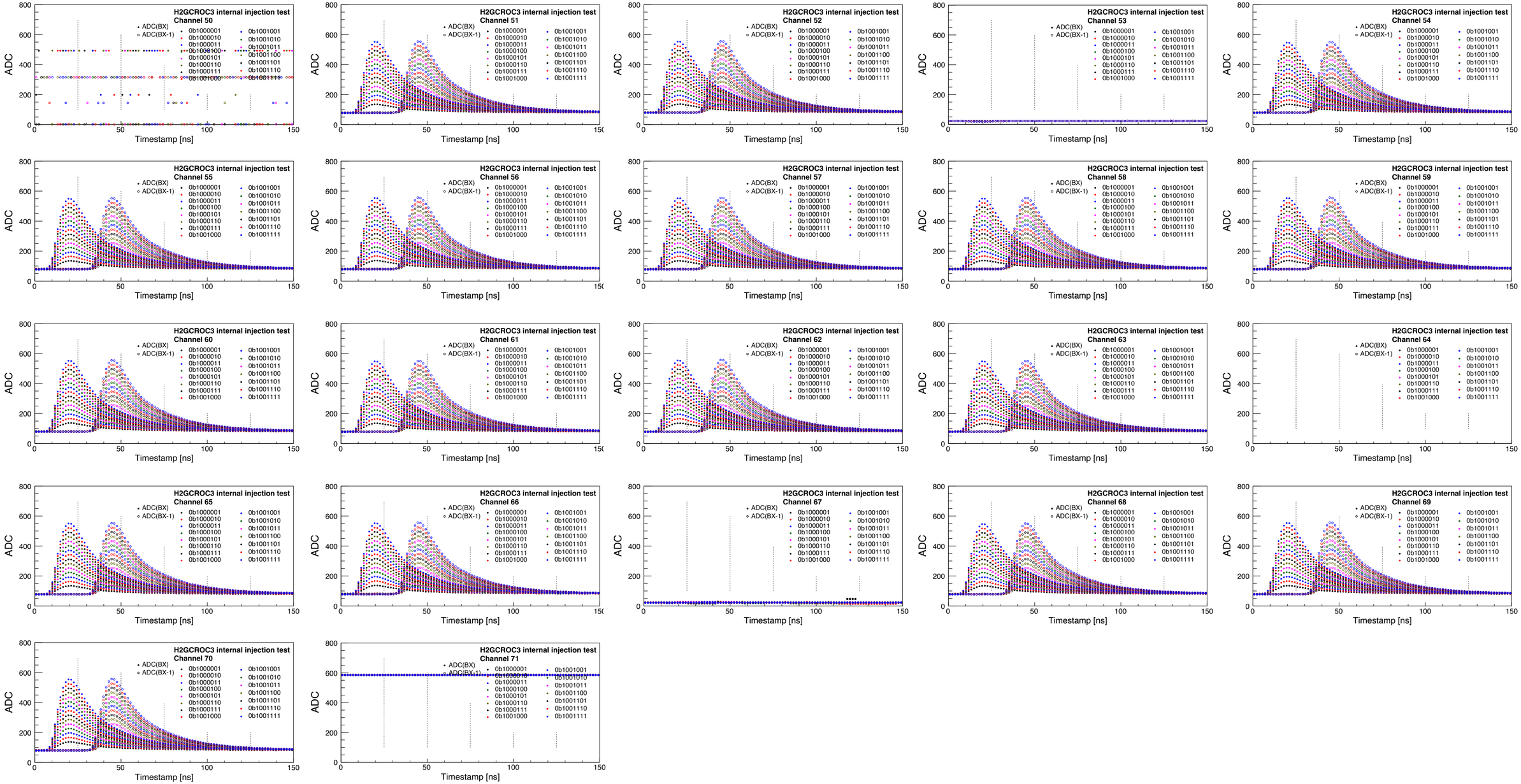
Injection


H2GCROC3 internal injection test
Channel 0
Channel 1
Channel 2
Channel 3
Channel 4
Channel 5
Channel 6
Channel 7
Channel 8
Channel 9
Channel 10
Channel 11
Channel 12
Channel 13
Channel 14
Channel 15
Channel 16
Channel 17
Channel 18
Channel 19
Channel 20
Channel 21
Channel 22
Channel 23
Channel 24
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

Injection


H2GCROC3 internal injection test
Channel 25
Channel 26
Channel 27
Channel 28
Channel 29
Channel 30
Channel 31
Channel 32
Channel 33
Channel 34
Channel 35
Channel 36
Channel 37
Channel 38
Channel 39
Channel 40
Channel 41
Channel 42
Channel 43
Channel 44
Channel 45
Channel 46
Channel 47
Channel 48
Channel 49
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]

Injection


H2GCROC3 internal injection test
Channel 50
Channel 51
Channel 52
Channel 53
Channel 54
Channel 55
Channel 56
Channel 57
Channel 58
Channel 59
Channel 60
Channel 61
Channel 62
Channel 63
Channel 64
Channel 65
Channel 66
Channel 67
Channel 68
Channel 69
Channel 70
Channel 71
ADC(BX)
ADC(BX-1)
0b1000001
0b1000010
0b1000011
0b1000100
0b1000101
0b1000110
0b1000111
0b1001000
0b1001001
0b1001010
0b1001011
0b1001100
0b1001101
0b1001110
0b1001111
ADC
Timestamp [ns]