dRICH RDO
“VTRx+ needs for dRICH”

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Reference: major update about dRICH DAQ at recent last 15 November

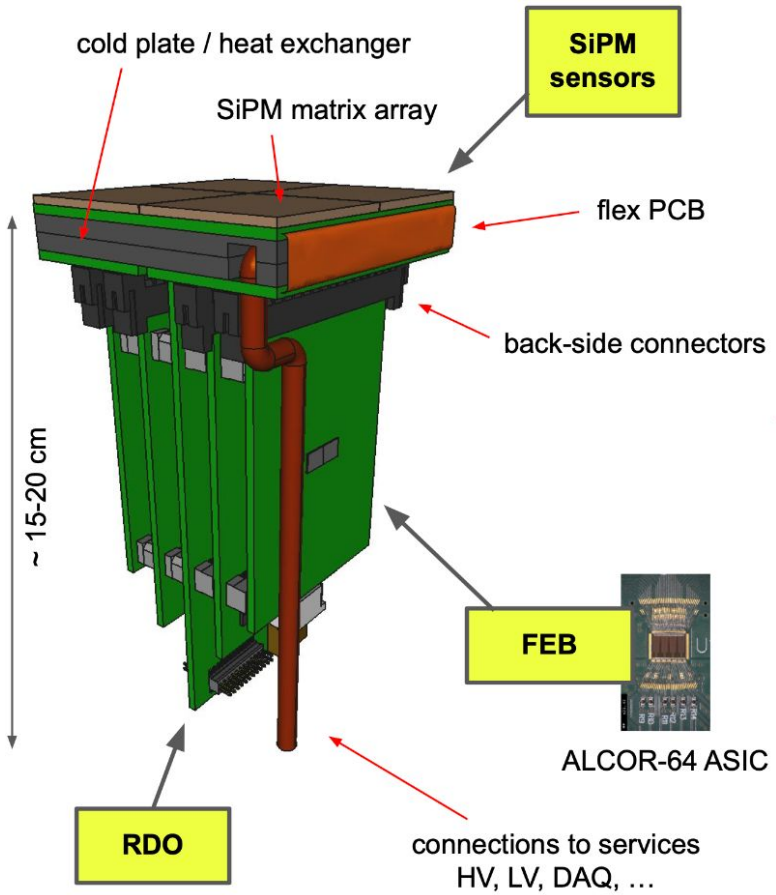
Outline

- RDO Overview
- Design elements and miscellanea updates VTRx+ (and RDO) relevant
  - VTRx+ update
  - Inputs from CMS Padova and ePIC DAQ
  - SEU rates + FPGA choice and baseline selections
- Baseline RDO design: VTRx+ integration
- Back-end information & plans

RDO: where is inside dRICH?

Photodetector unit

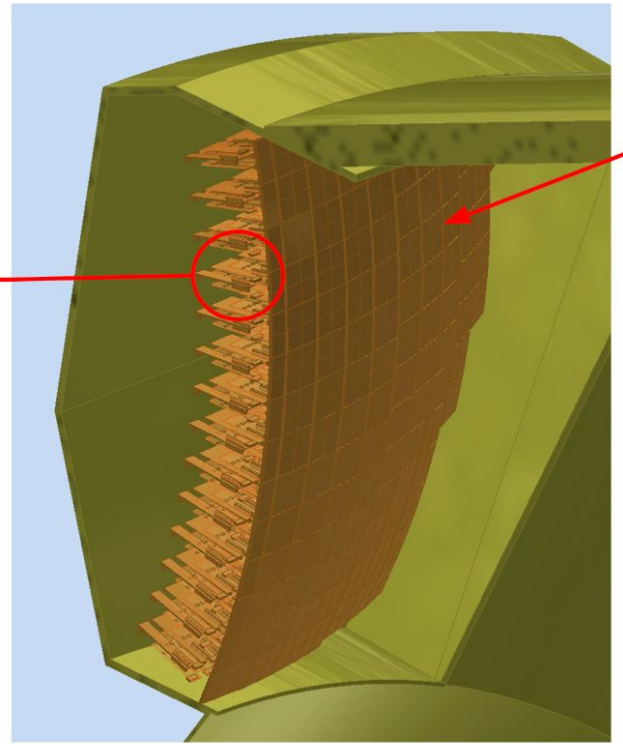
conceptual design of final layout

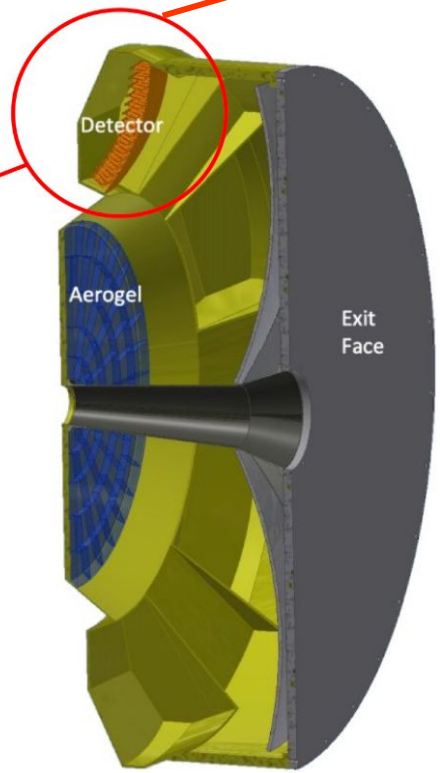


SiPM sensor matrices mounted on carrier PCB board

- 4x 64-channel SiPM array device (256 channels) for each unit
- 1248 photodetector units for full dRICH readout
  - 4992 SiPM matrix arrays (8x8)
  - 4992 ALCOR-64 chips
  - 319488 readout channels

detector box is a “compressed” space!





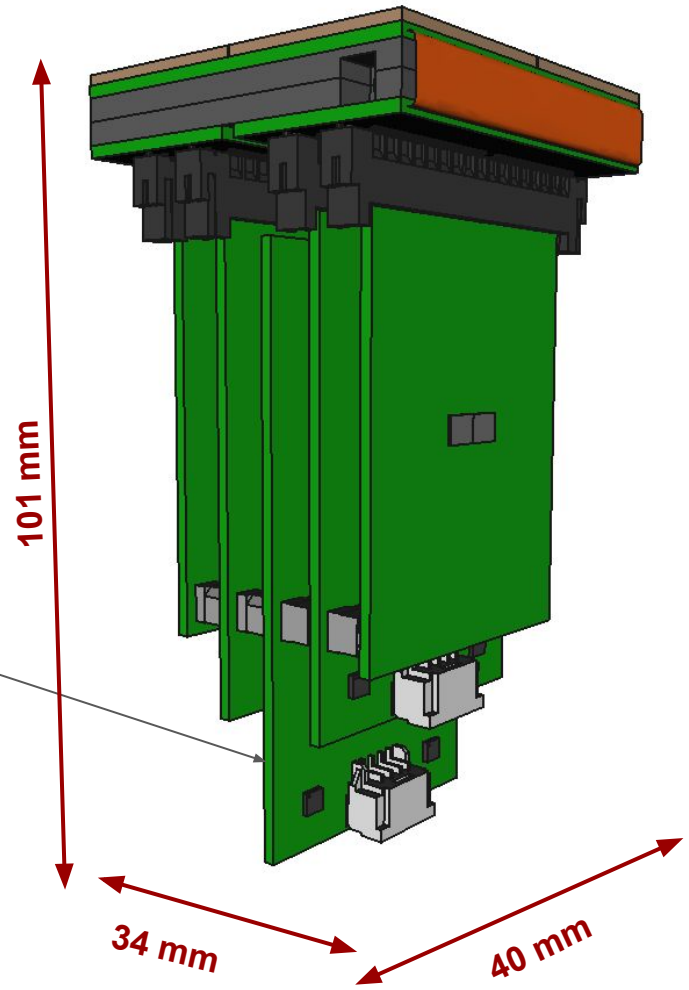
From R. Preghenella talk at last dRICH meeting (15 November)

RDO Overview

RDO is as a *component* of dRICH PDU

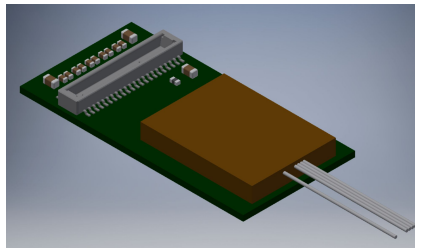
basic RDO specs/numbers:

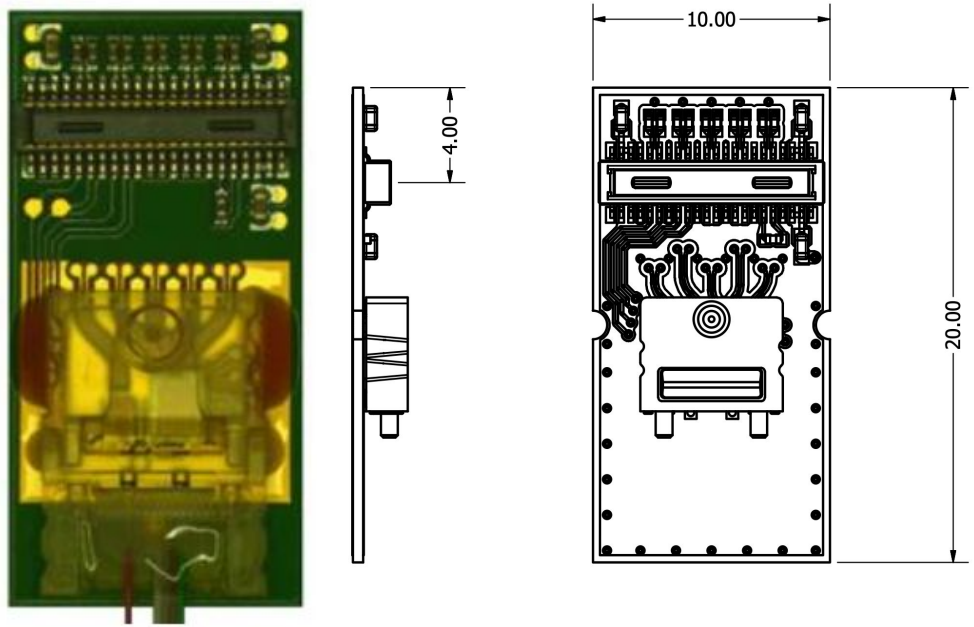
- provide interface to ePIC DAQ
- provide readout/config to 4 ALCOR64
- route HV to SiPM via FEB
- 1 optical link (TX/RX)
- “control” annealing (MOSFET setup)
- services (T sensors, current monitor, …)
- 4x9 cm^2 surface available

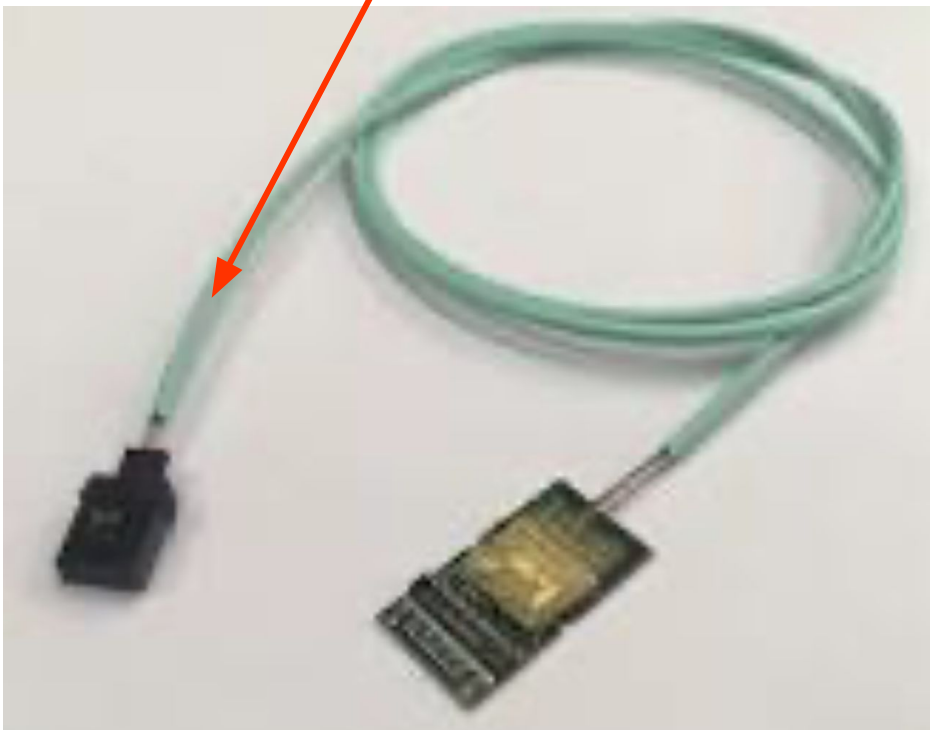


VTRx+ update

- remember: VTRx+ has a “compact, low-power and rad-tolerant” optical transceiver
- bandwidth: 10 Gbps TX, 2.5 Gbps RX
- requested ePIC/EIC project to prebook **1500 VTRx+ for dRICH:** this is **total + 20% spares**
- ordered via CERN/ALICE 20 VTRx+ for 2024/5 pre-production (pigtail 40 cm length with MTP connector)



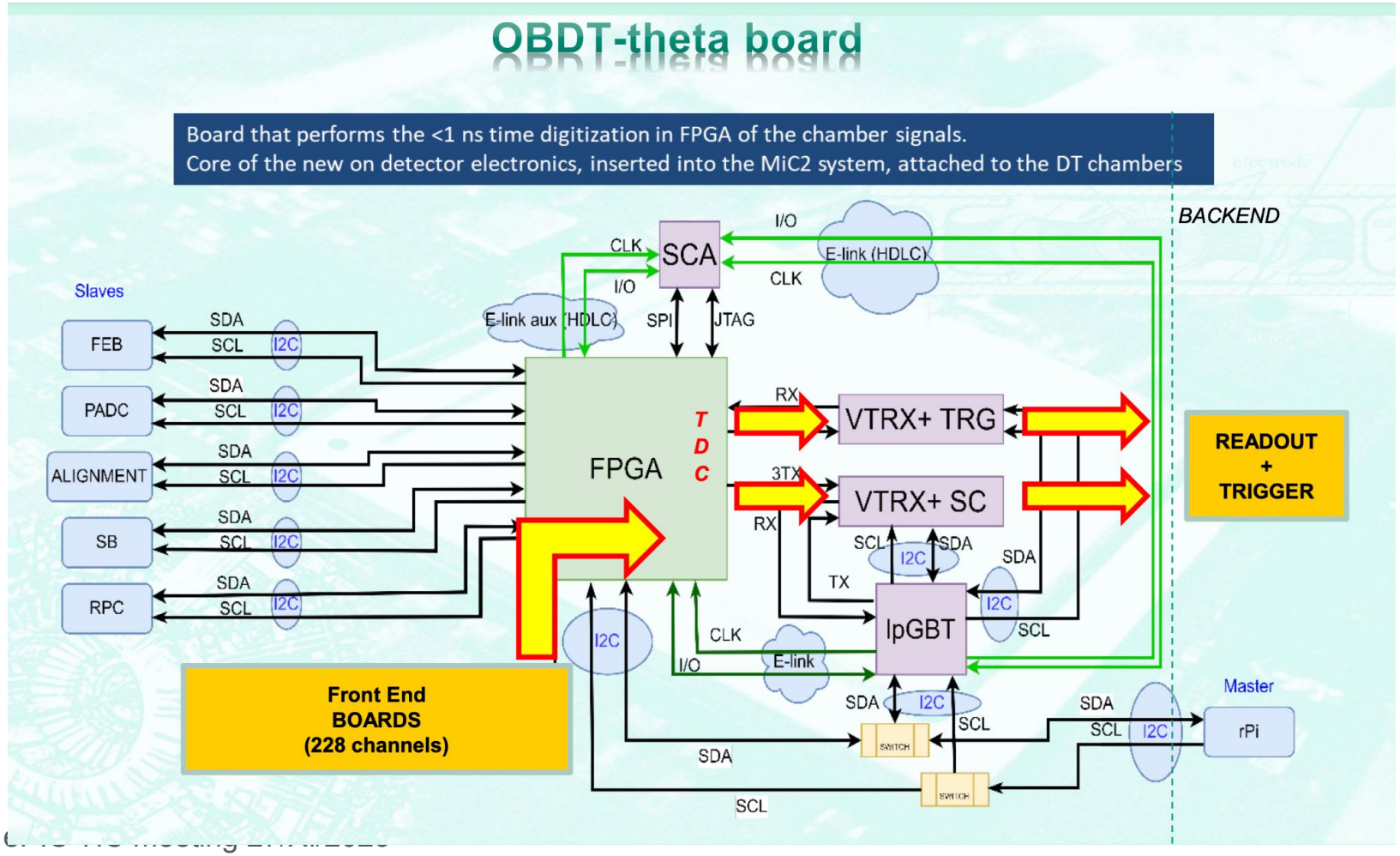




note traditional LHC application is lpGBT + VTRx+

Input from CMS Padova

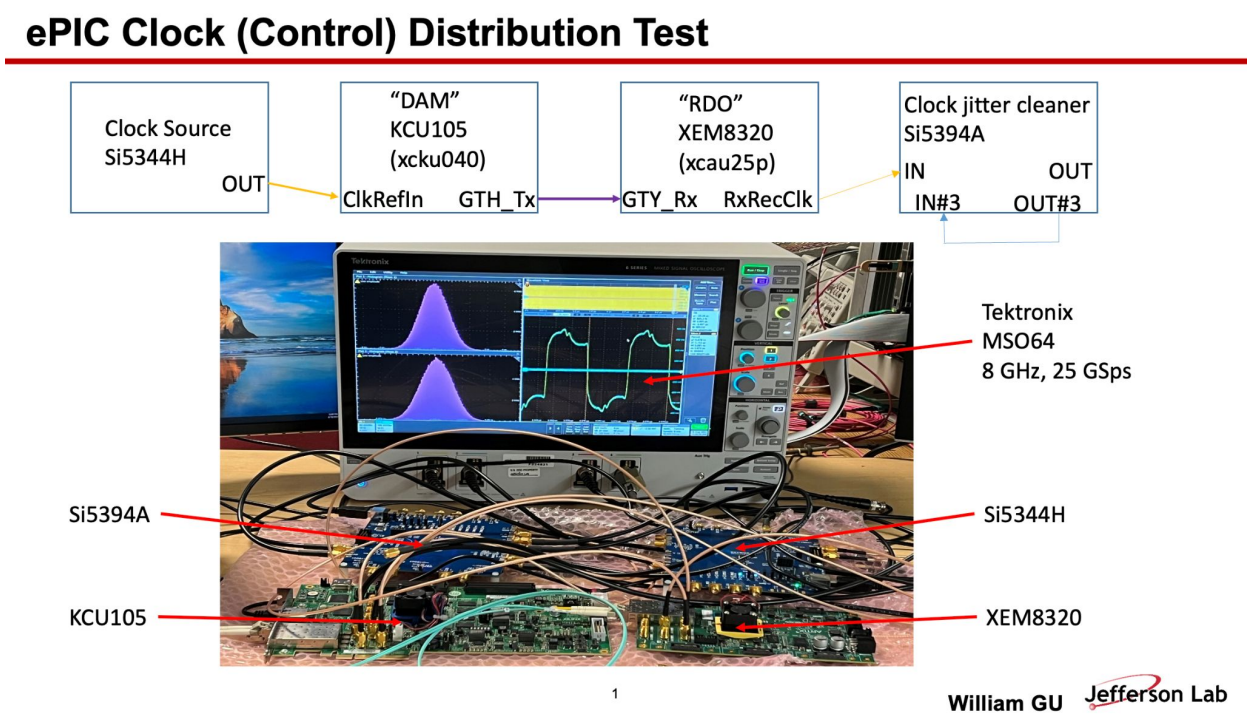
CMS Padova realized for Drift Tube chambers readout a card with a Polarfire FPGA without using lpGBT (to send data)

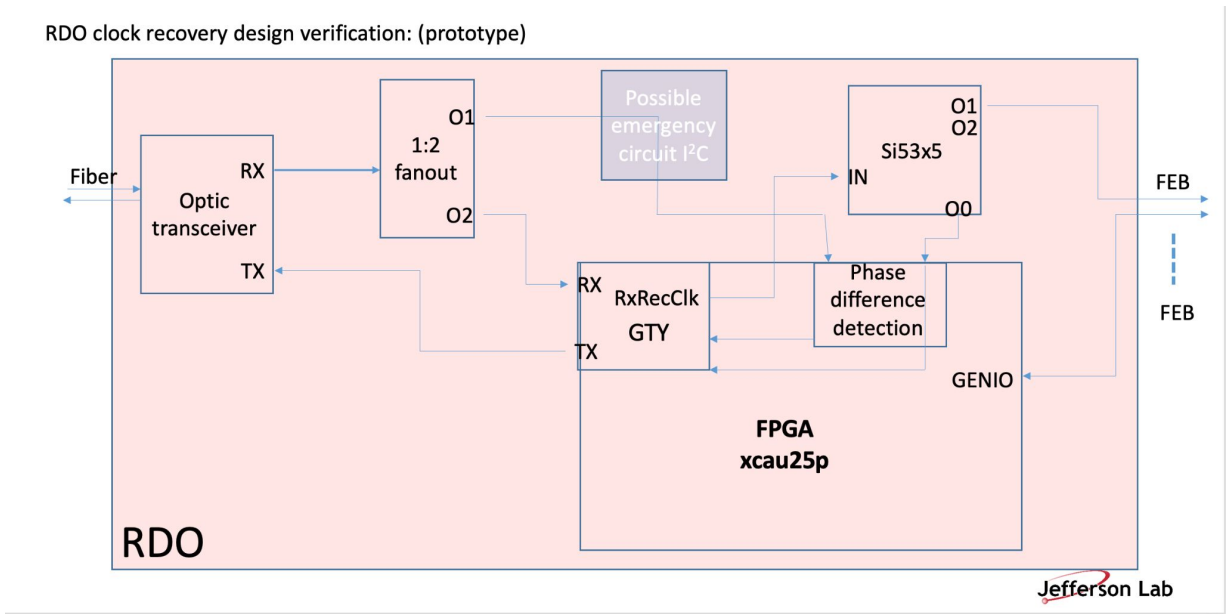


- no problem connecting directly FPGA serializer to VTRX+
- however clock still reconstructed via lpGBT

clock recovery on PolarFire might be challenging

Input from ePIC timing subgroup



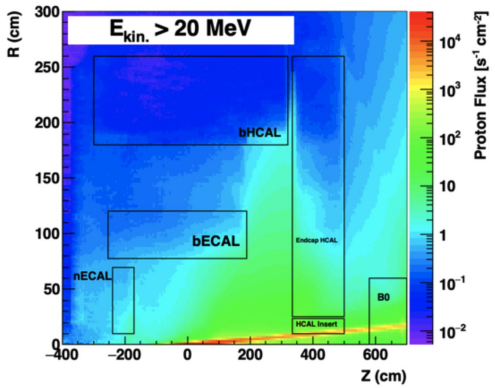


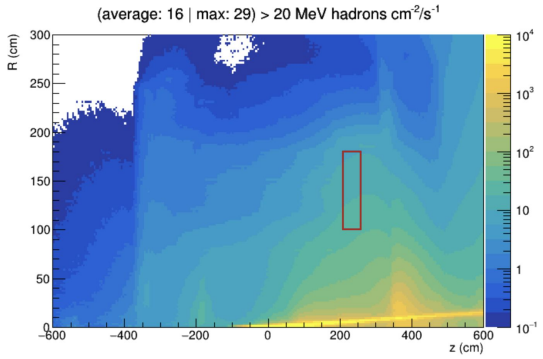
- Context: ePIC timing subgroup is a subset of DAQ&Electronics WG
  - First tests from W. Gu (JLab)
  - J. Schombach (ORNL) testing lpGBT+VTRx+ clock transmissions
  - Jo presented recently results using lpGBT+VTRx+ using a frequency equal to ⅔ f_{EIC} (39.42 MHz)

- ePIC link protocol not yet defined
- default RDO should have ARTIX UltraScale+
- clock multiplier from 98 MHz to 396 MHz to be studied with care

SEU rates + FPGA selection

Xilinx declares 2.67 × 10^{-16} cm^2/bit cross-section for CRAM bits
AUP15 has 42.8 × 10^{+6} configuration bits
dRICH flux (hadrons > 20 MeV): 20 $cm^{-2}s^{-1}$





1 SEU every 4.3x10^6 s/FPGA

↓

1 SEU every 3.5x10^3s/dRICH

↓

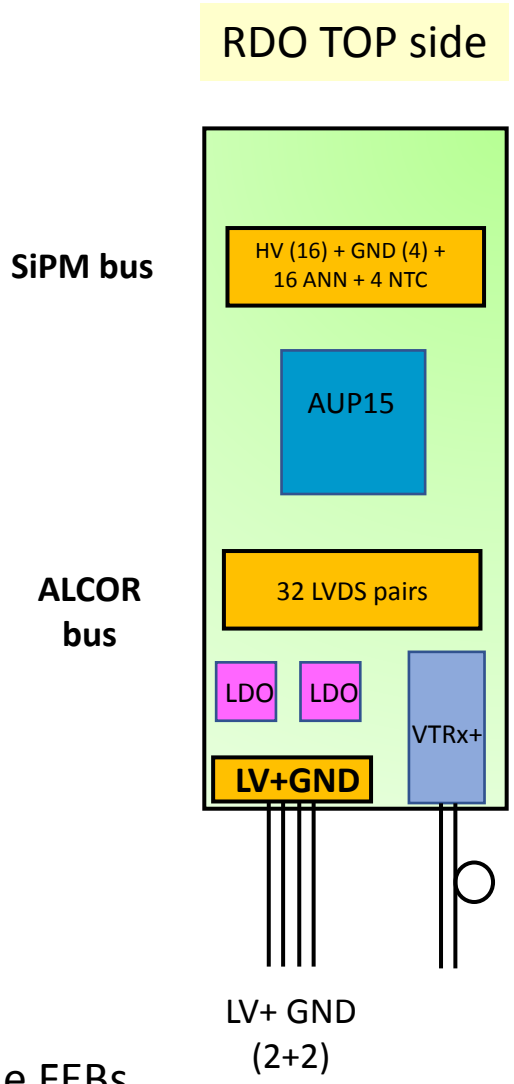
1 SEU every hour in whole dRICH

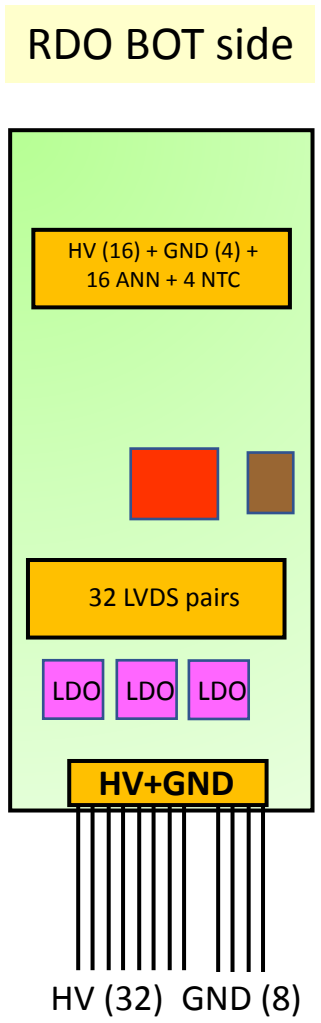
- SEU rate if confirmed seems manageable
- A scrubber might not be strictly needed
- RDO final design to be validated with a full irradiation test

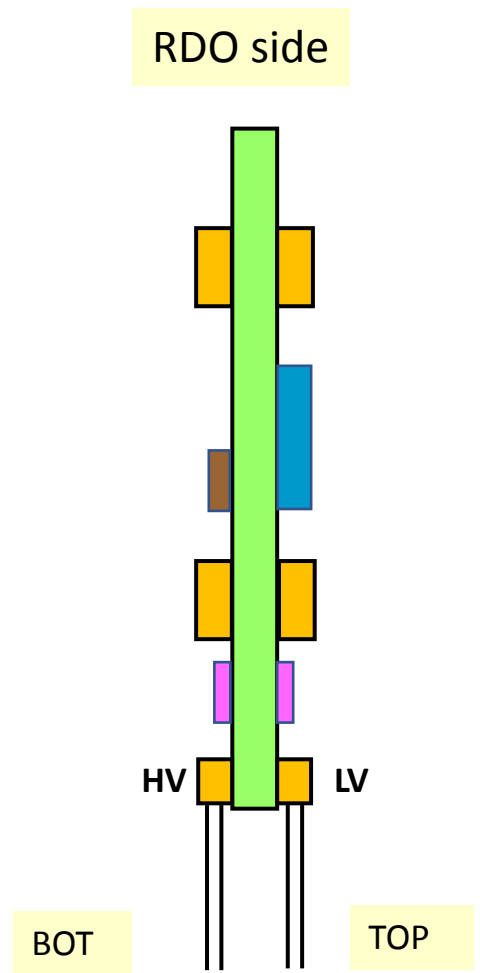
- Artix Ultrascale+ AU15P-SBVB484 (see backup) good compromise between physical size 1.9x1.9 cm^2, resources (5.1 Mb RAM), I/O pins (204)
- Smallest available Polarfire (MPF050T) as rad-tolerant scrubber seems effective choice (see later)

What about other ePIC RDO locations? SEU rate?

RDO and VTRx+: how they could look like (I)



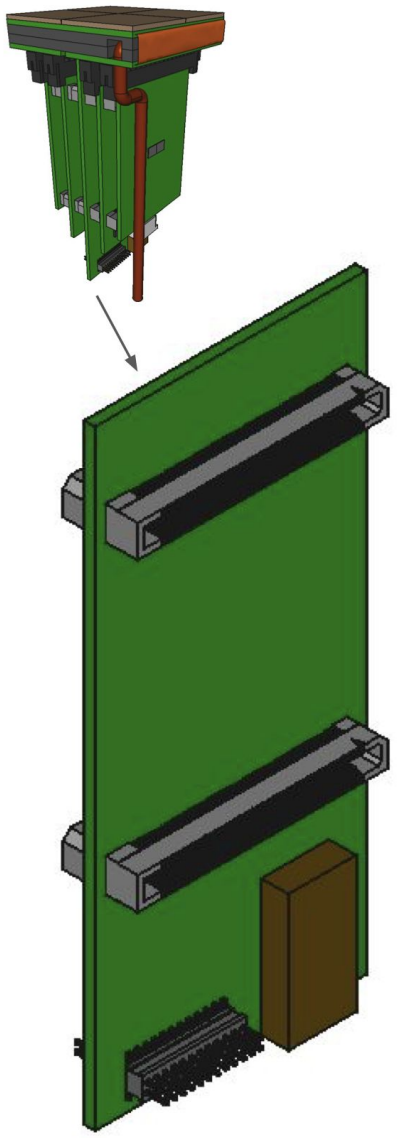


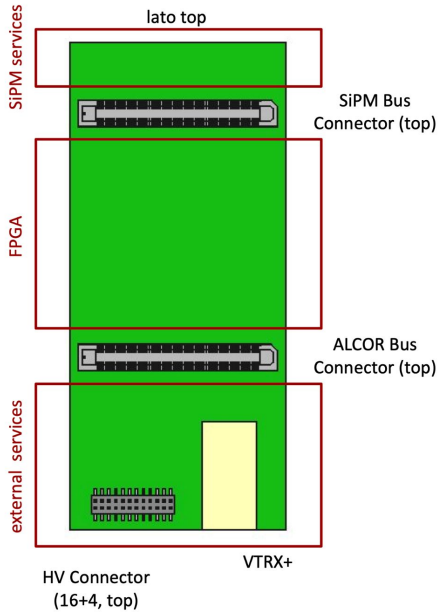


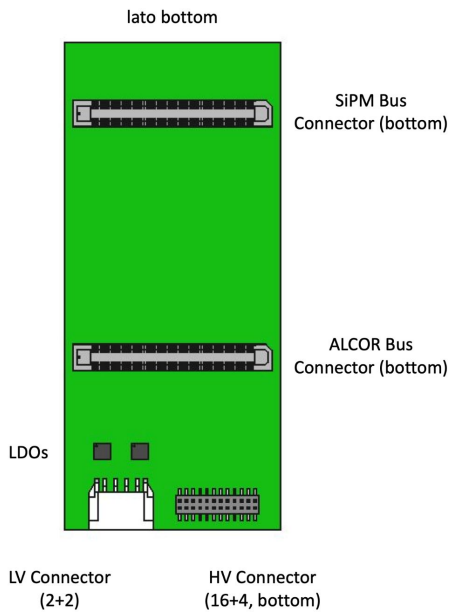
RDO does not distribute LV to the FEBs

components on scale excluding connectors

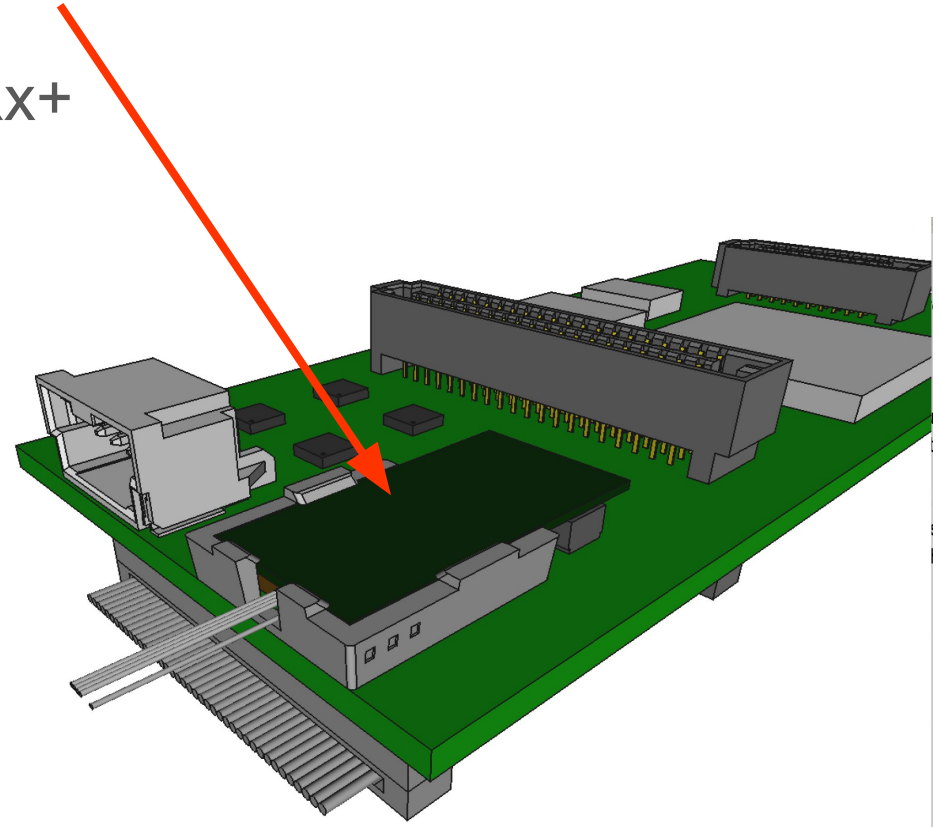
RDO and VTRx+: how they could look like… (II)





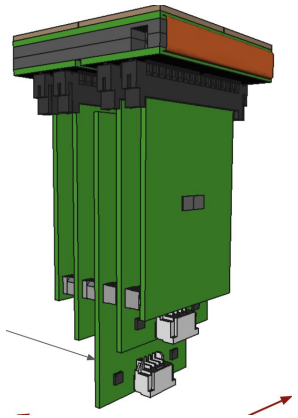


VTRx+



- VTRx+ pigtail length and cabling to detector box to be discussed with DAQ group (see talk by J. Huang at DAQ meeting 2 Nov)
- TOF group is developing in 2024 a RDO prototype too. We are in touch and plan is to share expertise (and possibly IP…;-))

RDO and ePIC DAQ



1248

- PDU: 1248
- RDO: 1248
- FEB: 4992

1248

I-level DAM (27)

- 47 links to PDU
- 1 link to II-level DAM

27

in exp. hall, rack mounted

PC with 4 FELIX each (??)

27

II-level DAM (1)

- 27 links to I-level DAM
- link from central ePIC [clock/trigger]

ePIC interaction tagger
able to reach our DAMS in 10 μs!

1

1

dRICH has largest number of RDOs in ePIC

EPIC Detector Scale and Technology Summary:

Detector System	Channels	RDO	Gb/s (RDO)	Gb/s (Tape)	DAM Boards	Readout Technology	Notes
Si Tracking: 3 vertex layers, 2 sagitta layers, 5 backward disks, 5 forward disks	7 m^2 36B pixels 5,200 MAPS sensors	400	26	26	17	MAPS: Several flavors: curved its-3 sensors for vertex Its-2 staves / w improvements	Fiber count limited by Artix Transceivers
MPGD tracking: Electron Endcap Hadron Endcap Inner Barrel Outer Barrel	16k 16k 30k 140k	8 8 30 72	1	.2	5	uRWELL / SALSA uRWELL / SALSA MicroMegas / SALSA uRWELL / SALSA	64 Channels/Salsa, up to 8 Salsa / FEB&RDO 256 ch/FEB for MM 512 ch/FEB for uRWELL
Forward Calorimeters: LFHCAL HCAL insert* ECAL W/SciFi Barrel Calorimeters: HCAL ECAL SciFi/PB ECAL ASTROPIX Backward Calorimeters: NHCAL ECAL (PWO)	63,280 8k 16,000 7680 5,760 500M pixels 3,256 2852	74 9 64 9 32 230 18 12	502	28	19	SiPM / HG2CROC SiPM / HG2CROC SiPM / Discrete SiPM / HG2CROC SiPM / HG2CROC Astropix SiPM / HG2CROC SiPM / Discrete	Assume HGCROC 56 ch * 16 ASIC/RDO = 896 ch/RDO 32 ch/FEB, 16 FEB/RDO estimate, 8 FEB/RDO conserve. HCAL 1536x5 *HCAL insert not in baseline Assume similar structure to its-2 but with sensors with 250k pixels for RDO calculation. 24 ch/feb, 8 RDO estimate, 23 RDO conservative
Far Forward: B0: 3 MAPS layers 1 or 2 AC-LGAD layer 2 Roman Pots 2 Off Momentum ZDC: Crystal Calorimeter 32 Silicon pad layer 4 silicon pixel layers 2 boxes scintillator	300M pixel 1M 1M (4 x 135k layers x 2 dets) 640k (4 x 80k layers x 2 dets) 400 11,520 160k 72	10 30 64 42 10 10	15	8	8	MAPS AC-LGAG / EICROC AC-LGAD / EICROC AC-LGAD / EICROC APD HGCROC as per ALICE FoCal-E	3x20cmx20cm 600^cm layers (1 or 2 layers) 13 x 26cm layers 9.6 x 22.4cm layers There are alternatives for AC-LGAD using MAPS and low channel count DC-LGAD timing layers
Far Backward: Low Q Tagger 1 Low Q Tagger 2 Low Q Tagger 1+2 Cal 2 x Lumi PS Calorimeter Lumi PS tracker	1.3M pixels 480k pixels 700 1425/75 80M pixels	12 12 1 1 24	150	1	4	Timepix4 Timepix4 (SiPM/HG2CROC) / (PMT/FLASH) Timepix4	
PID-TOF: Barrel Endcap	2.2M 5.6 M	288 212	31	1	17	AC-LGAD / EICROC (strip) AC-LGAD / EICROC (pixel)	bTOF 128 ch/ASIC, 64 ASIC/RDO eTOF 1024 pixel/ASIC, 24-48 ASIC/RDO (41 ave)
PID-Cherenkov: dRICH	317,952	1242	1240	13.5	28	SiPM / ALCOR	Worse case after radiation. Includes 30% timing window. Requires further data volume reduction software trigger
pfRICH DIRC	69,632 69,632	17 24	24 11	12.5 6	1 1	HRPPD / EICROC (strip or pixel) HRPPD / EICROC (strip or pixel)	

work (almost) done communicating dRICH numerology in ePIC

The big dRICH DAQ plan

2024	2025	2026
• **hardware effort** • RDO prototype as close as possible to final • RDO readout of old FEB32 / VTRx+ implementation • initial ePIC link test with RDO (clock) • input to TDR • radiation tests	• integration with ALCOR64 in the PDU • **readout with VC709 & ePIC link (including clock)** • RDO rev. 2 final components • possibly test in detector box • (likely radiation tests again….)	• FELIX available in ePIC to groups • use of DAM (FELIX2) • **crucial firmware development L1-DAM / L2-DAM**

2027	2028	2029
production	assembly	assembly in-situ DAM deployment + commissioning

in parallel:

- someone has to think/build ePIC interaction tagger
- data reduction/calibration through L2-DAM FPGA or SRO to be integrated

Conclusions

- ongoing effort toward specifications/requirements for RDO (at 60/70%)
- defined number of VTRX+ needed (1500) [total + 20% spares]
- secured VTRx+ sample (20) for early prototypes and defined FPGA baseline
- good liaisons with relevant ePIC “corners” (DAQ group, timing DAQ sub-group, other subsystems working on RDO prototypes…)

With respect to ePIC, our asks (somehow RDO, VTRx+ and DAQ related)

★ need of a final word about securing this pre-booking with CERN
★ common mitigation strategy for SEU in RDO Artix Ultrascale+ based?
★ RDO design and dRICH DAQ is sustainable as long as we will have an interaction tagger (to be at least partially described in the TDR…)