On the use of VTRX+ in ePIC MPGD detectors

Irakli.mandjavidze@cea.fr
on behalf of the MPGD group

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Quick outlook

- Studies of the use of VTRX+ CyMBaL tracker based on system considerations approach
  - → Bandwidth and functional considerations
  - → Mechanical, radiation, magnetic field and power constraints

- 3 frontend organization options studied combined with 2 powering schemes
  - → FEB with electrical RDO interface
    - no VTRX+
  - → Merged FEB / RDO with optical VTRX+ interface
    - With a variant of an on-detector RDO serving a number of FEBs
  - → FEB with optical interface
    - COTS FireFly from Samtec or community VTRX+

- Studies applicable and extended to all MPGDs
  - → Can be shared with interested groups
    - For crosscheck, improvements
    - For alleviation or enhancement of preoccupations

- Brief outcome concerning only VTRX+ use cases

Few details in Backup

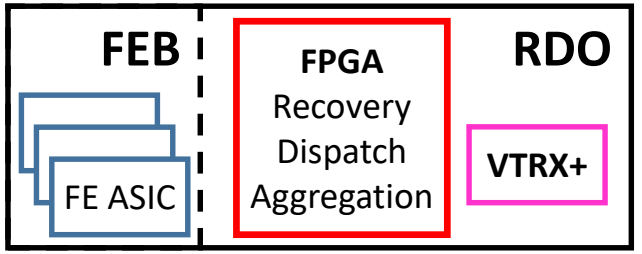
General remarks on VTRX+

- Bandwidth
  - → The 2.5 Gbit/s Rx link is more than enough to synchronize frontends, convey sync and async commands
  - → The 4 x 10 (5) Gbit/s Tx links are more than enough to transmit physics, calibration, slow control and monitoring data
- Environmentally friendly
  - → Lightweight
  - → Small
  - → Radiation hard
  - → Low power
    - However, requires 2 power supplies
- Fragile
  - → A common ePIC pool of QA provision units ?
  - → Per sub-system pool ?
- Pigtail feature
  - → May require more than 1 pigtail length
    - Increasing the pool of QA provision units
  - → May require to take the choice decision now
    - When space constraints of the inner detector are still changing

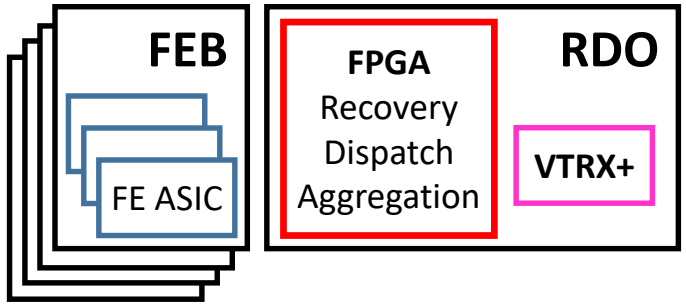
Estimation of MPGD VTRX+ needs based on current knowledge

- Certain VTRX+ frontend organization options require an on-board “intelligence” implementing a subset of lpGBT
  - → An association of a low-end FPGA and VTRX+

  - → Merged FEB / RDO : ~650 VTRX+ units including 10% extras for prototyping
    - CyMBaL 128 ; µRWELL-BOT 384 ; µRWELL-ECT 80
    - ~50% more power compared to lowest power option of a FEB with electrical RDO interface
      - 45 – 48 mW / channel



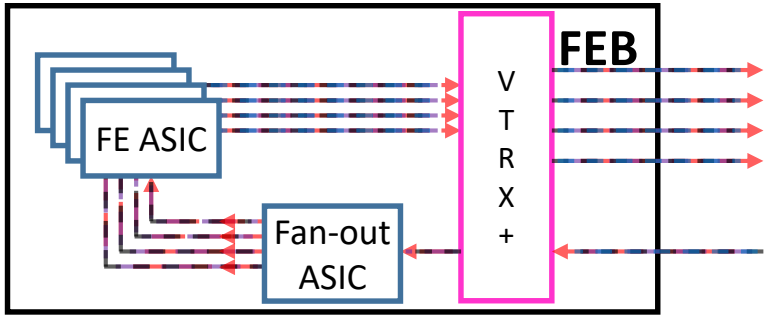
  - → On-detector RDO : ~190 VTRX+ units including 25% extras for prototyping
    - RDO aggregating 4 FEBs
    - CyMBaL 32 ; µRWELL-BOT 96 ; µRWELL-ECT 20
    - ~11% more power compared to lowest power option of a FEB with electrical RDO interface
      - 33 – 37 mW / channel



- Harsh environment especially due to almost 2T magnetic field
  - → Complex power distribution network for multiple voltage rating components : at least, 1V (substantial), 1.2V (bulk), 2.5V, may be 1.8V
    - May require bulky high cross-section LV wires if DC-DC converters cannot be used
    - May require extra space for DC-DC converters if they are bulky and for shielding if they are EMI source
  - → Make sure SEU rates are acceptable and recovery time is low
    - *e.g.* 8h MTBF for entire CyMBaL tracker with 128 merged FEB/RDOs

Estimation of VTRX+ needs based on current knowledge

- FEB with direct VTRX+ optical interface option requires special features from FE ASIC
  - → An on-chip interface to downstream serial Rx link for clock, sync and async command recovery
  - → Plus non-mandatory handy features
    - Low speed ADC for on-chip and environmental monitoring
    - Few GPIO pins for on board control
  - → (more than) considered for Salsa



  - → 660 VTRX+ units including 10% extras for prototyping
    - ~8% more power compared to lowest power option of a FEB with electrical RDO interface
      - 32-35 mW / ch
    - RDO layer removed completely – direct FEB – DAM connections

Rafael fan-out ASIC
Few details in Backup

- Better immunity to harsh environment
  - → Smaller board with tiny extra components
  - → All components are radiation tolerant
  - → May require less complex power distribution network with voltage ratings limited to only 1.2V (bulk), 2.5V (negligible)

Mot de la fin

- Our knowledge of the ePIC Inner detector in general and its MPGDs in particular is not mature enough

- Studies are needed and ongoing within MPGD community, within Elec/DAQ and Integration groups
  - → Can we enhance Salsa with clock-data recovery mechanism ?
  - → Can the same FEB form-factor be used for all MPGDs ?
  - → Can we use FPGAs within the inner detectors ?
  - → Can we use DC/DC regulators within the inner detectors ?
  - → What are the COTS components compatible with the low ePIC radiation environment ?
  - → Can we count on ePIC-wide access to CERNs radiation hardened, magnetic field tolerant powering components?
  - → How close can be RDOs placed to FEBs ?
  - → How close can be LV power supplies placed to FEBs ?
  - → …
    - *e.g.* cooling related questions

- Despite of the effort, cannot commit firmly either on VTRX+ use cases nor on their quantities
  - → Depending of FEB/RDO organization options, the needs are O(200) or O(700)
    - Plus 5-10% for QA provision units
  - → Extra uncertainty due to the risk mitigation scenario with 8 more disks and 2 more barrel layers : 224 FEBs
    - 56 or 224 more VTRX+ depending on FEB/RDO organization option
  - → Might be a lost opportunity

Backup

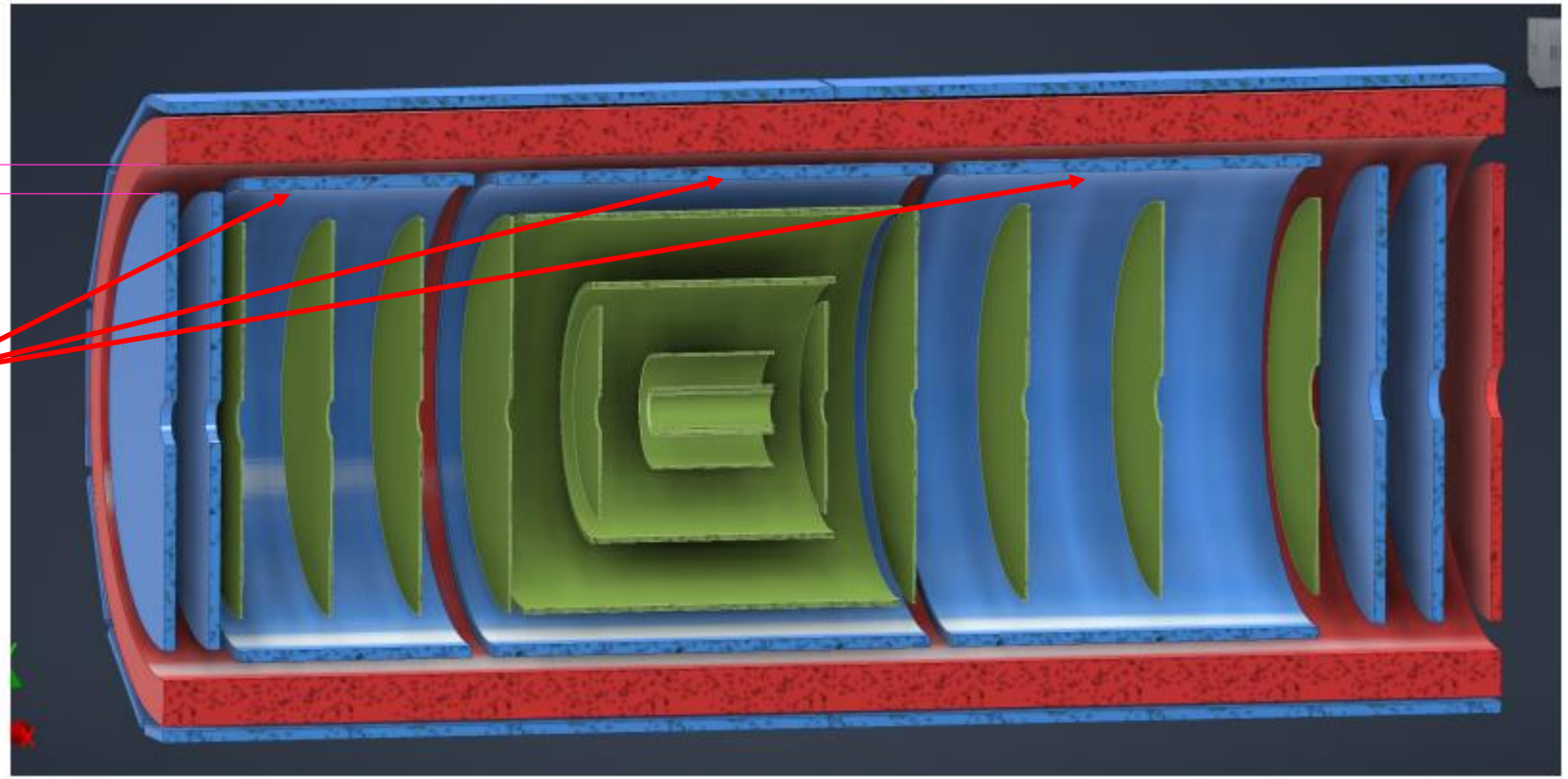
A CyMBaL tracker reminder to illustrate MPGD environment

Spatial constraints for inner barrel cylindrical tracker

- Space is stringent: 6 cm
  → Detectors, gas pipes, HV cables

60

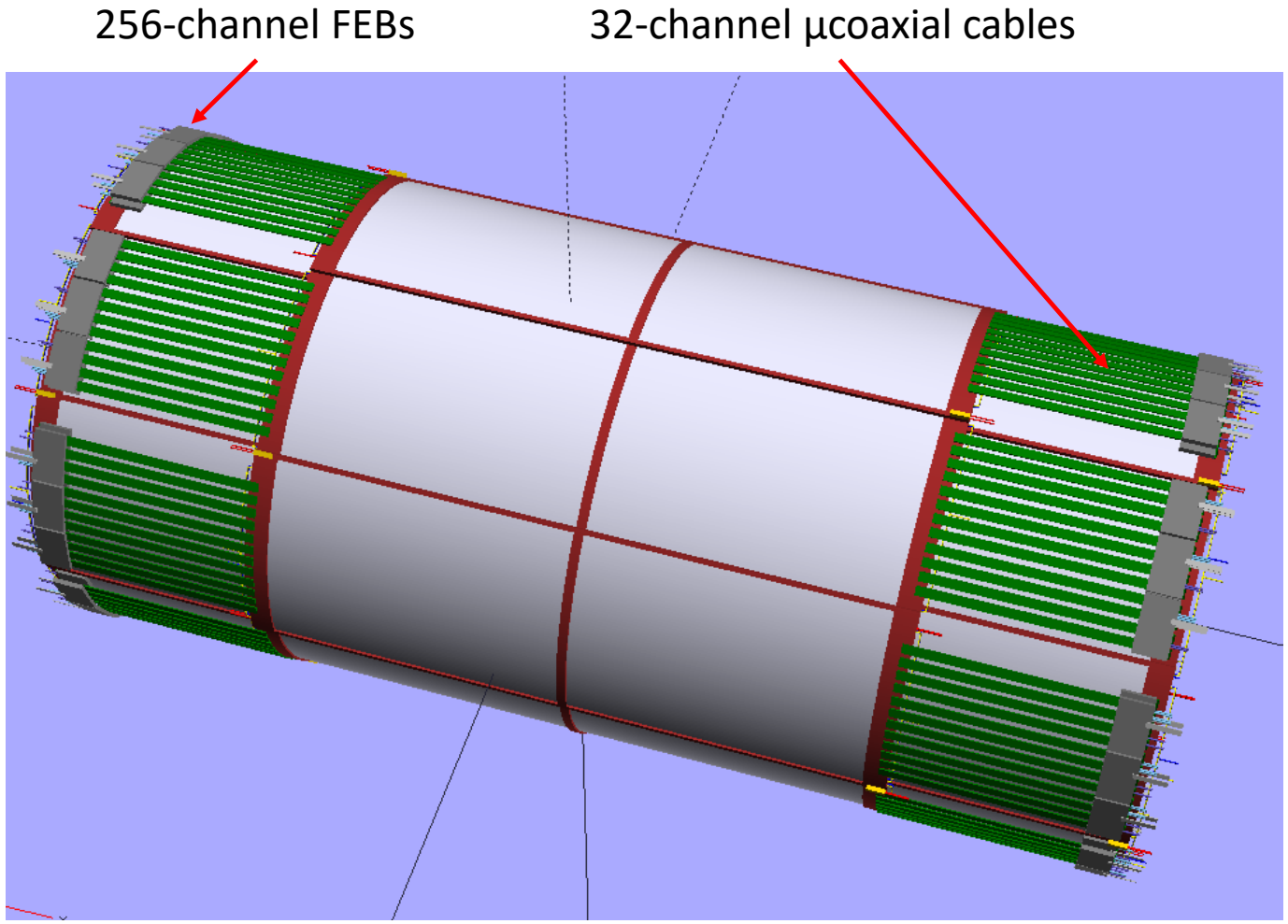
Cylindrical
Micromegas
(Saclay interest)



- On detector frontend electronics
  → FEBs + LV distribution + RDO interface cabling + cooling

Example of CyMBaL: one of the possible configurations under study

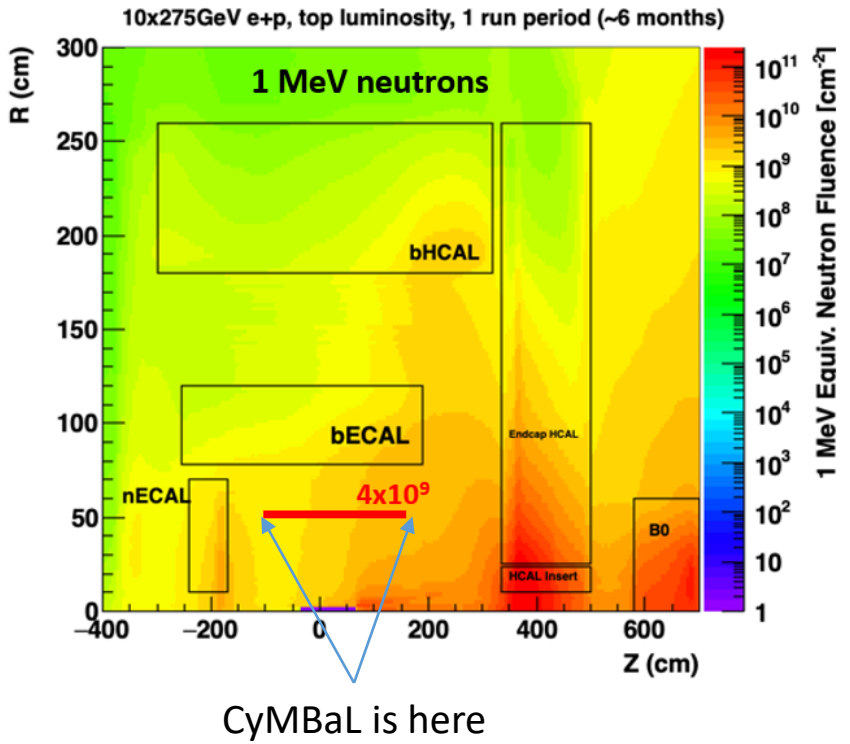
- Still under torment of optimization
  - → Just a snapshot to give an idea
- 32K channels
- 128 256-channel FEBs
  - → Only central detector FEBs visible
    - Peripheral FEBs in a row bellow
    - Or in a second row
- 32 1024-channel RDOs
  - → 4 FEBs per RDO
- Where to place RDOs not really clear
  - → Electrical FEB-RDO interface : 5-6 m
    - 16 on either side of Barrel
  - → Optical FEB-RDO interface : no limit
    - Attractive option



Inner detector fronted environment

- Stringent space
- Restricted material budget including for cooling
- Magnetic field
- Radiation

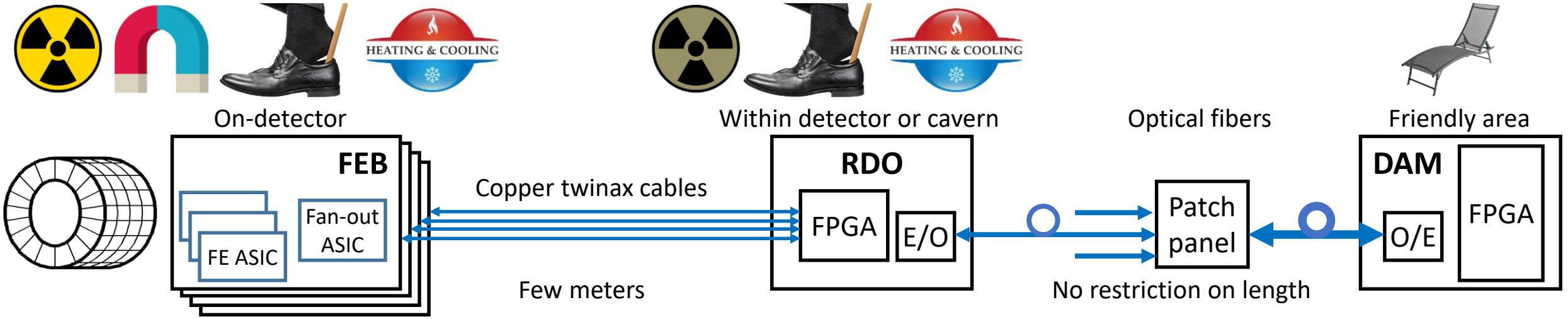
- Example of CyMBaL tracker environment
  - → TID after 10 years : 10 krad
  - → Neutron fluence after 10 years: 10^{11} n_{eq} / cm^2
  - → 20 MeV proton flux: 100 particle / cm^2 / s
  - → Magnetic field: 1.9 T



- Most probably similar radiation and magnetic field environment for other MPGD detector frontends
- What about the radiation and magnetic field environment of other inner detector frontends ?

FE organization options

FEB with no on-board intelligence and electrical interface



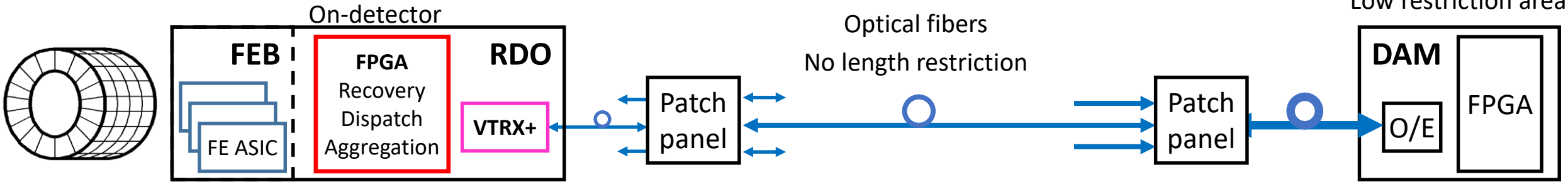
- Passive electrical interface
  - → Downstream: clock, synch commands, asynchronous commands (I2C)
  - → Upstream: physics and calibration data, configuration and monitoring

- FEB
  - → Radiation hardened ASICs
  - → Low active component count: minimal power consumption
    - ~30-35 mW / channel
    - 1 mm^2 (DC/DC + LDO) or 5.6 mm^2 (LDO only) wires to power a FEB
      - Caution: DC/DC regulators may be bulky and source of EMI

- RDO: Is there any suitable place ?
  - → Overall integration issue

Merged FEB / RDO with optical VTRX+ interface

Low restriction area

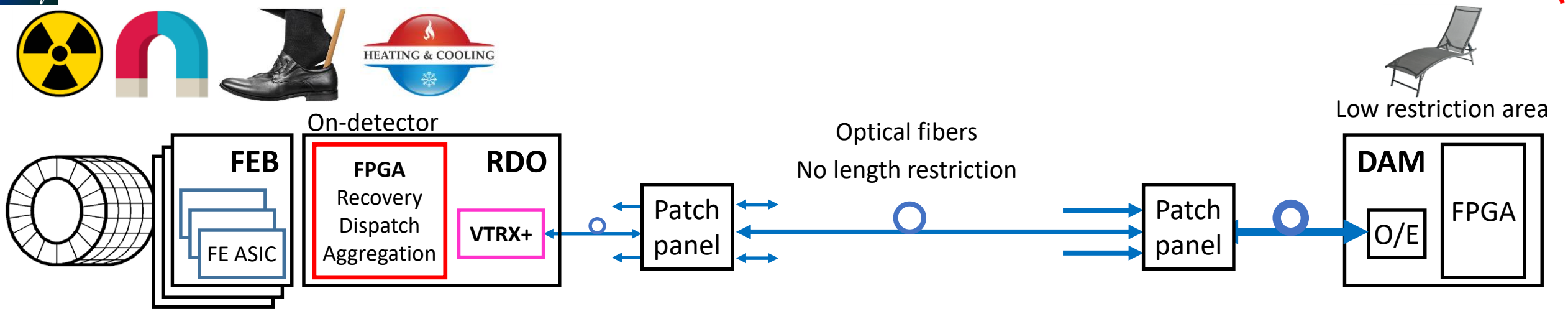


- On-FEB RDO in a harsh environment

- FE ASICs are thought with “lpGBT / CERN” interfaces
  - → Separate lines for downstream interfaces: clock, synchronous commands, asynchronous configuration commands
  - → VTRX+ needs to be coupled with an on-RDO “intelligence” to recover this imbedded information
  - → CERN has lpGBT; ePIC counts on FPGAs

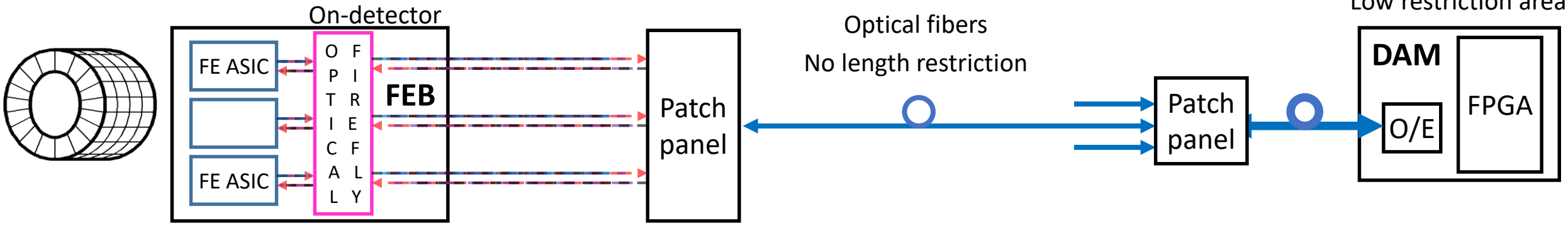
- On FEB FPGA / VTRX+ combination
  - → SEU effects need to be understood, acceptable failure rates to be agreed on
    - Estimation: 8h MTBF for entire CyMBaL with a low cost low profile Latice Nexus radiation tolerant FPGA
  - → Worst power consumption scenario
    - Estimation: 45-50 mW / channel - 50% increase compared to electrical interface
    - 1.5 mm^2 (DC/DC + LDO) or 8 mm^2 (LDO only) wires to power FEB
  - → Cooling and its additional infrastructure !

On-detector RDO with optical VTRX+ interface



- On-detector RDO per detector module
  - → 4 FEBs / RDO
    - Higher integration
    - More optimal use of RDO resources : FPGA logic + VTRX bandwidth
  - → Harsh environment
    - Same SEU preoccupation as for merged FEB / RDO
  - → Further studies needed to understand on-detector space constraints
    - Place
      - An extra board with interface optimization: number, size
    - Power distribution
    - Cooling

FEB with optical interface: COTS optical FireFly

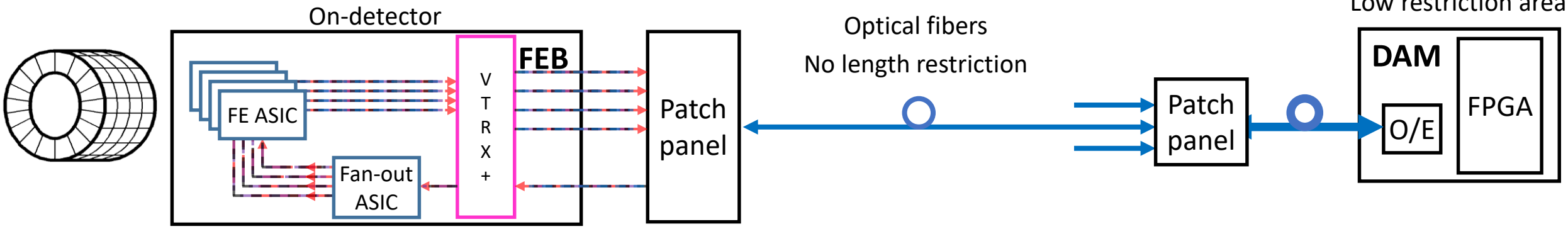


- FE ASICs are directly interfaced to 4-lane bidirectional parallel optic FireFly transceivers
  - → Requires an “innovative” ASIC interface: Rx line encoding clock and data (sync & async commands)
  - → Plus extra handy features:
    - A low speed embedded ADC for environmental monitoring
    - A GPIO outputs for on-board control

- FEB
  - → Radiation hardened ASICs
  - → Low active component count: minimal power consumption
    - ~35-37 mW / channel - 15% increase compared to pure electrical interface
    - 1 mm^2 (DC/DC + LDO) or 6 mm^2 (LDO only) wires to power FEB

- No RDO layer !

FEB with optical interface: VTRX+



- FE ASICs are directly interfaced to VTRX+
  - → Downlink with embedded clock / sync / async data distributed with high fidelity fan-out
  - → Requires an “innovative” ASIC interface
    - Working on CDR circuitry for Salsa

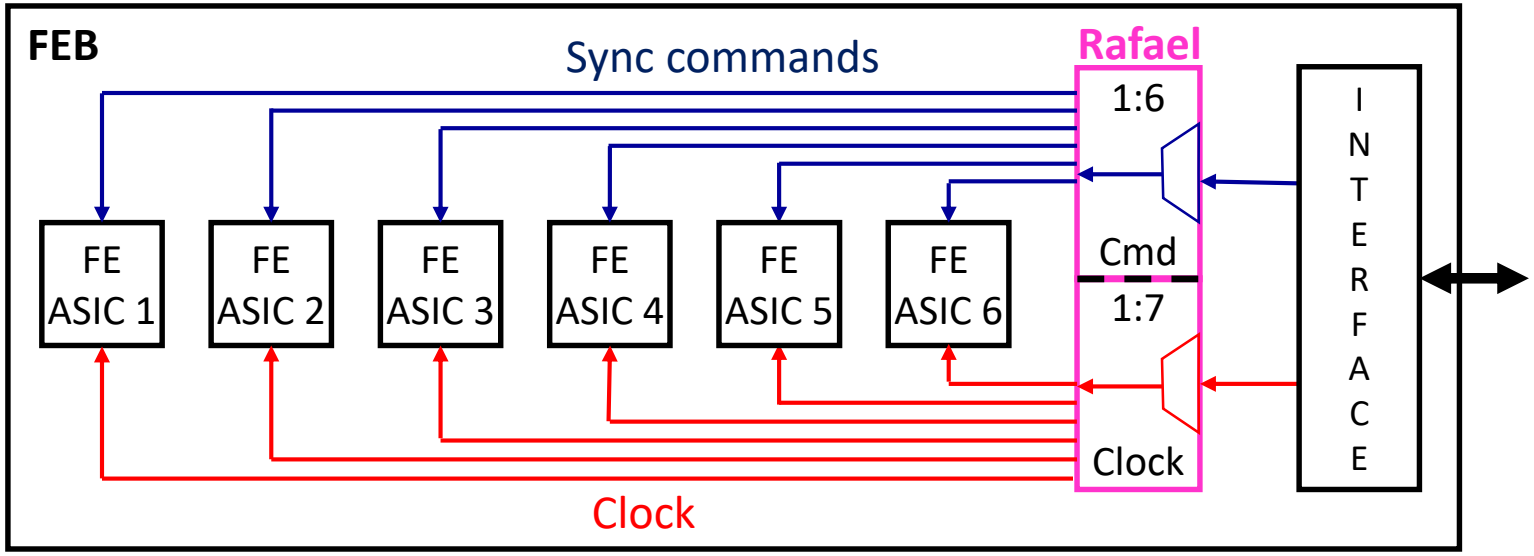
- FEB
  - → Radiation hardened ASICs
  - → Minimal power consumption after electrical interface option: only VTRX+ consumption added
    - ~ 32-35 mW / channel - 8% increase compared to pure electrical interface
    - 0.9 mm^2 (DC/DC + LDO) or 5.8 mm^2 (LDO only) wires to FEB

- No RDO layer !

Clock and fast command distribution example

- Rafael - Radiation-hArd Fan-out ASIC for Experiments at LHC - developed at Irfu, CEA Saclay
  - → 3 inputs and 13 outputs
  - → CLPS signaling
    - CM voltage: 0.6 V
    - Differential swing: 200-400 mV
    - Programmable drive and emphasis
  - → Single buffer: any input to 13 outputs
  - → Double buffer
    - Input 1 to 6 outputs
    - Input 3 to 7 outputs
  - → Up to 400 MHz and beyond
  - → Low additive jitter : < 2 ps
  - → Propagation delay : ~1 ns
  - → C2C and P2P skew : < 300 ps
  - → 130 nm technology
  - → LHC-level TID, neutron, SEU & latch-up

Rafael



Data bandwidth

- Estimated physics data bandwidth per 256-channel FEB
  → CyMBaL tracker
- Data volume determined by physics
  → Calibration data are small
    - Calibration can be done regularly on-line
- Background generated data has to be taken into account
  → Hens safety factor of 5
- VTRX+:
  → Single 5-10 Gbit/s Tx link seems to be enough
    - One needs to aggregate 66.6 64-channel ASICs (4k channels) to load VTRX+ at 50% (20 Gbit/s) of its total throughput
      - 1 VTRX = 1/8 of the entire CyMBaL : simply impractical

  → The 2.5 Gbit/s Rx link is more than enough for MPGDs to
    - Recover good quality clock
    - Pass synchronous commands
    - Pass slow control asynchronous commands
      - That is exactly what is done in Clas12 for sub-nanosecond synchronization of ~20k tracker channels

Channel rate kHz		Sampling Mbit/s	Amplitude - Time Mbit/s
2	(physics)	200	40
10	**(safety)**	**1 200**	**200**
50	(Clas12)	5 500	900