next ASICs for EIC at OMEGA

Ch. de LA TAILLE

Organization for Micro-Electronics desiGn and Applications

Comparison EICROC / HGCROC

EICROC

- « 2D chip » 16 -> 1024 channels
- Input capacitance : Cd = 1-5 pF
- Dynamic range : 1 fC – 50 fC
- ToA and ADC
- Target power : 1 mW/ch
- Area 10 mm² (300 mm² final)

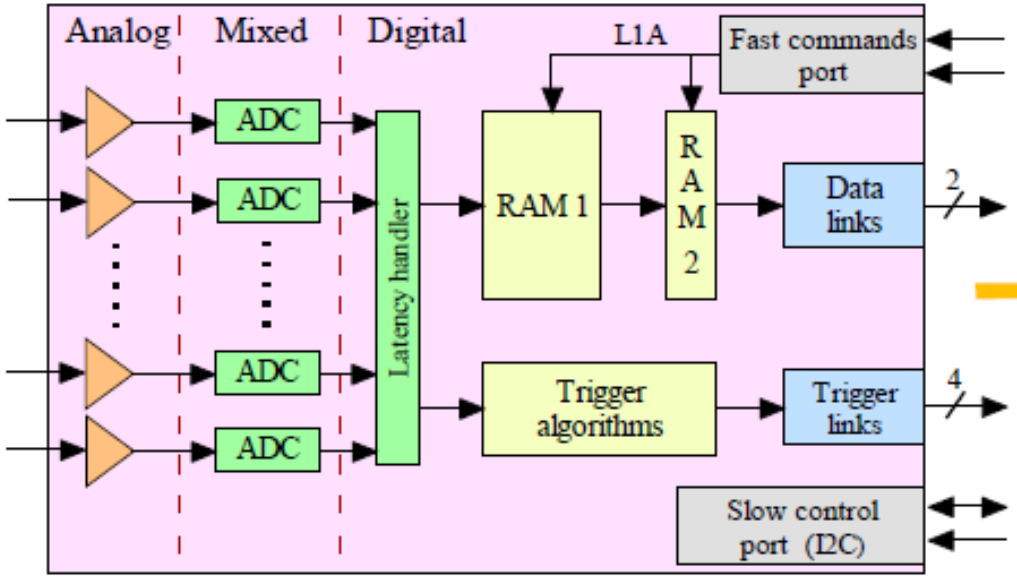
HGCROC

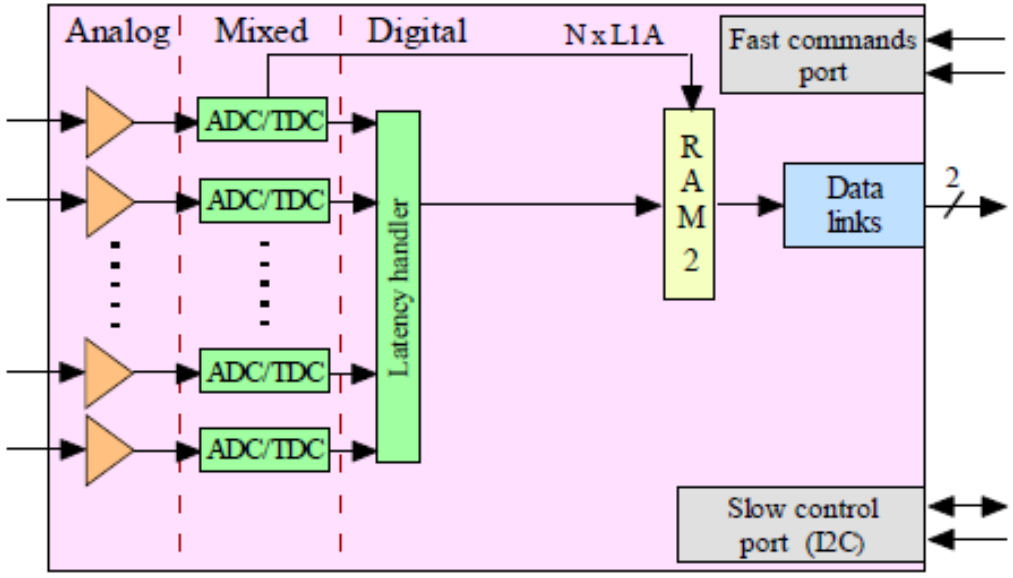
- « 1D chip » 72 (64) channels
- Input capacitance : Cd = 5-50 pF
- Dynamic range : 1 fC – 10 pC
- ToA and ToT
- Target power : 5-10 mW/ch (now 15)
- Area 100 mm²

- SiPM version H2GCROC
- Cd = 100 – 2.5 nF
- Studies for 10 nF groupings
- Can be used by EIC calo

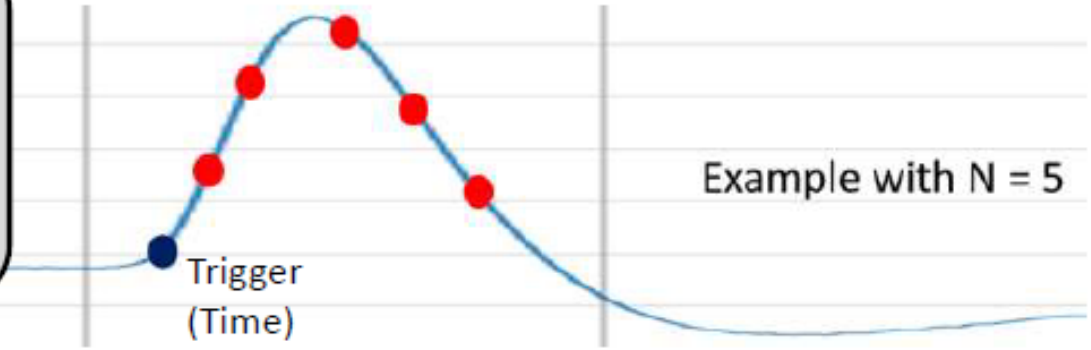
Evolution for EIC readout [F. Dulucq]

- Data streaming : auto-trigger and zero-suppress, 200 MHz clock
- Already done in HKROC (see backup)





- Each event passing the threshold is readout
- Auto-trigger with N "samples" (1 to 7)
- Can be exercised with present HGCROC (multiple L1A-triggers)



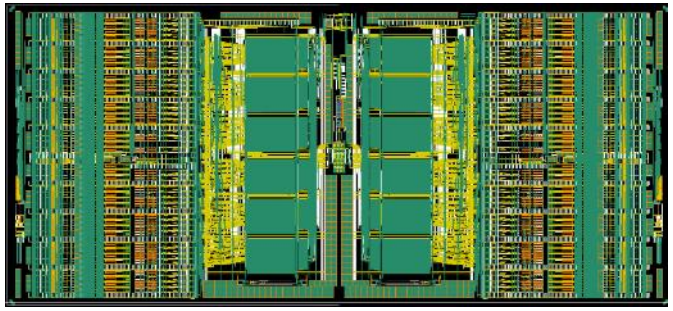
Evolution of H2GCROC : CALOROC1 (2024)

- SiPM readout calorimetry : CMS H2GCROC with EIC readout (200 MHz clock and fast commands)
  - SiPM from 500 pF to 2.5 nF (or 10 nF)
  - ~5-10 mW/channel

- 2 versions : conservative and exploratory
  - Conservative : uses H2GCROC (ADC, TOT) as it is and replaces the backend
  - Exploratory : new analog part (dynamic gain switching).
  - Pin to pin compatible
  - Backend « à la HKROC » : auto-triggered, zero-suppressed
  - 40 MHz internal clocking (ADC, TDCs)

- Channel number tbd : 32 (HKROC) or 64 (HGCROC)
  - Cost issue and pin/pin compatibility with prototypes

HKROC

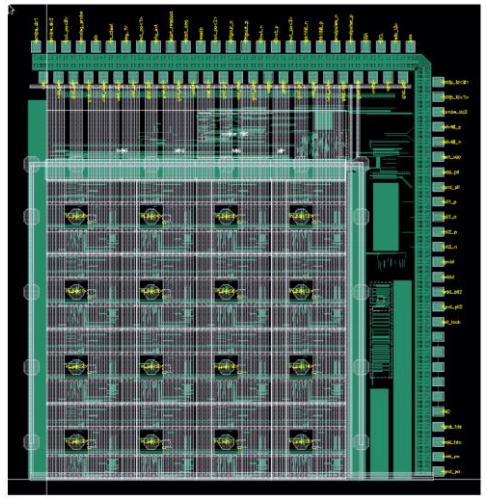


Evolution of EICROC

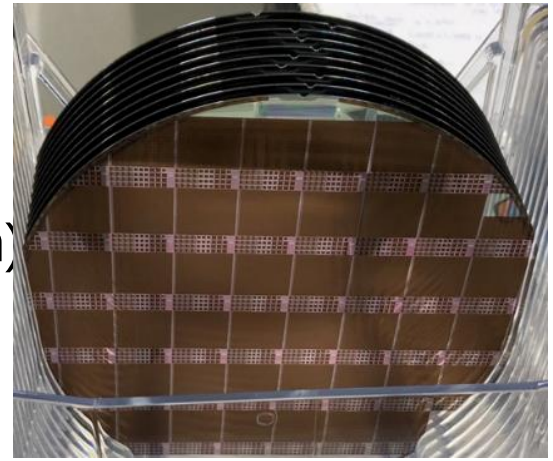
- EICROC0 is a testbeam prototype => sensor characterization
  - Triggered readout
  - all data shipped out : 16 ch * 8 samples ADC + TDC
  - Present power ~2 mW/ch + 4*20 mW « analog probe preamp »
  - ADC power + shaper/driver to be reduced from ~1 mW to 100 µW/ch => EICROC0A

- EICROC1 will address larger dimensions 4x16 or 8x16
  - Address floor planning and power distribution
  - Selective readout : hit + 9 neighbouring channels

- EICROC2 final size : 32x32

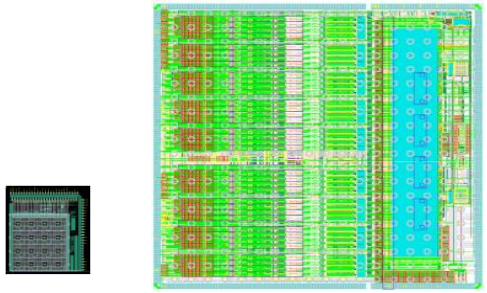


Plans for 2024

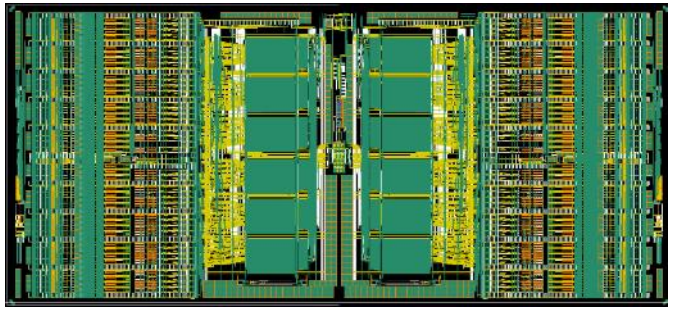


- CALOROC = H2GCROC (SiPM) for EIC
  - Analog part = H2GCROC, backend EIC specific
  - Need to choose HGCROC pin-pin compatibility (64 ch) or HKROC size (32ch)
  - 2 versions : conservative (ADC/ToT), improved (multi-gain)
  - Cost in MPW : 2 * (50 or 100 mm²) * 2 k€ > Engineering run = 250 k€
  - Mid/fall 2024 tbd

HKROC



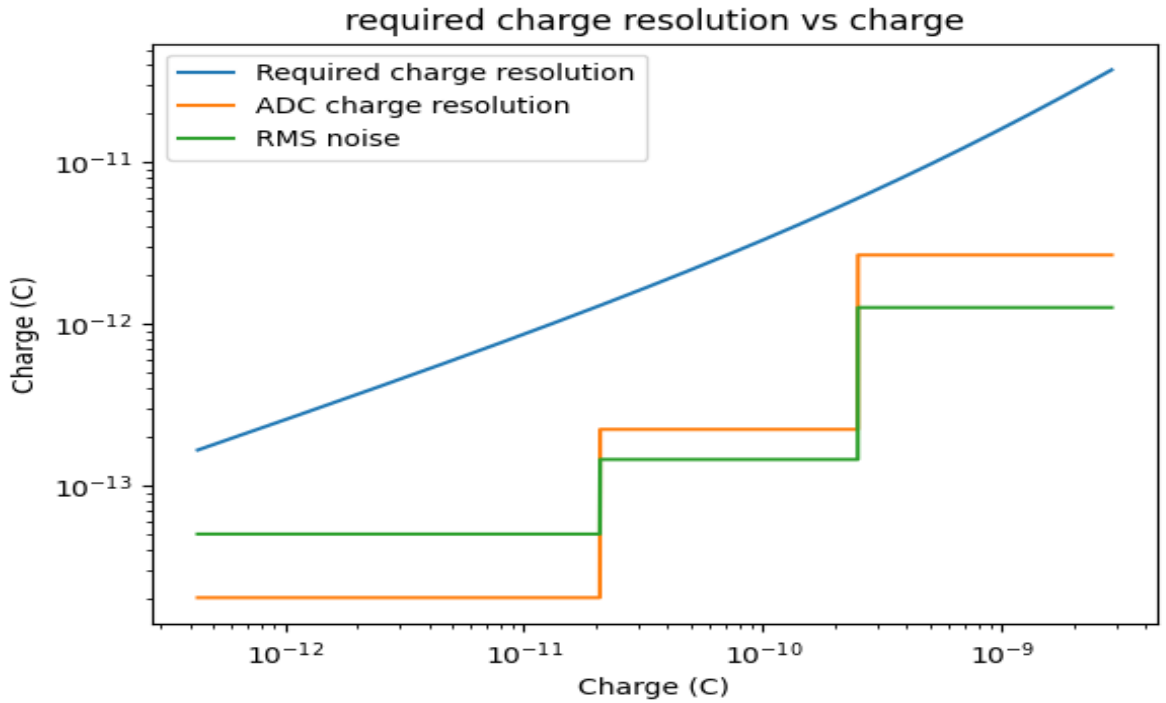
- EICROC
  - Possibly EICROC0A with improved digital noise and low power ADC
  - EICROC1 (4 or 8)*16 channels with possible column « flavours »
  - Probably not yet with EIC readout
  - Area : 20 - 35 mm²
  - Mid/fall 2024 especially if Engineering Run chosen

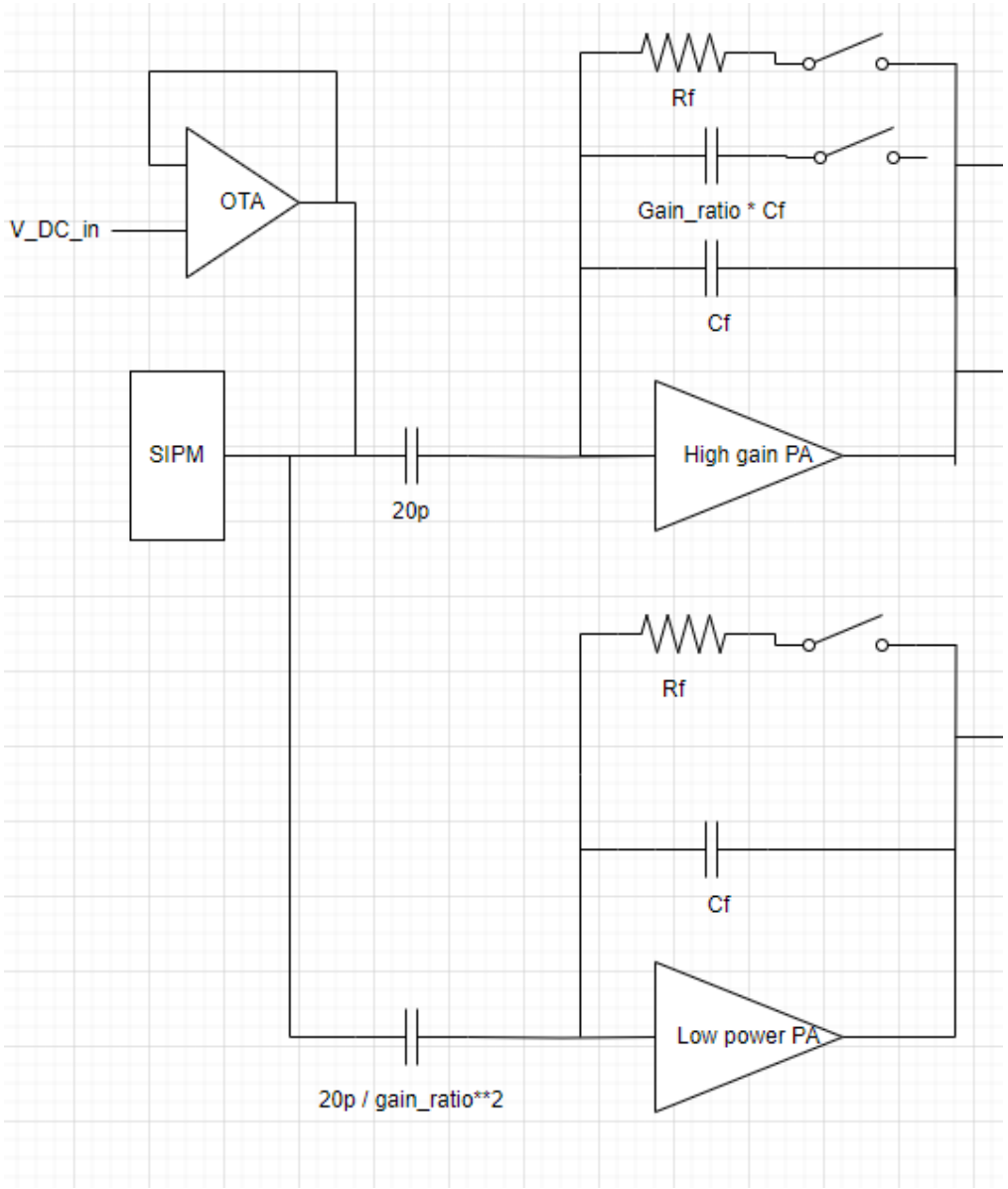


backup

CALOROC1A (also 2024)

- Variant with new analog part
- Dynamic gain switching
- Study of current conveyor and voltage amplifiers « à la spiroc »
- Study low power ADCs (clock gating)
- Will fit (most) FCC needs

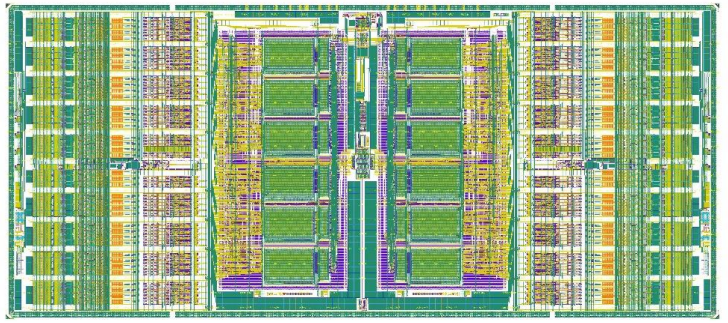


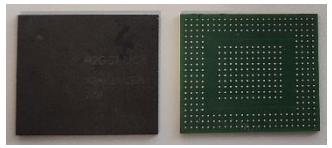


H2GCROC: SiPM version. Requirements

Requirements for H2GCROC (The SiPM version of the ASIC):

- Charge dynamic range : **160 fC to 320 pC**
- Timing accuracy **< 100ps for pulses above 3 MIPs (4.5pC)** for a $C_{det} = 100pF$
- Compensation of the leakage current up to **1mA**
- Radiation resistance up to **300 kRad**
- **Input DAC** to tune the overvoltage

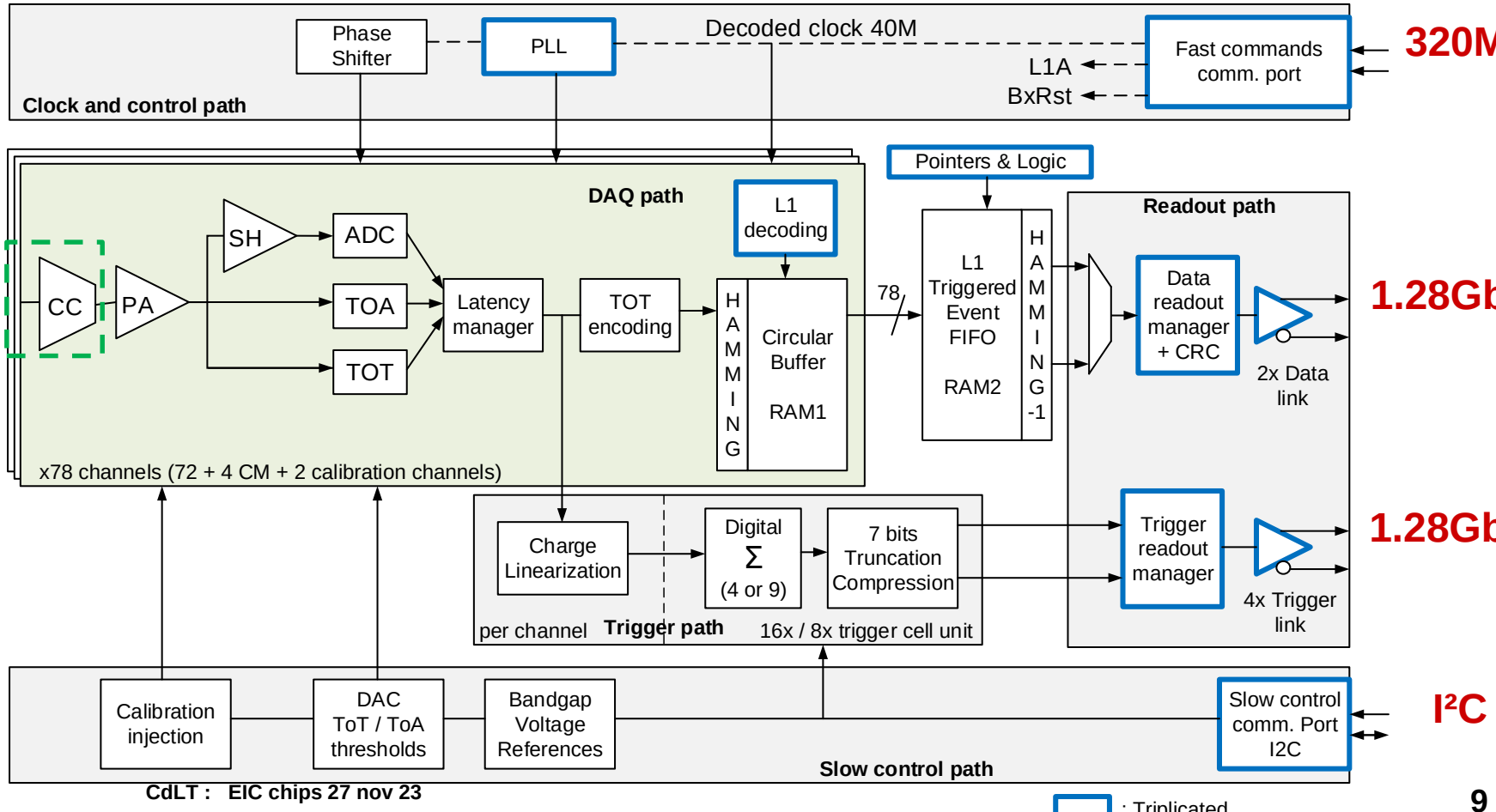




Current Conveyor based on KLAUS chip from Heidelberg UNI.

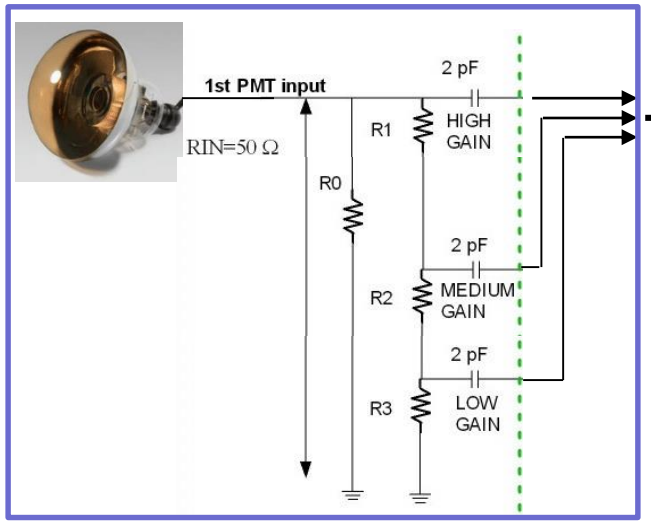
Attenuates the current at the input with 4 bits.

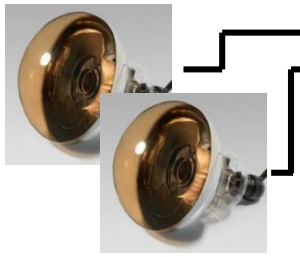
CC gain:
0.025 to 0.375
(step 0.025)

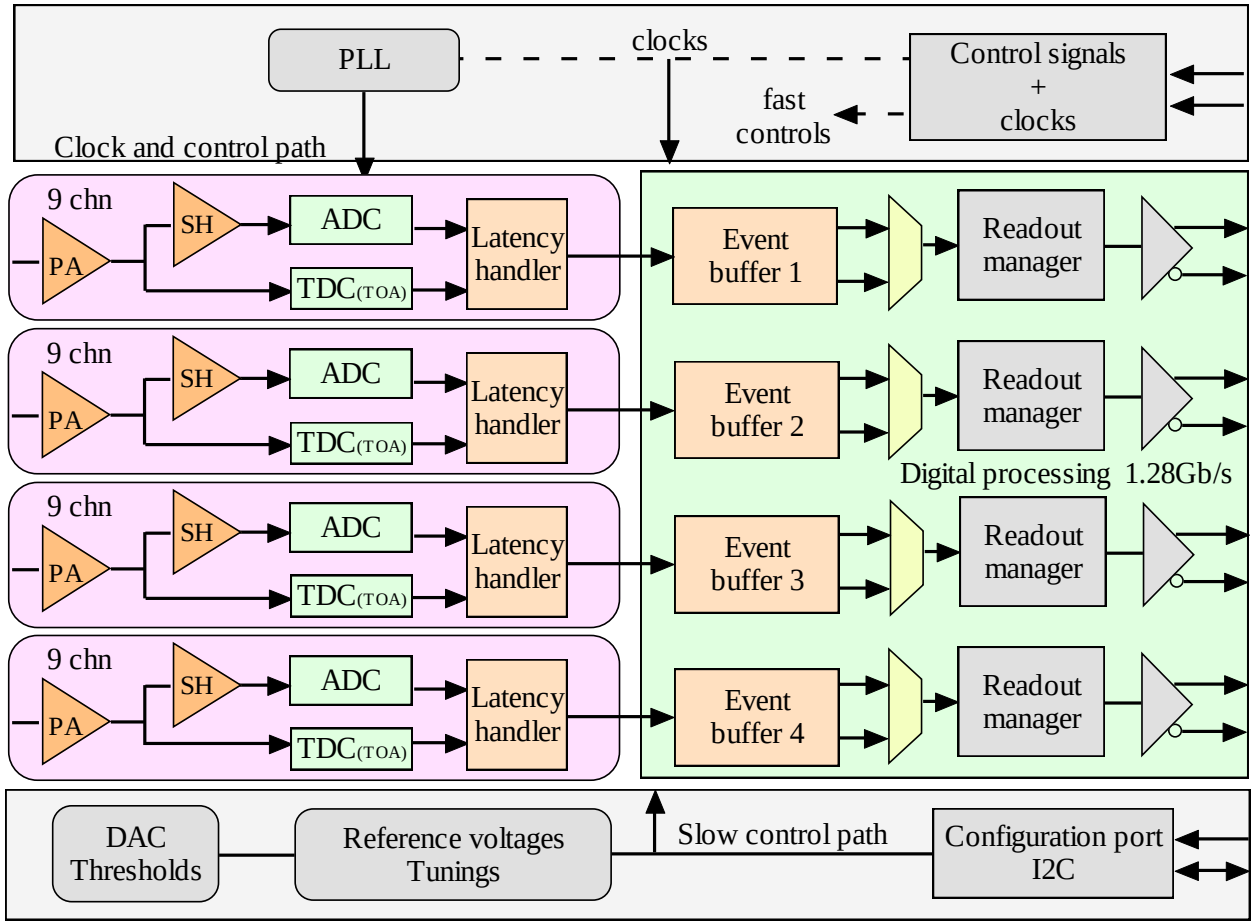


HKROC main features

- HKROC is 36 channels: 12 PMTs with High, Medium and Low gain
  - Or 36 PMTs with one gain



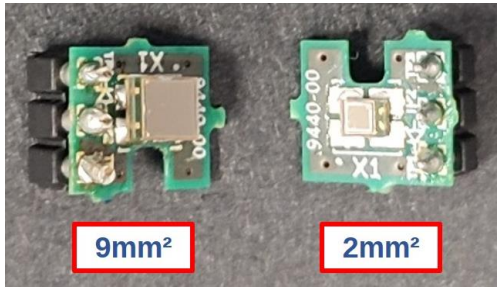


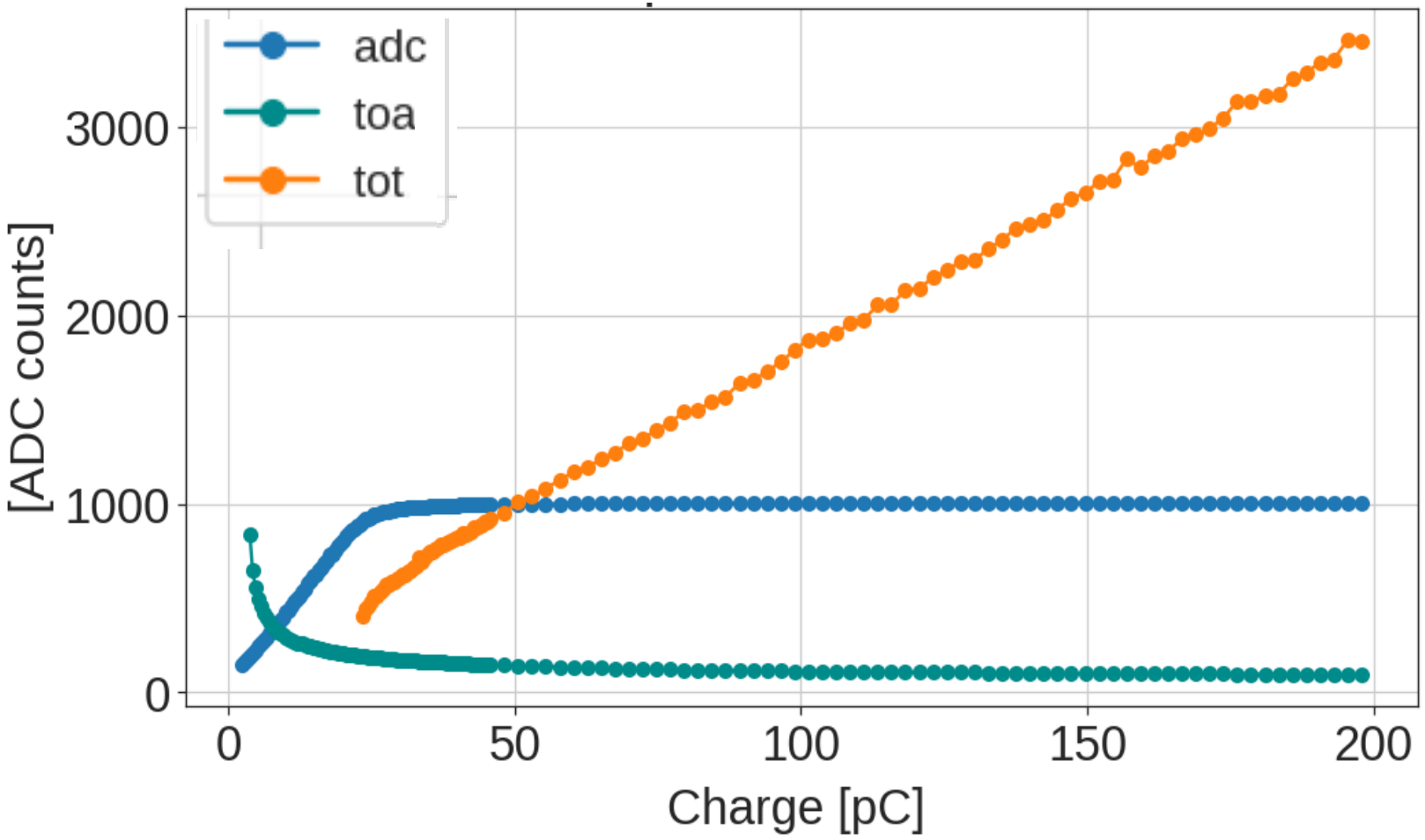


- ASIC in TSMC 130 nm node
- Low power: 10 mW per channel
- Large charge measurement with 3 gains (up to 2500 pC)
- Integrated timing measurements (25 ps binning)
- Readout with high speed links (1,28 Gb/s)
- HKROC is a waveform digitizer with auto-trigger

ADC and TOT readout

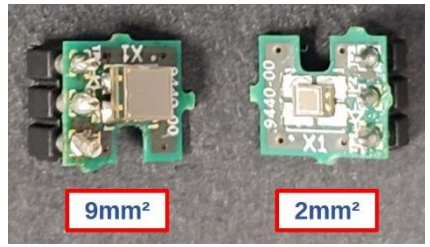
- 16bit dynamic range split in 10 bit ADC and 12 bit ToT
- Tests with 2 sizes of SiPM : 2mm² (120 pF) and 9 mm² (560 pF)



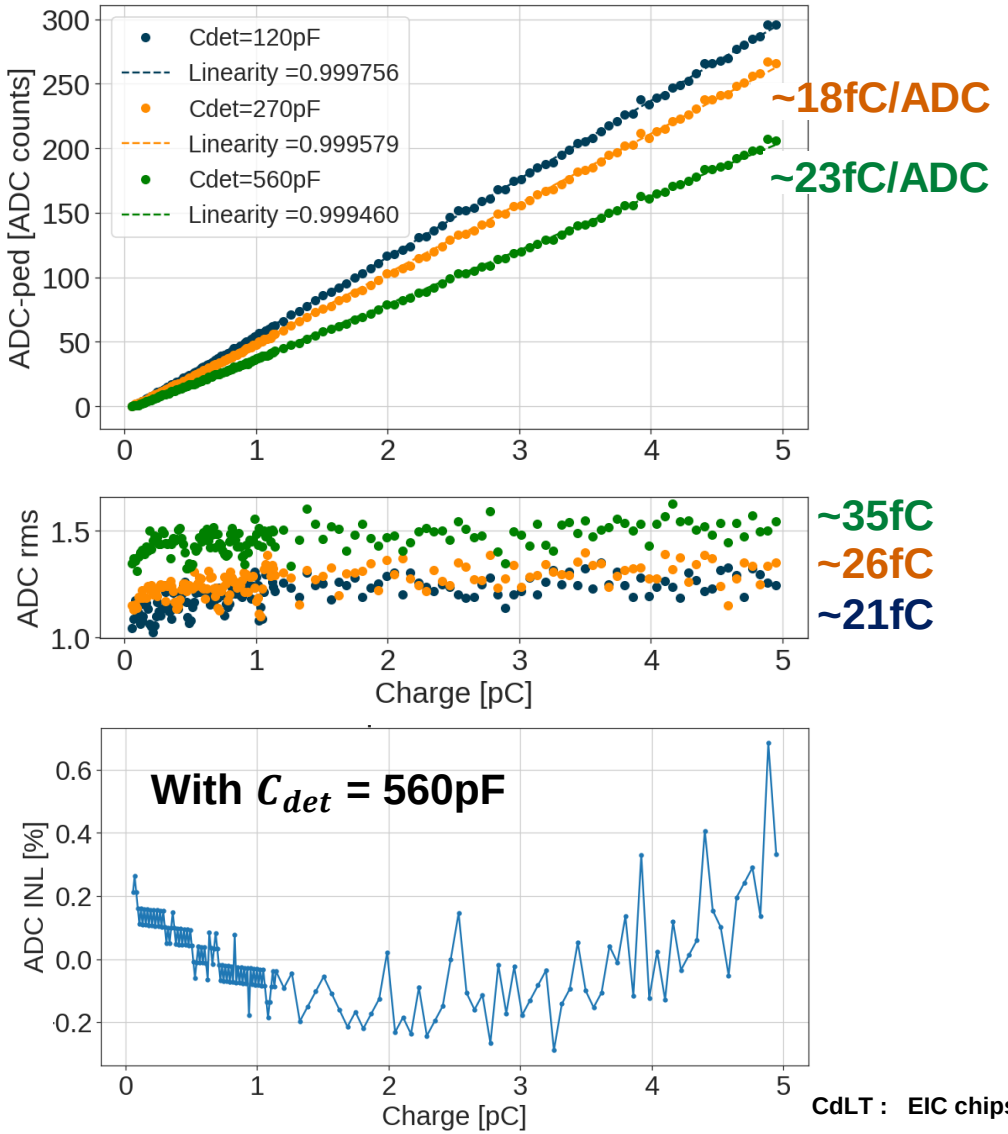


Physics mode : test pulse injection

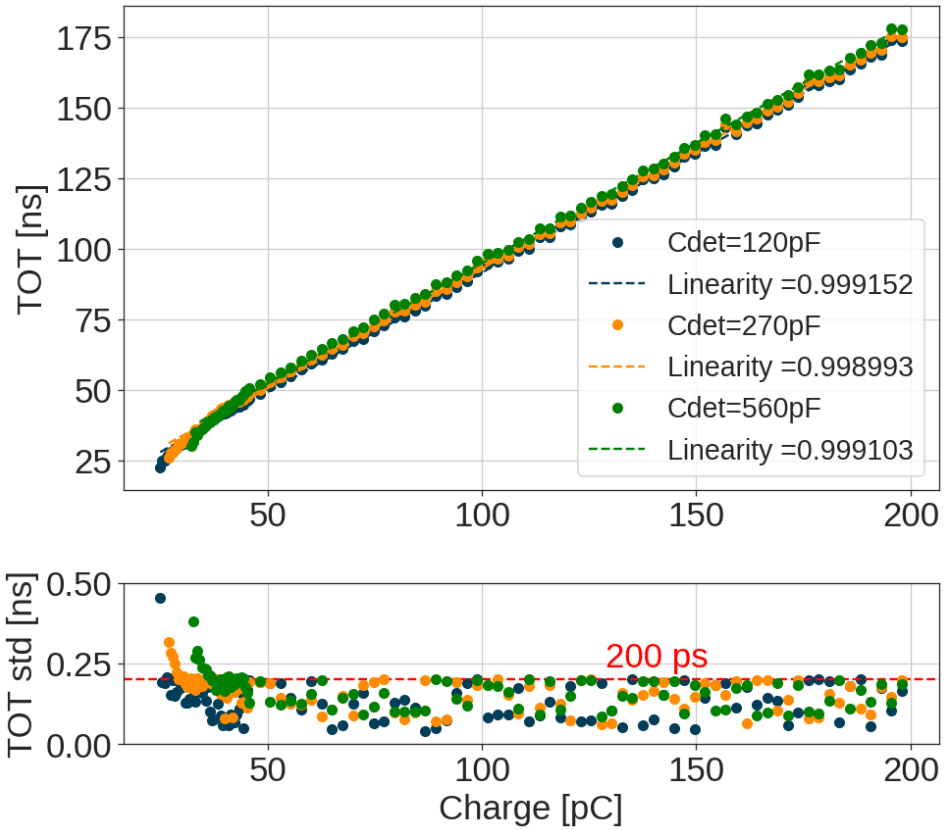
- ~ 60 fC minimum detectable charge efficiently, up to 320pC



Low range injection (ADC):



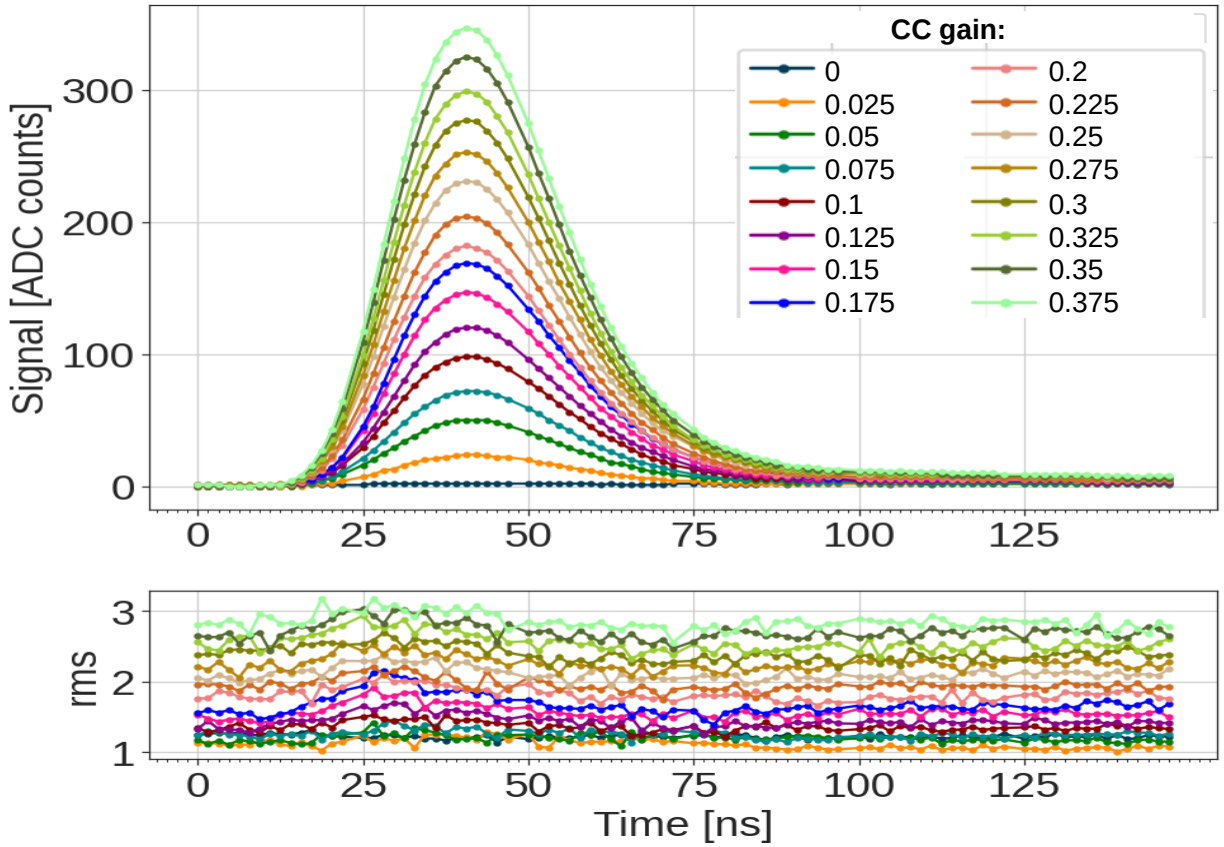
High range injection (TOT):



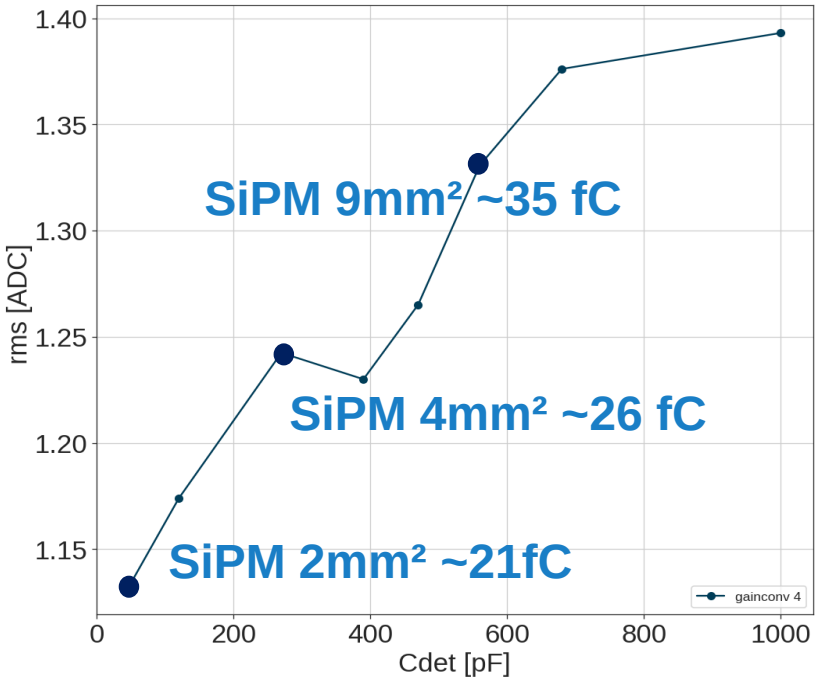
Physics mode

- The CC gain has good performance in linearity.
- The increment in noise is due to the gain configuration and the detector capacitance of the SiPM.

CC gain scan:

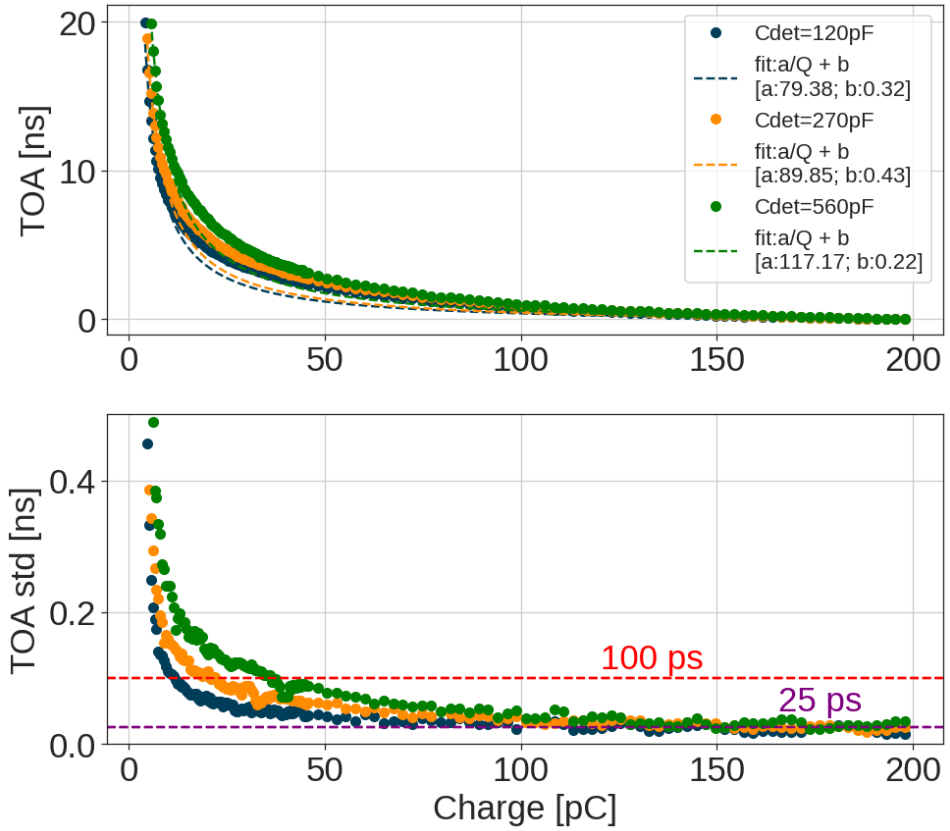


Noise vs C_{det}:



Physics mode : ToA

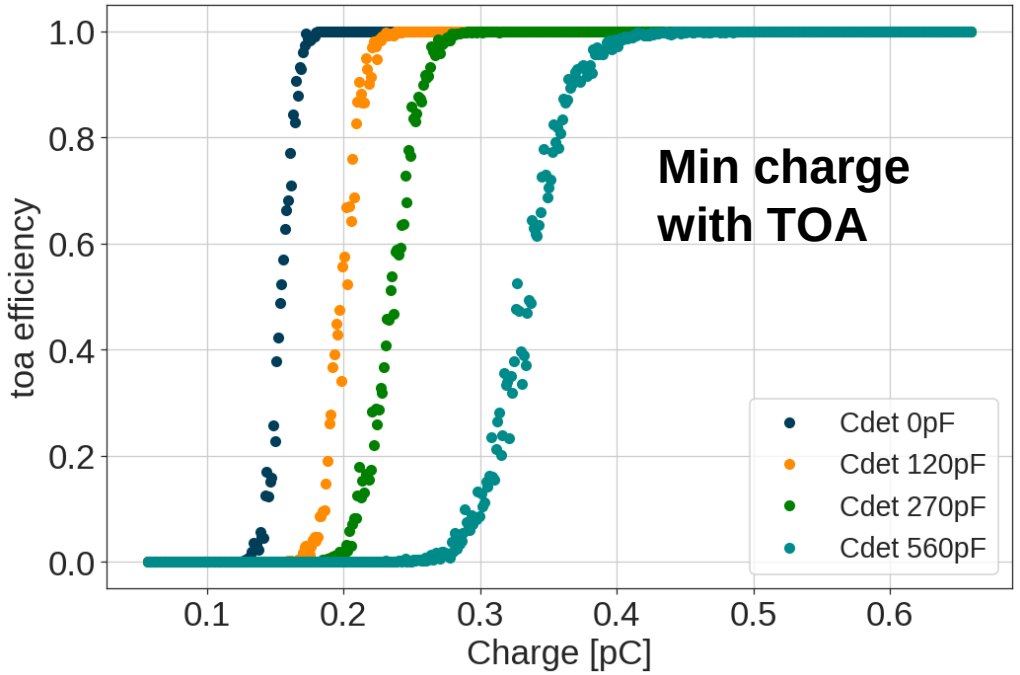
Time of Arrival (TOA) :



- The increase in noise due to larger C_{det} shifts the minimum charge associated with TOA data.
- The thresholds can be adjusted channel-wise for a uniform performance.

Effect of C_{det} on TOA:

- Larger C_{det} produce larger time walk due to the duration of the signal.
- Increasing C_{det} delayed the achievement of a 100ps resolution in charge injection.



Calibration mode: Single-photon-spectrum

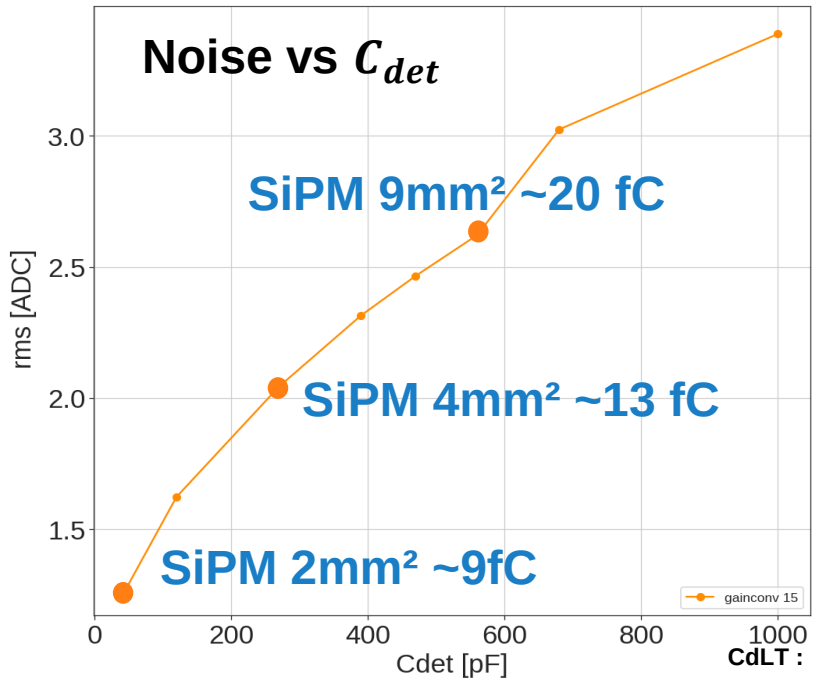
Also a different configuration of the ASIC is necessary to increase the SNR.

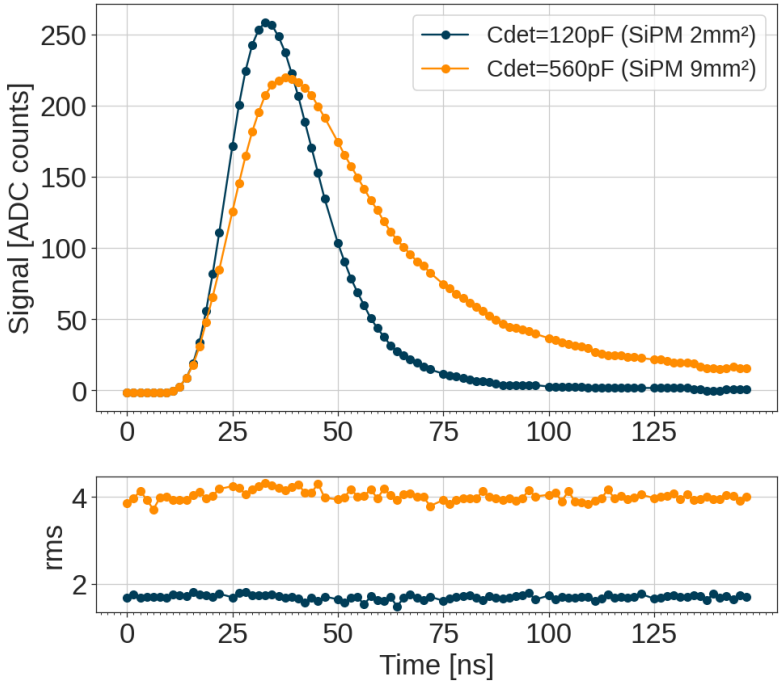
2mm²:

- CC gain attenuation = **0.3**
- $R_f = 16.6\ k\Omega$
- $C_{f\_total} = 600fF\ (C_f + C_{fcomp})$

9mm²:

- CC gain attenuation = **0.375**
- $R_f = 16.6\ k\Omega$
- $C_{f\_total} = \mathbf{300fF}$ (To make the pulse shorter)



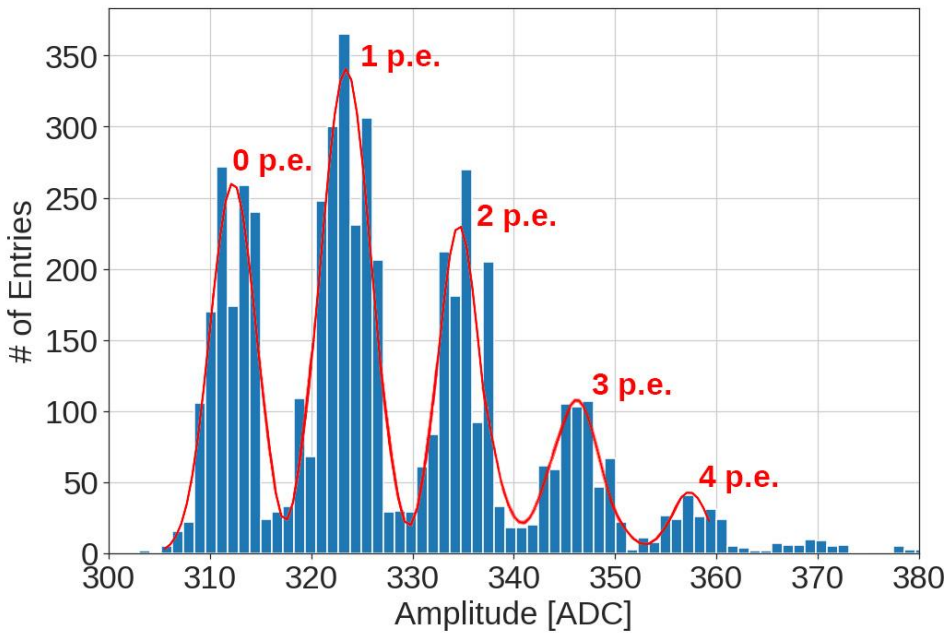


*Noise measured with the same configuration parameters for all C_{det}.

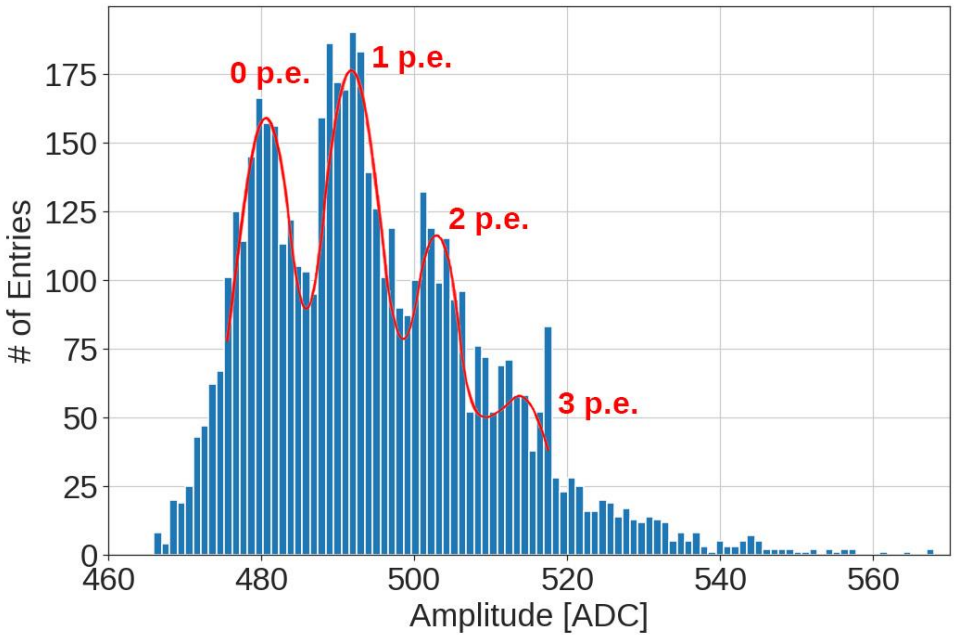
- The increment in noise is due to the detector capacitance of the SiPM.
- SNR can be improved with the gain configuration.

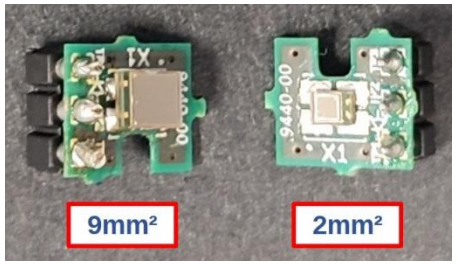
Calibration mode: Single-photon-spectrum

- **2mm²:**



- **9mm²:**



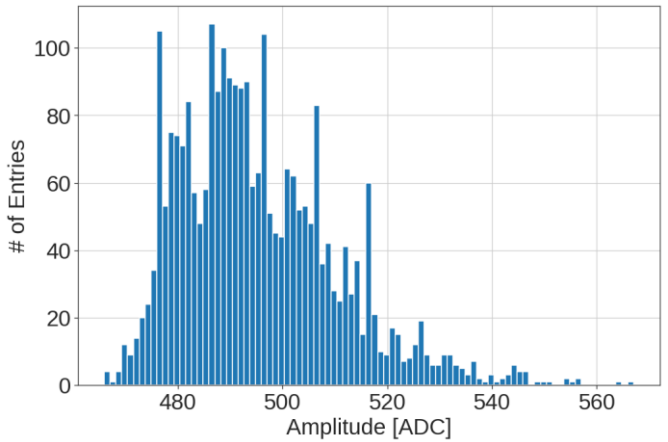


***Extra step for 9mm² SiPM calibration:**

The large C_{det} of the 9mm² SiPM produce an increment of DNL and make it harder to see the photon separation.

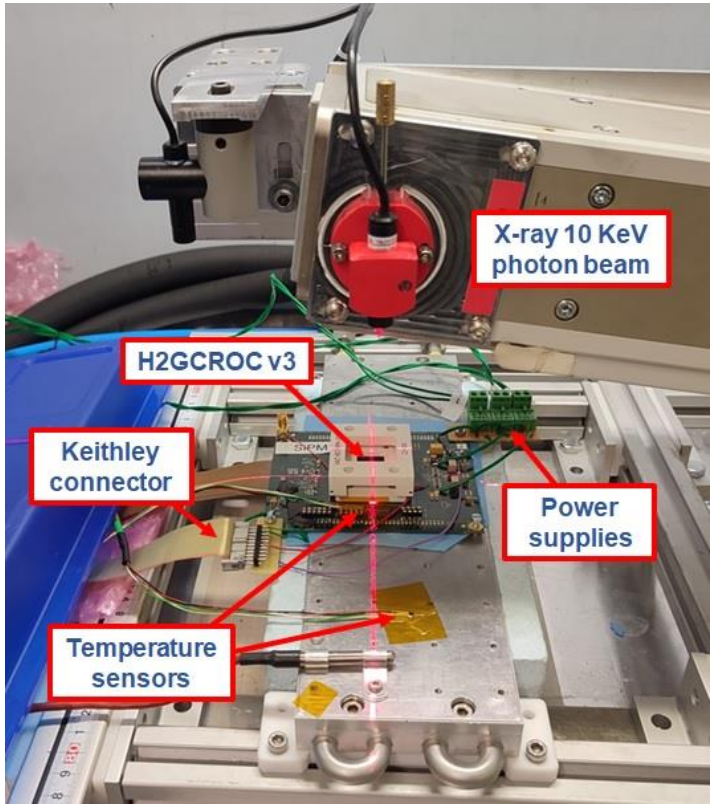
The DNL can be mitigated taking data with different pedestal levels using the ASIC to move the pedestals (*Trim_inv* parameter). SPS is clearer after aligning the data.

Without DNL correction:

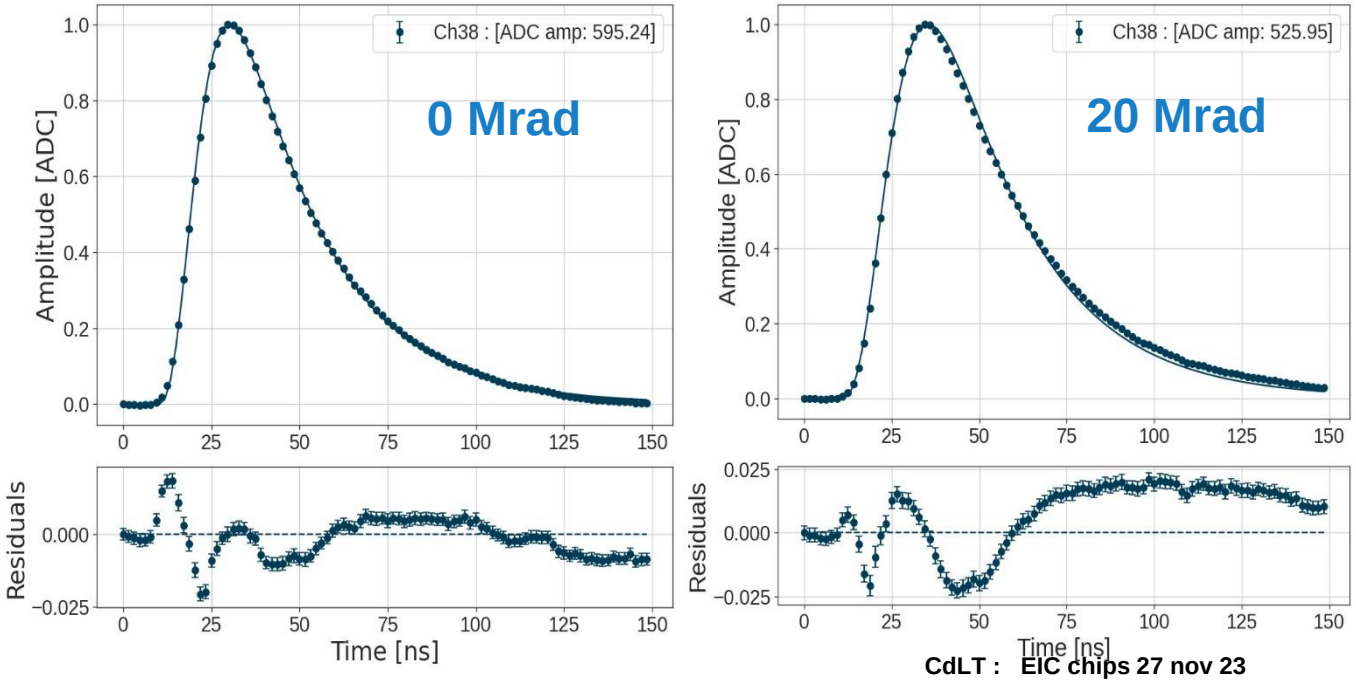


Irradiation campaigns

- Power consumption, ADC & TDC performance, noise, links stability, etc. tested during irradiation
- **TID irradiation tests in both ASIC versions.**
- **Heavy ion and Proton irradiation in the Si version of the ASIC**
  - Increase on triplicated parts for HGCROC3b



Stability of ADC measurements after 20Mrad:



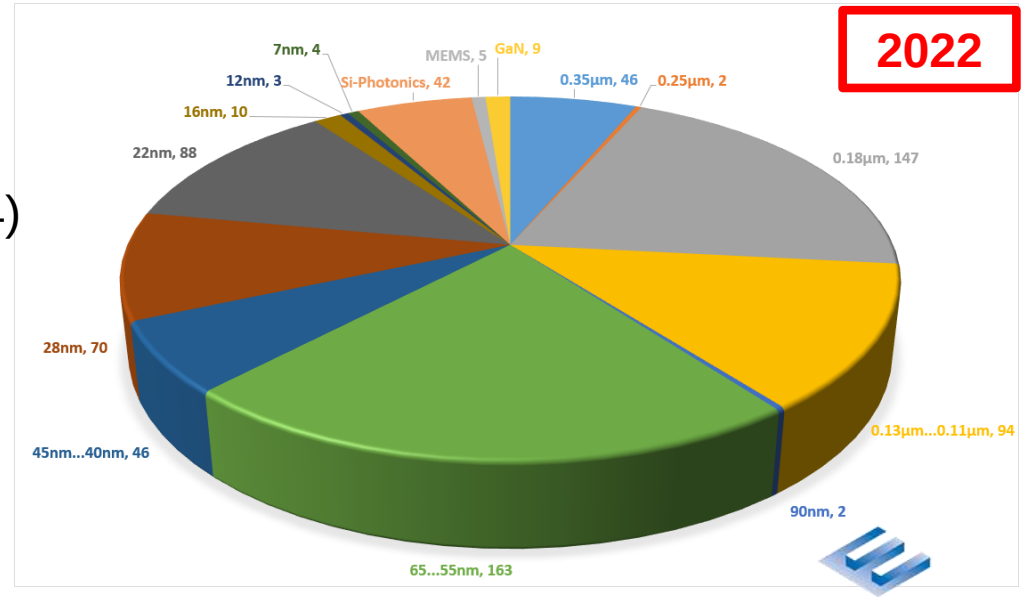
- **H2GCROCv3** has proven to be **radiation tolerant up to 20 Mrad** at room and -5°C with good ADC, TDC and PLL measurements.

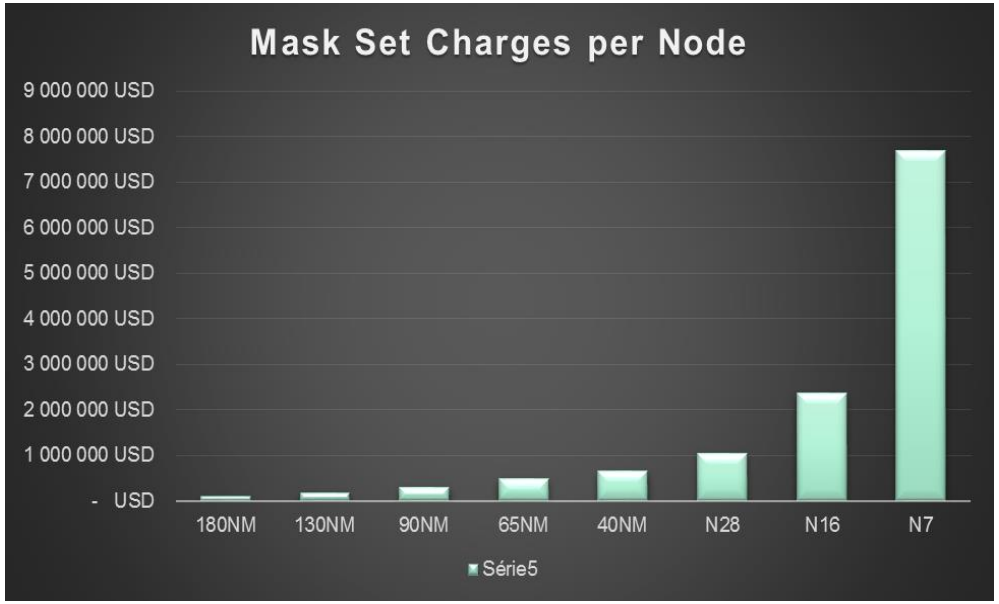
Technology choice for mixed signal ASICs

- TSMC 130nm : mixed signal, cheap
  - Very mature technology with good analog performance
  - 2.5 k€/mm² MPW, 300-350 k€/engineering run (20 wafers C4)
  - Perenity ?

- TSMC 65 nm : mixed signal, main stream
  - ~2-3 times lower power in digital, similar in the analog (compared to 130n)
  - 5 k€/mm², 700-800 k€/ engineering run

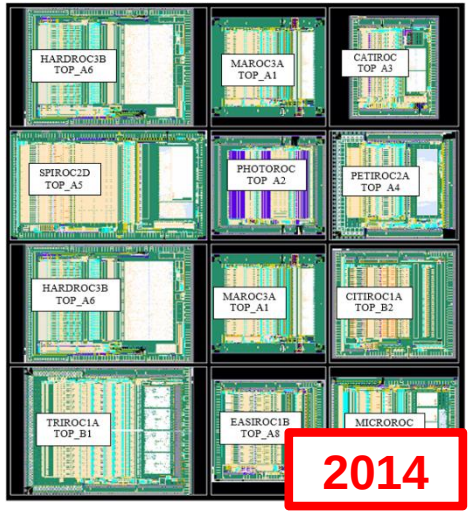
- TSMC 28 nm : digital oriented
  - High density integration (pixels)
  - High performance, lower power digital, similar in the analog
  - 10 k€/mm², 1-1.5 M€/ eng run



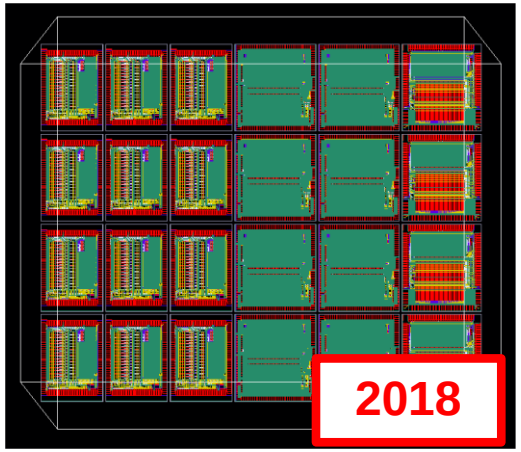


OMEGA Engineering runs

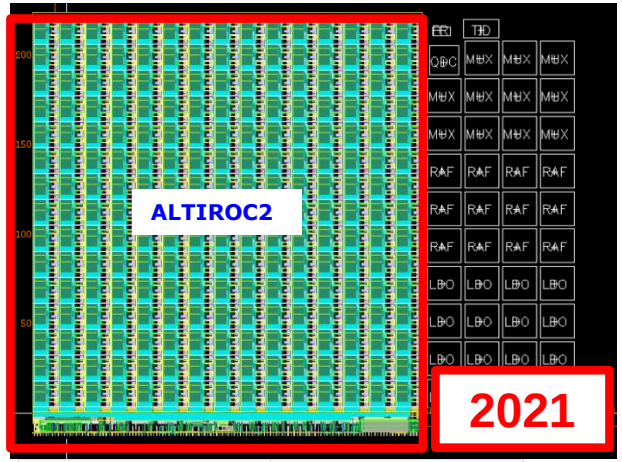
- 8 engineering runs in 9 years !
  - AMS SiGe 0,35um 2014, 2016, 2018
  - TSMc 130nm : 2019, 2020, 2021, 2x2023
  - Cost : 200-300 k€, shared between projects



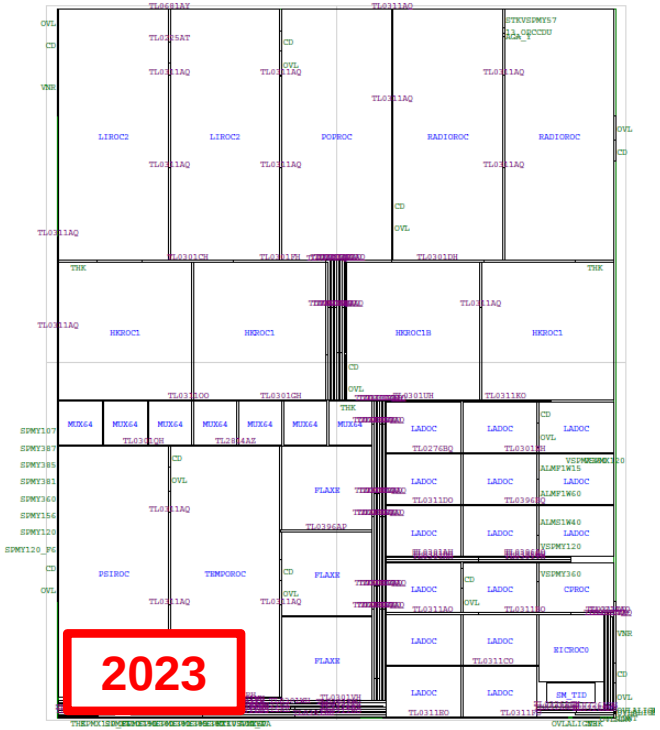
2014



2018



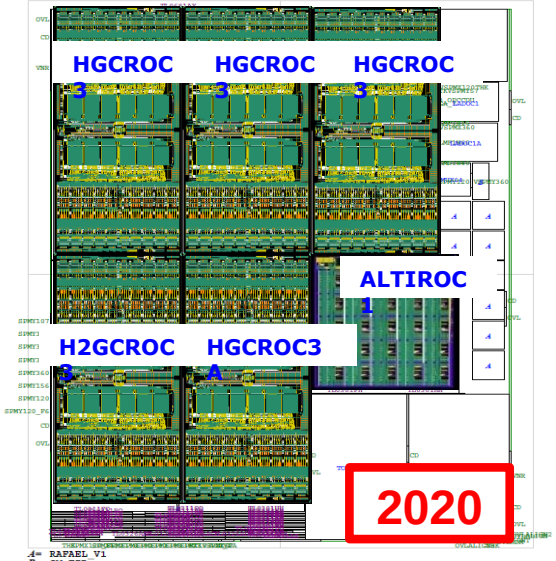
2021



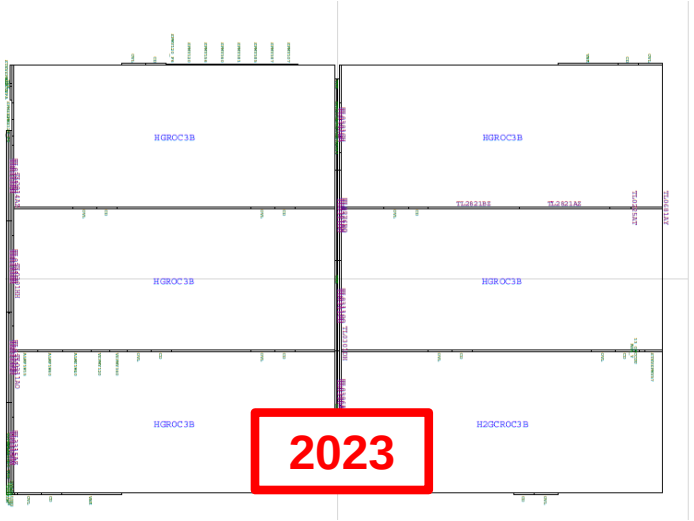
2023

2016

2019



2020



2023