ePIC uRWELL tracker electronics discussion

MPGD-DSC uRWELL-Trackers meeting

12/21/2023

Basic requirement from ePIC-mRWELL electronics

1. Need to support detector capacitance (including capacitive sharing r/o). Preferably having the possibility of selecting multiple capacitance ranges.
2. Better timing resolution / peaking time as MPGDs will be crucial for background rejection (< 20 ns ?)
   - Sharp ~200 ps electron spike with ~ 50 ns ion tail in uRWELL.
3. Need to support EIC signal rate (slide 2).
4. Streaming readout (my personal preference due to flexibility in using higher level offline trigger for Physics analysis). However, it needs to be compatible with DAQ software.
   - Doesn't hurt having the option to operate in triggered mode.
5. Low noise level (< 20 e-/pF , based on SAMPA for sPHENIX TPC).
6. Gain (30 mV/fC ?)
7. Low power consumption (<20 mW/channel ?) to avoid heating . Also helps with reducing the noise

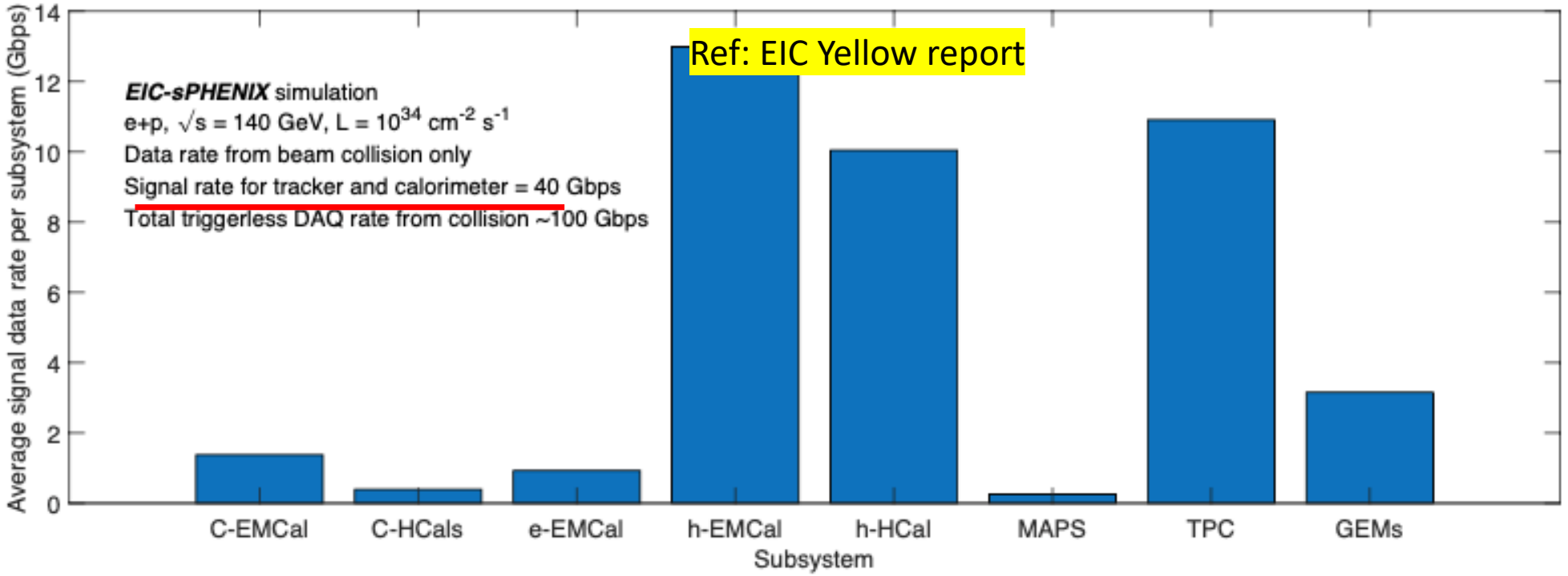

Figure 10.6: Signal data rates from tracking and calorimetric detectors from EIC collisions via full detector GEANT4 simulation of an EIC detector concept based on sPHENIX [1417, 1419], which also applies to the reference EIC detector as in this report. Zero-suppression and realistic data format based on sPHENIX prototyping are assumed in this estimation. The overall tracker data rate is 40 Gbps. The estimated rate with PID detector and moderate detector noise would reach 100 Gbps for full experiment. Please note that the backgrounds, e.g. beam gas interaction, excessive detector noise, synchrotron photon hit rate, may dramatically increase the data rate in some detectors, but they are not included in this plot and they will be discussed in Section 10.4.

Characteristics of various chips available for gaseous detector readout

	SAMPA	VMM	TIGER	DREAM	AGET	AFTER
Architecture	Front-end + ADC + DSP	Front-end + S&H + discri + 3xADC	Front-end + S&H + discri + TDC + ADC	Front-end + analog memory		
	Analog characteristics					
Number of channels	32	64	64	64	64	72
Input dynamic range	66/500 fC	0.1-2.0pC	2.0-50 fC	50-600 fC	120 fC - 10 pC	120-600 fC
Peaking time range	160-300 ns	25, 50, 100 and 200 ns	60 ns (TDC), 170 ns (ADC)	50 ns - 1 μs	50 ns - 900 ns	100 ns - 2 μs
Full signal occupancy	550 ns					
Polarity	+/-	+/-		+/-	+/-	+/-
Detector capacitance range	18.5 pF/40-80 pF	200pF	up to 100pF	200 pF		<30pF
Noise level	600/900 e$\check{}$07b	300 e$\check{}$07b at 9 mV/fC	up to 2000 e$\check{}$07b	610 e$\check{}$07b + 9 e$\check{}$07b/pF	580 e$\check{}$07b + 9 e$\check{}$07b/pF	370 e$\check{}$07b + 14.6 e$\check{}$07b/pF
Sensitivity/Gain	20-30/4 mV/fC		12.4 mV/fC (TDC), 11.9 mV/fC (ADC)			120 fC/mV
Remarks			CR-RC shapers			
	Digital characteristics					
Sampling frequencies	10-20 MHz	200 MHz	1-40 MHz	1-50 MHz	1-100 MHz	1-100 MHz
ADC resolution	10-bit	10-bit	10-bit (Wilkinson)	No ADC	No ADC	No ADC
TDC time resolution		8-bit + 12 global	5 ns			
Remarks	10 MS/s			Internal trigger	Internal trigger	
Data treatment functions	On-board DSP	none	none			
Data bandwidth	11x320 Mbit/s	<1 Gbit/s	1.28 Gbit/s (triggerless)			
Streaming readout capacity	3.4G bit/s		Readout on			
			internal trig., programable thres.			
	Other information					
Die size	9.6x9.0 mm^2	15.3x8.3 mm^2	5×5 mm^2			7.8 x 7.4 mm2
Package size	TFBGA 15x15 mm^2	400BGA				28 x 28 mm
Power consumption	20 mW/ch	10 mW/ch	12 mW/ch @ 3.3V	10 mW/ch	10 mW/ch	10 mW/ch
Technology	130 nm CMOS	130 nm MOSFET	110 nm CMOS	350 nm AMS CMOS	350 nm AMS CMOS	350 nm AMS CMOS
Remarks						