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SALSA ASIC for the EPIC MPGD readout

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MPGD-DSC meeting

07/12/2023

Introduction

SALSA specifications

First prototype results

Prospects

SALSA CHIP DESIRED SPECIFICATIONS

Versatile front-end characteristics

- 64 channels
- Large input capacitance range, optimized for 50-200 pF, reasonable gain up to 1nF
- Large range of peaking times: 50-500 ns
- Large gain ranges: 0-50 to 0-5000 fC
- Large range of input rates, up to 100 kHz/ch with fast CSA reset (limit assumed for EPIC: 25 kHz/ch)
- Reversible polarity
- Front-end elements can be by-passed

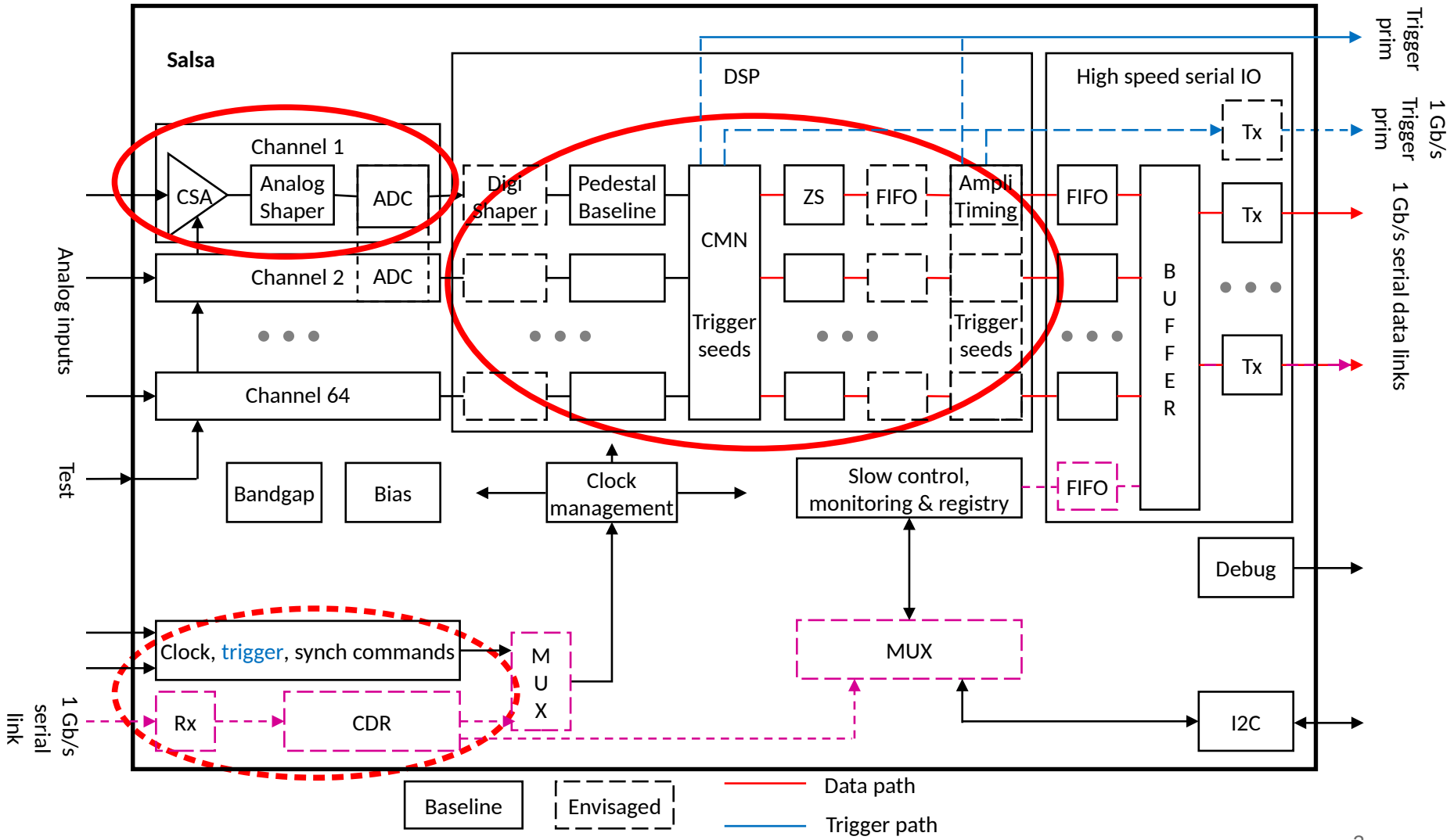
Digital stage

- Fast sampling ADC for each channel on 12 bits (> 10 effective bits) at up to 50 MS/s
- Possibility to double rates by coupling pairs of channels
- Integrated DSP for internal data processing and size reduction, treatment processes to be selected according to user needs
- Continuous readout compatible with streaming DAQ foreseen at EIC, triggered mode also available
- Several 1 Gb/s output data links

General characteristics

- ~1 cm² die size, implemented on modern TSMC 65nm technology
- Low power consumption ~ 15 mW/channel at 1.2V
- Radiation hardened (SEU, TID), working at 2T magnetic field

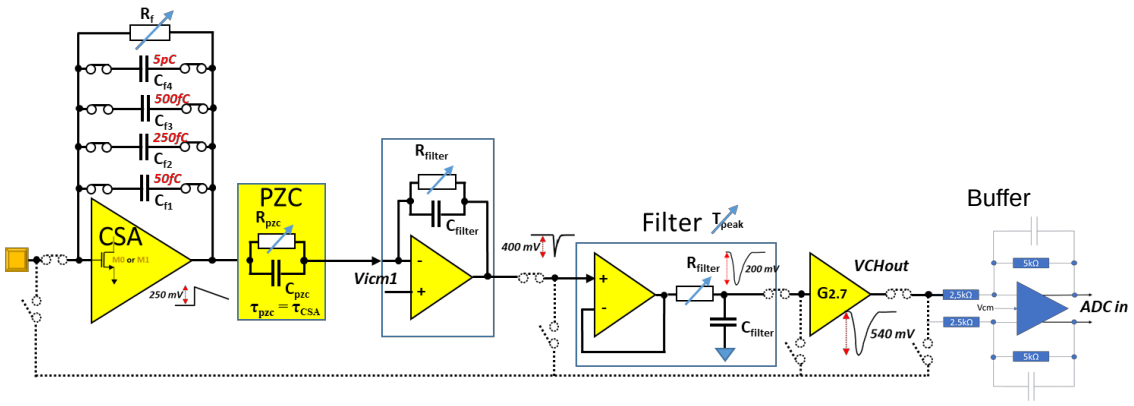
Preliminary design of SALSA



SIGNAL AMPLIFICATION AND DIGITIZATION

Front-end stage

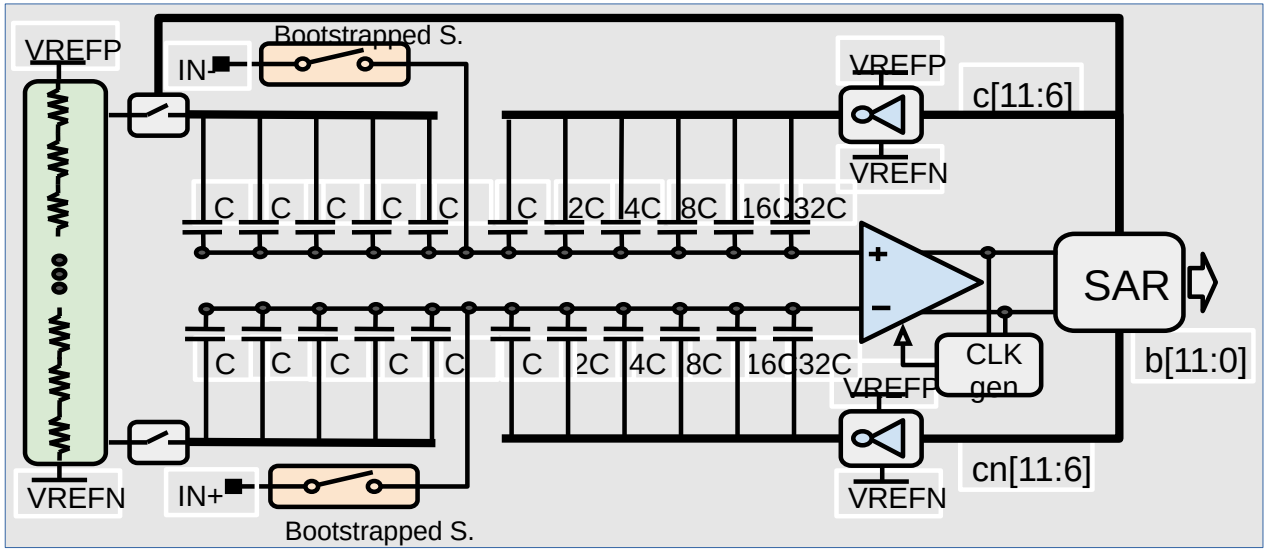
- Charge Sensitive Amplifier + Pole-Zero Cancellation + shaper
- 4 gain ranges from 0-50 fC to 0-5 pC
- 8 peaking times 50 to 500ns
- 2 input transistor sizes
- 2 polarities
- Integrated anti-saturation circuit
- Integrated test pulses



Scheme from P. Baron

ADC block

- 12 bits 5-50 MS/s SAR ADC
- Expected 10-11 ENOB bits



Scheme from H. Hernandez

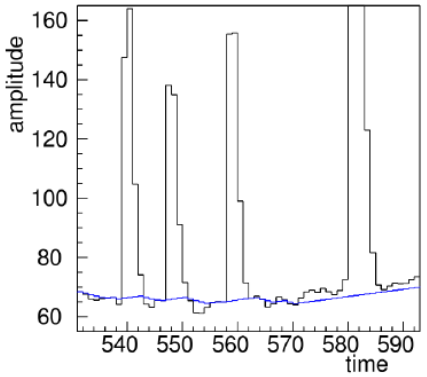
DSP DATA PROCESSING, PRELIMINARY VERSION

General remarks

- Data processing, reduction and formatting from ADC values to output links
- Each process can be deactivated individually by user
- Process parameters through ASIC registers
- Part of codes from SAMPA chip
- Considered processes still under study, suggestions welcome !

Baseline corrections

- Pedestal subtraction with fixed value per channel
- Common mode correction to reduce common noise impact
- Baseline slope following algorithm



Plot from SAMPA doc

Digital shaping

- Cancellation of signal tail if necessary

Zero suppression

- Keeping samples above fixed thresholds, possibly neighbor ones
- Different data format between ZS and non-ZS samples

DSP DATA PROCESSING, PRELIMINARY VERSION

Feature reconstruction

- To further reduce data flux
- For instance peak finding algorithm: amplitude + time + TOT extraction

Trigger management

- Samples selected to be extracted when trigger signals received
- Trigger primitives generation when samples above threshold
- Nature of trigger primitives to be defined (logic signal, data on specific fast link, etc...)

Data monitoring and calibration

- Specific fast commands to generate calibration data (non-ZS, with test pulses, etc...)
- Software scaler per channel for occupancy evaluation

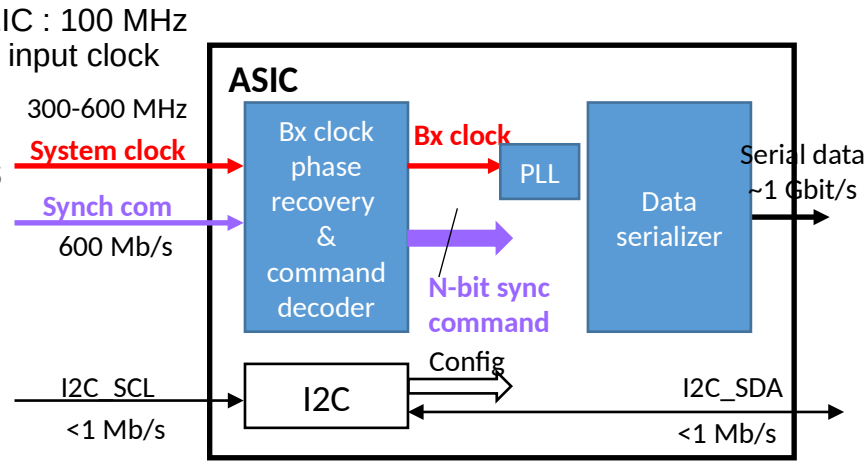
Data formatting and buffering

- Formats for ZS and non-ZS sample data, featured data, monitoring data
- Output data flux segmented in packets which will contain all kinds of data
- Packet identification by numbering and timestamps
- Packet buffering and transmission over 1 or several Gbit/s links
- Generation of error packets in case of troubles

CLOCK, FAST COMMAND AND SLOW CONTROL INPUTS

Traditional way

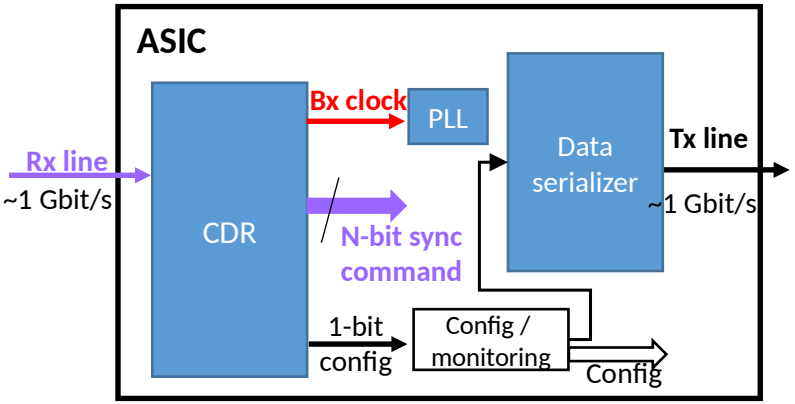
- 1 differential input for clock
- 1 differential input for fast commands: T_0 synchronization, calibration triggers, event triggers (non-streaming readout mode), etc...
- 1 SDA + SDC I2C input for slow control and configurations
- Will be implemented in SALSA

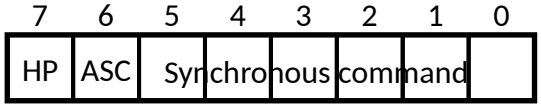


Schemes from I. Mandjavidze

Single encoded line grouping all inputs

- High speed 1Gb/s differential input which carry clock + fast commands + slow-control
- Internal CDR in SALSA to extract the different parts
- 8 bits every 10 ns (EIC): 6 bits for fast command ID, 1 bit for slow-control, 1 parity bit
- Slow control output through data output line
- Simplify connectivity: 1 diff input for everything instead of 4
- Possibility to implement this in SALSA in parallel with the traditional way
- May be proposed to some other readout ASICs in EIC as well

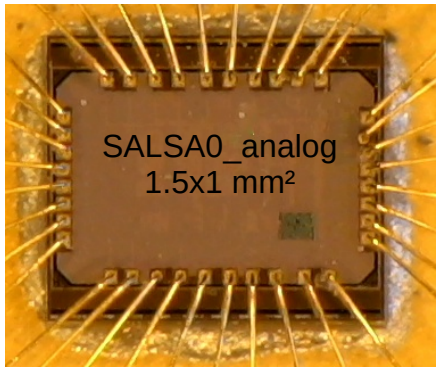




TIMELINE OF THE PROJECT

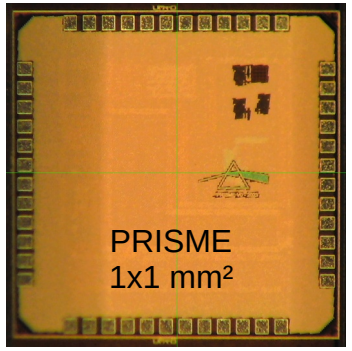
The different steps

- 2020-22: Discussions and reflections on the project
- 2022-23: SALSA0 prototypes to study first designs
  - SALSA0_analog featuring 4 front-end channels
  - SALSA0_digital featuring an ADC block
- 2023: PRISME prototype to test PLL block designed at IRFU + first version of general services
- 2023-24: SALSA1 prototype to test full front-end + ADC chains
- 2023-25: SALSA2 prototype to test fully featured ASIC including DSP, but with ~32 channels
- 2025-26: SALSAf as pre-serial prototype with nominal number of channels



Status of prototypes

- SALSA0 prototypes submitted in November 2022 and January 2023, tests of analog proto in progress, tests of digital ones started
- PRISME prototype, received in December 2023, under packaging, tests to be started this month or beginning of January
- SALSA1 design ongoing, submission foreseen 1st trimester of 2024
- Reflections on SALSA2 architecture and DSP data processing ongoing, submission foreseen beginning of 2025



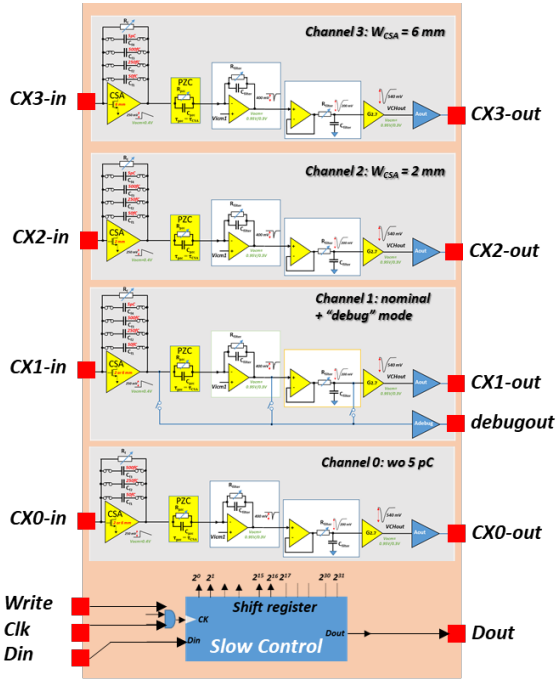
TESTS ON FRONT-END STAGE

SALSA0_analog prototype

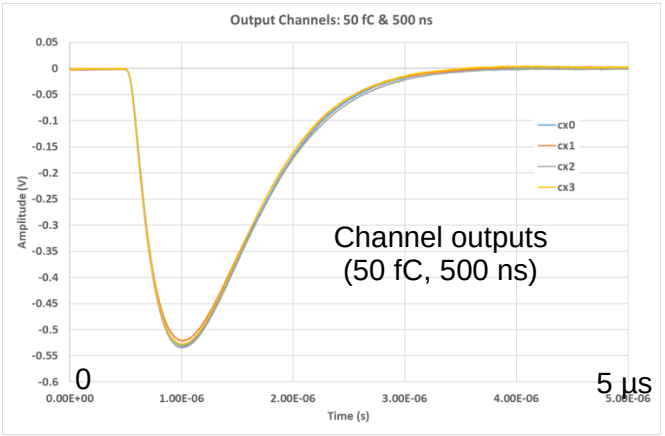
- 4 front-end channels with slight differences between them
- CX1 channel with debug output for monitoring
- CX0-2-3 with different input transistors, CX0 without 5 pC gain range

Preliminary results

- Test-bench with selectable input capacitance, input signal generation with configurable amplitude and rate, programmable oscilloscope, etc...
- Almost all configuration parameters (gains, peaking times, anti-saturation,...) were tested and work well
- Measurements in agreement with simulations: bias currents, power consumption, DC values, etc...
- Some discrepancies concerning transfer functions and noise levels especially at 50 fC gain range
- Origin due to parasitic resistances in the chip. Now understood and reproduced in simulations. Already corrected in the CSA design for SALSA1
- Further tests in progress, in particular vs temperature

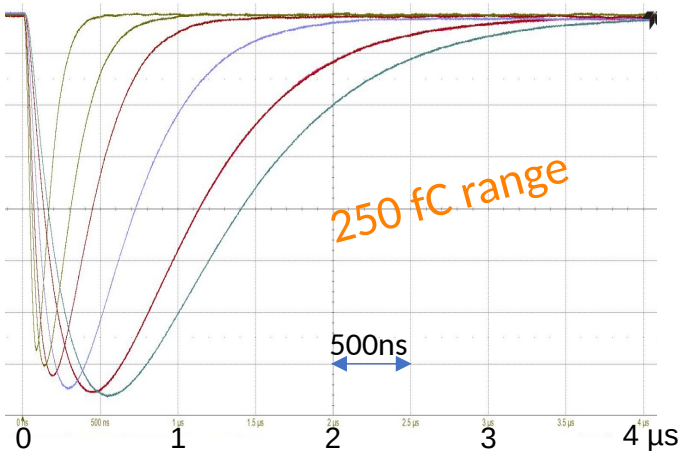


Scheme from P. Baron

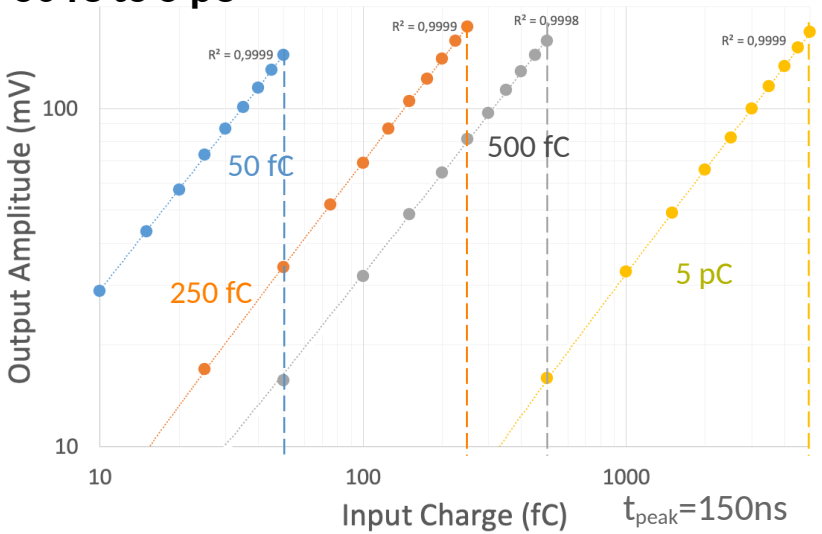


MAIN RESULTS WITH 120 PF INPUT CAPACITANCE

Peaking time programmable from **50 ns to 500 ns** with no tail

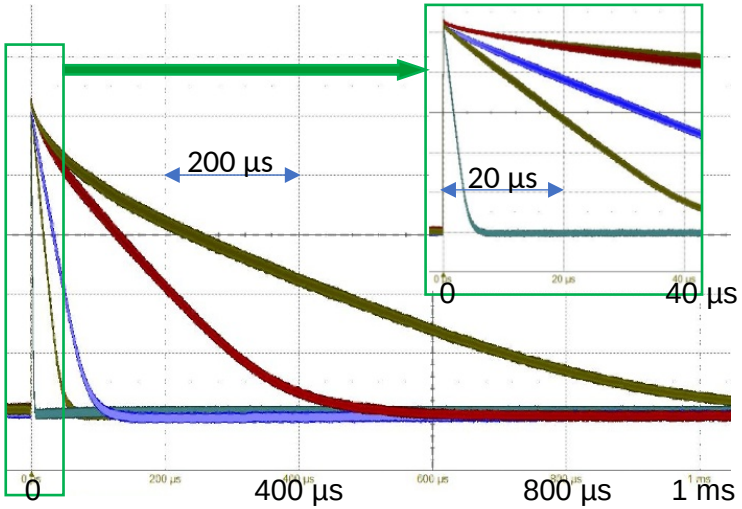


Gain programmable => dynamic range from **50 fC to 5 pC**

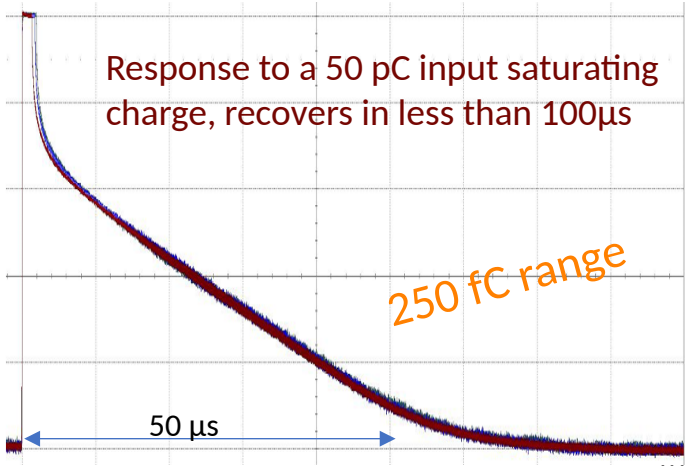


Preliminary

T_{fall} CSA programmable from 5 µs for high rate to 1 ms for low noise



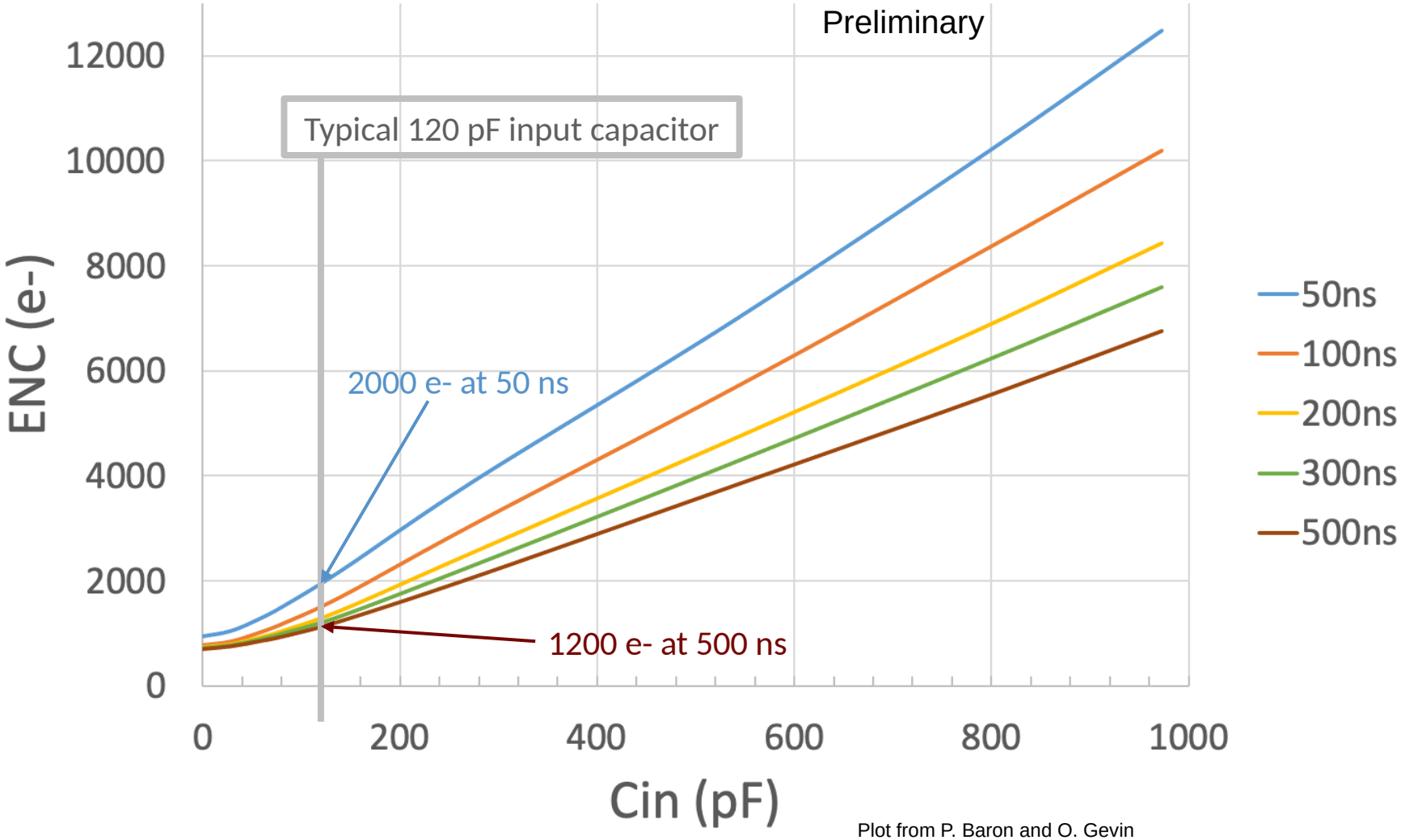
CSA anti-saturation circuit => **fast recovering**



Plots from P. Baron and O. Gevin

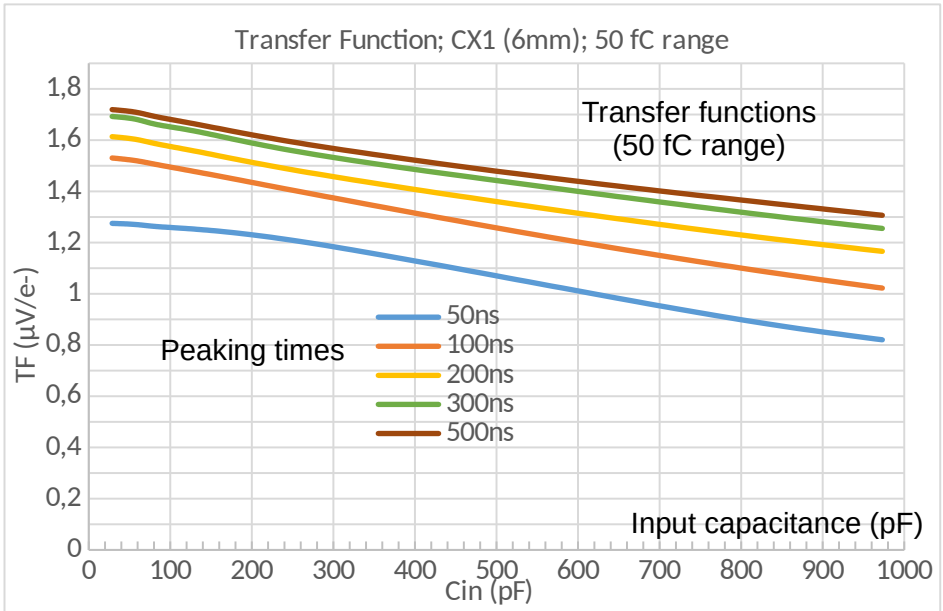
MAIN NOISE RESULTS: TYPICAL CASE

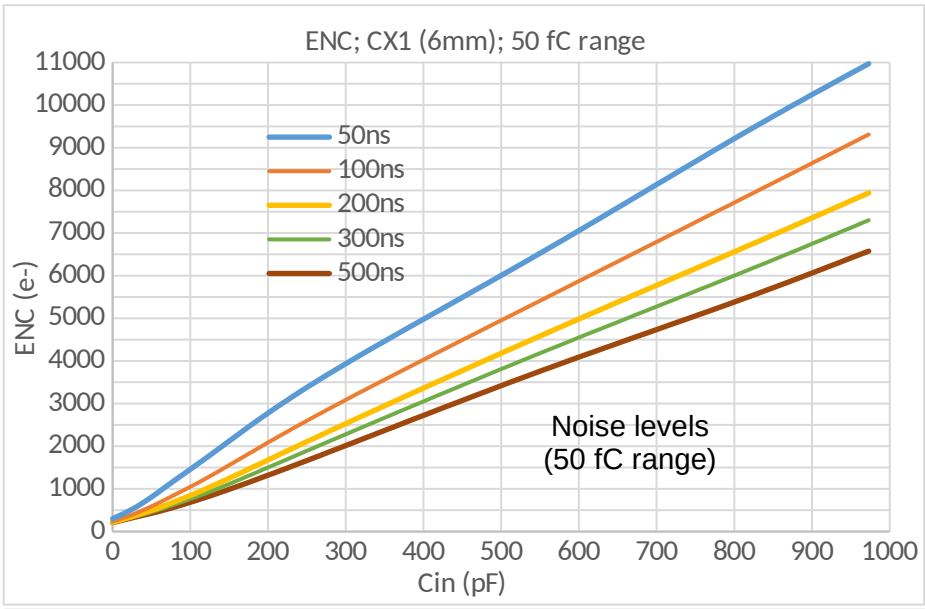
Equivalent Noise Charge in the **250 fC range** at different peaking times



Plot from P. Baron and O. Gevin

TESTS ON FRONT-END STAGE





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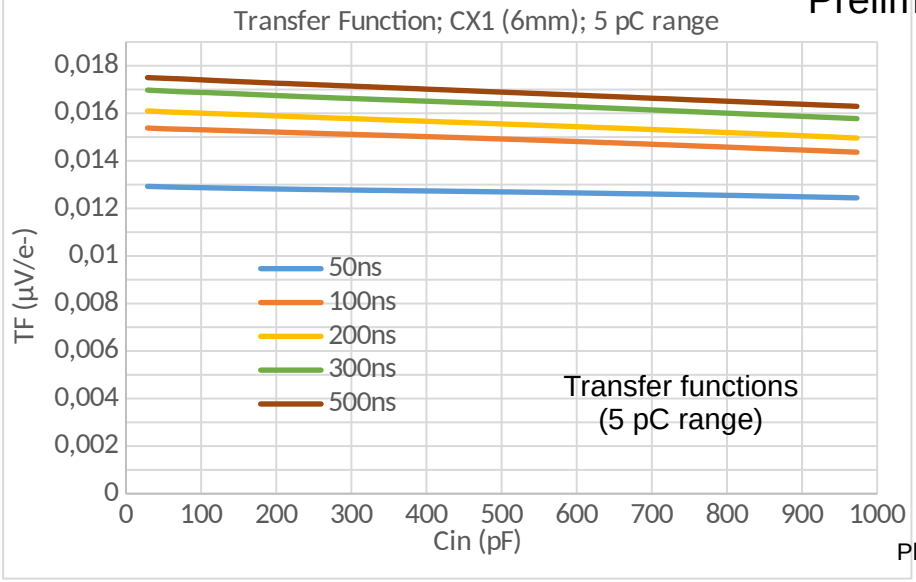
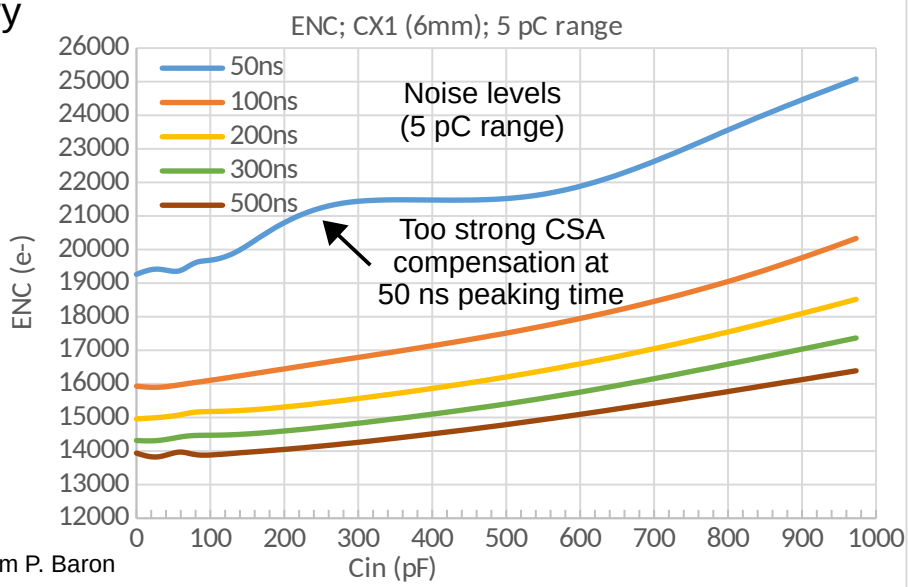




Plots from P. Baron

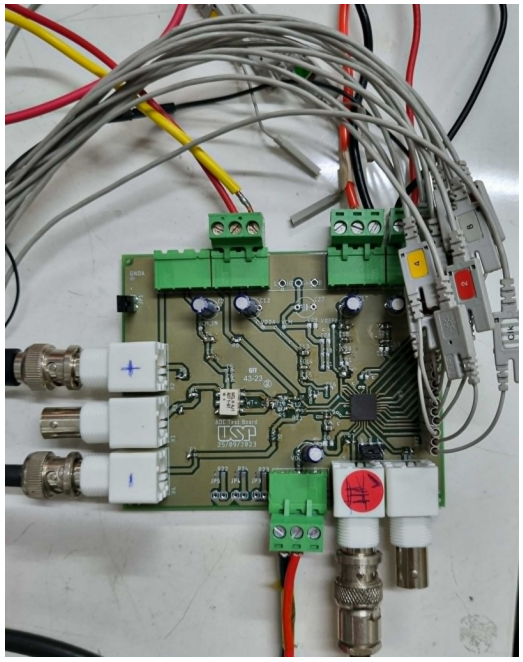
TESTS ON ADC BLOCK

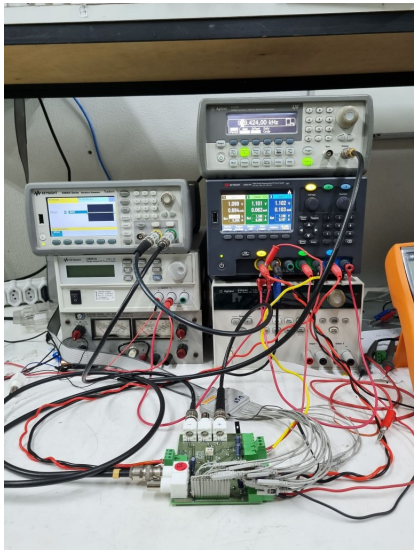
SALSA0_digital prototype

- 1 ADC block
- Test board to feed LV and clocks (sampling and conversion)
- Digital analyzer to read ADC output
- Tests started after mid-November

Very preliminary outcomes

- Problems of bonding with some of the prototypes
- Power consumption lower than foreseen in simulation (factor > 2)
- Unexpected offset for the 0 digital value, investigation ongoing on test board and in simulation
- ADC prototype under study, no result yet





CONCLUSIONS AND QUESTIONS

Present status

- Performance specifications finalized, but could be adapted in function of chip block study results. We are still open to suggestions !
- Tests ongoing on SALSA0 and PRISME prototypes, helpful to fix bugs, verify simulations, and evaluate performances
- Design of SALSA1 prototype (front-end + ADC) in progress
- Studies ongoing on logic architecture and DSP data processing for SALSA2 prototype

Questions related to SALSA

- Are present specifications satisfactory for all EPIC MPGDs ?
- Still miss full requirements from barrel and endcap µRWell concerning signal amplitudes (typical, min, max), hit rates/channel, input capacitance, expected noise levels, expected peaking times, etc…
- What DSP features are required ? What specific requirement concerning data format ?
- What about the calibration strategy for MPGDs ? Characteristics required for calibration data ? What rate ?
- Discussion foreseen January 18th about DSP content, data format and backend interface with DAQ/electronics WG