On FEBs for ePIC MPGDs
Intro for technical and organizational choices
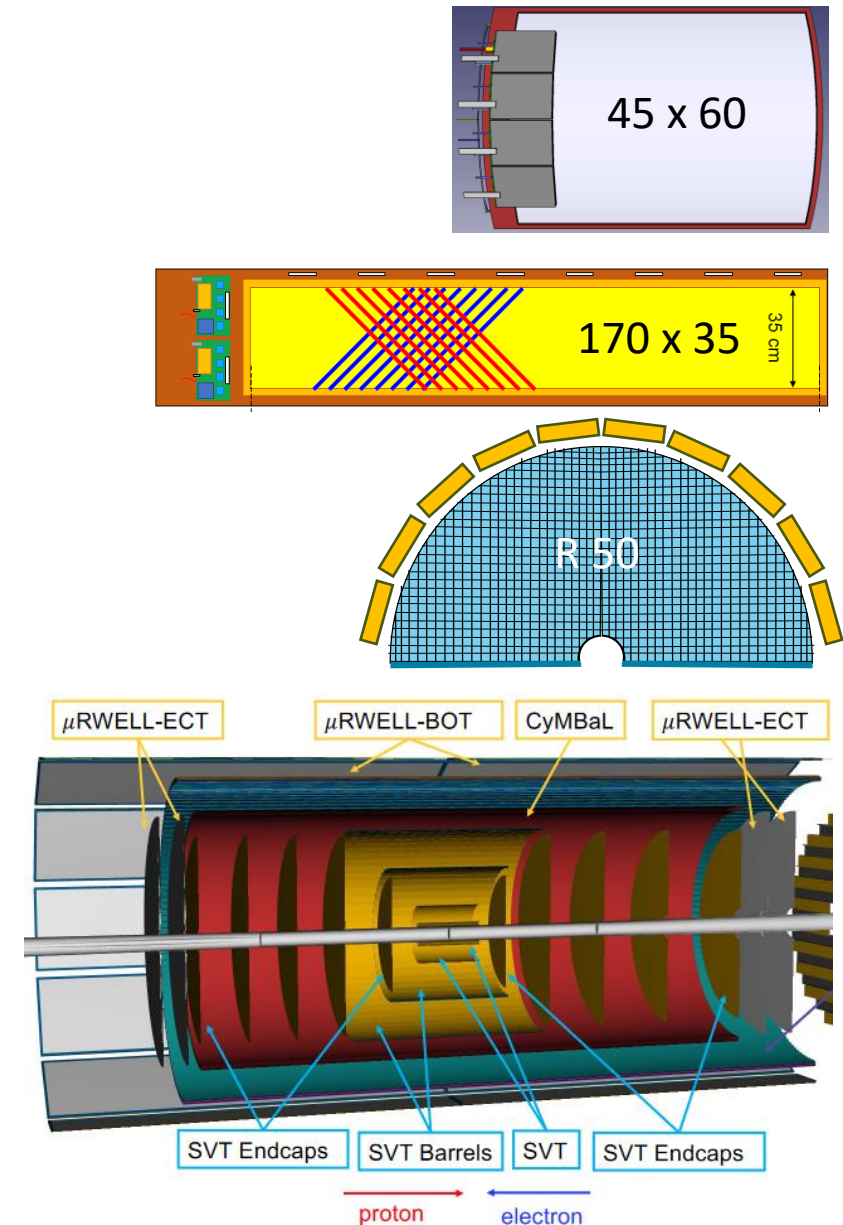
Irakli Mandjavidze
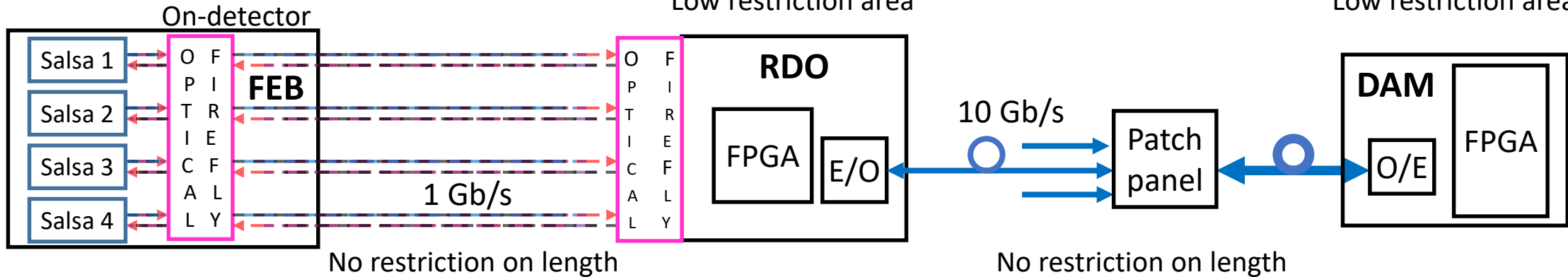
Irfu, CEA Saclay
Gif-sur-Yvette, 91191
France
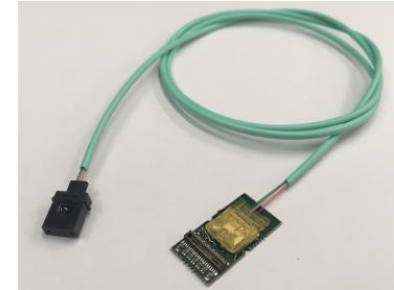
MPGD-DSC general meeting
7/Nov/2024

Outlook

- Reminder of the readout architecture

- Evolution since the Tracking (March) and eDAQ (June) TDRs
  - → Generalization of VTRX+
  - → Strong move towards lpGBT

- Impact on MPGD FEBs and readout

- How to proceed …

- Summary

- Cylindrical Micromegas Barrel Layer : CyMBaL : ~30k channels
    - → 32 **tiles** of 1024 channels each

45 x 60

- μRWELL Barrel Outer Tracker : μRWell-BOT : ~100k channels
    - → 24 **modules** of 4 096 U-V strips each

170 x 35

35 cm

- μRWell End Cap Tracker : μRWell-ECT : ~30k channels
    - → 8 **half-disks** of 4 000 X-Y strips each

R 50

- **~160k-channel** heterogeneous system
    - → Micromegas, μRWell, barrel, endcap, curved, planar, circular

μRWELL-ECT   μRWELL-BOT   CyMBaL   μRWELL-ECT

- Common approach to acquire data from different types of ePIC MPGDs
    - → Use same frontend ASIC
        - ■ Salsa – under development
    - → Share frontend design between groups
        - ■ Adapt form factor if needed

SVT Endcaps   SVT Barrels   SVT   SVT Endcaps

proton   electron

Electron-Ion Collider

FEB based on Salsa's unified interface with optical FireFly

Low restriction area

Low restriction area

On-detector

Salsa 1, Salsa 2, Salsa 3, Salsa 4 — OPTICAL FIREFLY — **FEB**

1 Gb/s

No restriction on length

OPTICAL FIREFLY — **RDO** — FPGA, E/O

10 Gb/s — Patch panel — **DAM** — O/E, FPGA

No restriction on length

- **FEB :**
  - → ASICs are directly interfaced to 4-lane bidirectional parallel optic FireFly transceivers
  - → Requires an "innovative" ASIC interface:
    - Rx line encoding clock and data (sync & async commands)
    - Plus extra handy features:
      - A low speed embedded ADC for environmental monitoring
      - A GPIO outputs for on-board control

Optical 4 Tx & 4 Rx FireFly from Samtec

- **RDO : common hardware with adaptation based on COTS FireFly transceivers from Samtec**
  - Four 4-lane bidirectional FireFly components are needed to serve 4 FEBs
  - → Placed anywhere in user friendly area
    - No particular restrictions on power consumption, cooling infrastructure, radiation, magnetic field

- **CERN low profile low power electrical / optical transceiver**
  - → Developed for HL-LHC upgrade
  - → 1 downlink : up to 2.5 Gbit/s
  - → 4 uplinks : up to 10 Gbit/s each
  - → Radiation hard
  - → Fragile
  - → One shot production

- **2023 : request from EIC project and ePIC**
  - → Rise a hand if ABSOLUTELY needed
  - → MPGD response after in-depth study : cannot pronounce on ABSOLUTE but can be a missing opportunity
  - → Project response to MPGD response – no VTRX+ for MPGDs

- **August 2024 : push from EIC project and ePIC to generalize its use for inner detectors**
 - → MPGD response : ~1 000 units including spares and prototyping

FEB based on Salsa's unified interface with VTRX+

Low restriction area

Low restriction area

On-detector

CERN VTRX+
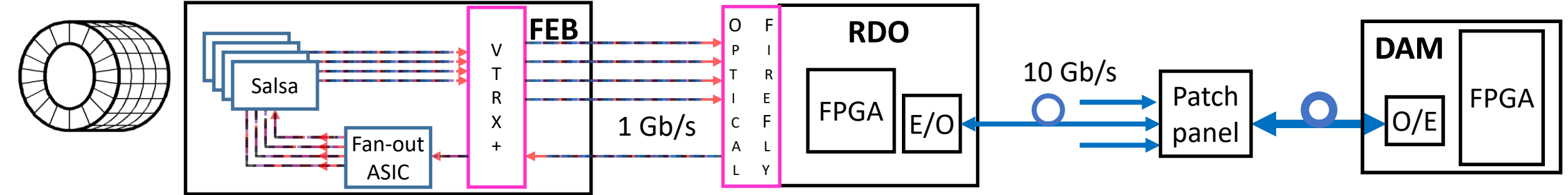
- **FEB**
  - → Salsa receives embedded clock / sync / async data over the unified RX interface
    - ■ VTRX+ RX serial link to Salsas via a rad-hard fan-out ASIC
  - → Salsa sends physics, monitoring and slow control data over a single TX line
    - ■ One VTRX+ TX serial link per Salsa
  - → All ASICs are radiation hard
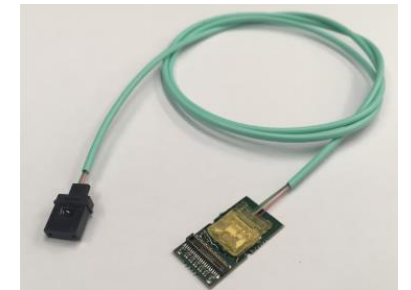
- **RDO : common hardware with adaptation based on COTS FireFly transceivers from Samtec**
  - ■ Four 4-lane bidirectional FireFly components are needed to serve 4 FEBs
  - → Placed anywhere in user friendly area
    - ■ No particular restrictions on power consumption, cooling infrastructure, radiation, magnetic field

# The lpGBT story

- **CERN low power gigabit transceiver**
  - → Developed for HL-LHC upgrade
  - → 1 downlink : up to 2.5 Gbit/s
  - → 1 uplinks : up to 10 Gbit/s each
  - → Control and aggregate data from a number of ASICs
  - → 40 MHz clock domain with 5 ps clock jitter
  - → Radiation hard
  - → One shot production

Paulo.Moreira@cern.ch

- **Summer 2024 : ePIC frontends using CERN-flavored ASICs**
 - → Move to use lpGBT as on-board "transparent" controller-aggregator
    - ■ Avoiding the use of FPGAs on frontends
  - → ~100 MHz / 5 * 2 = ~40 MHz within the narrow locking range of lpGBT

- **September 2024 : ePIC eDAQ WG asks who can and is interested to use lpGBT**
  - → MPGD response : lpGBT is certainly an interesting and attractive option
    - ■ https://indico.bnl.gov/event/25106/contributions/97861/attachments/57983/99568/241017_IM_lpGbt2Salsa.pdf
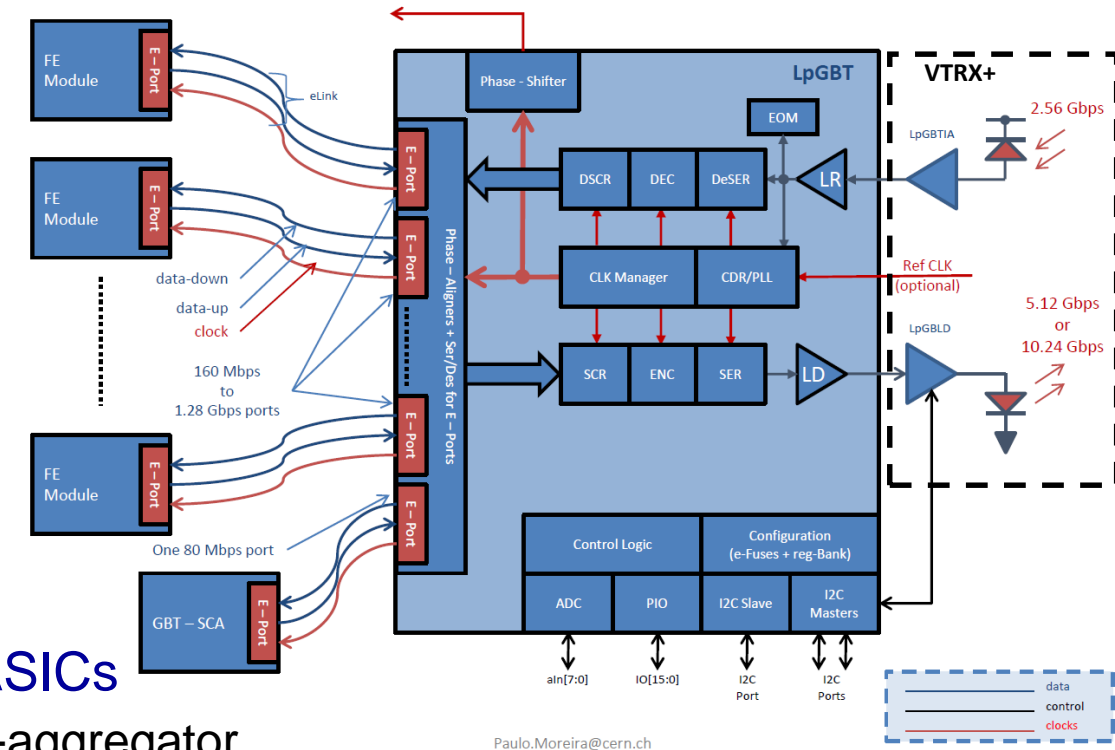
FEB based on Salsa's heterogeneous interface with lpGBT
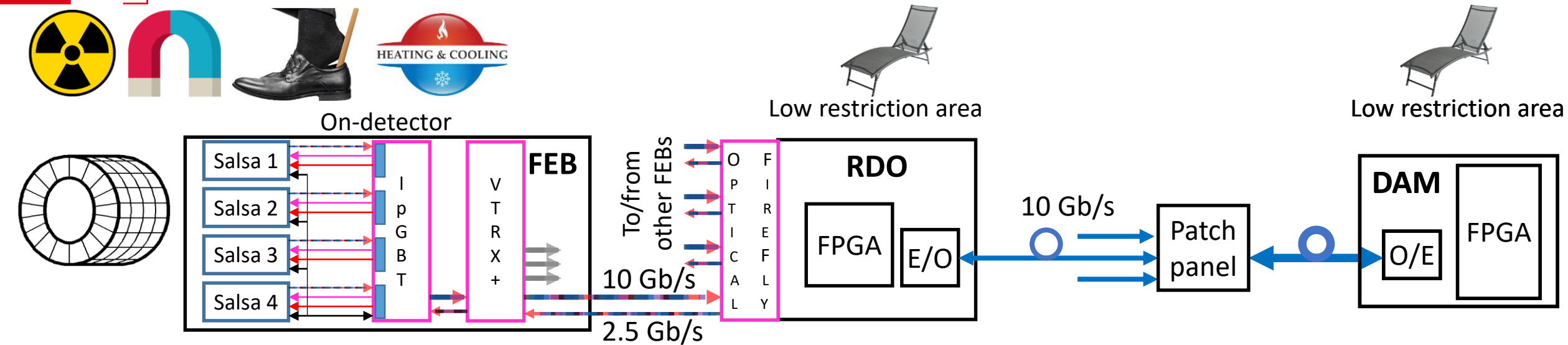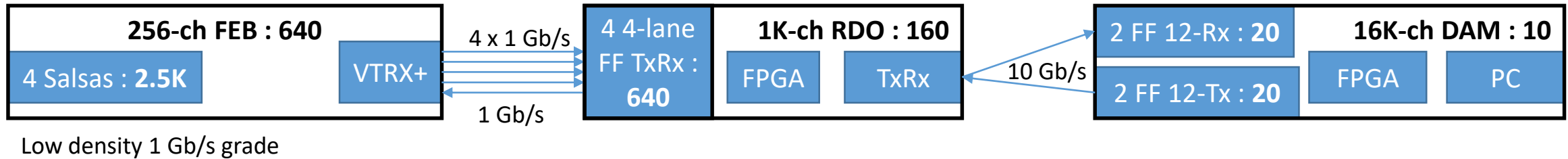

- **256-channel FEB**
  - → Salsa receives recovered clock and sync data from an lpGBT eLink group
  - → Salsa sends physics, calibration and monitoring data to a number of lpGBT lines of the eLink group
  - → Salsa's are configured over daisy chained I2C interface from lpGBT
  - → lpGBT provides a bidirectional interface between 4 Salsas and remote FPGA on RDO
  - → lpGBT provides digital and analog control of the board – GPIO, ADC
  - → VTRX+ is used with only one TX line
  - → All ASICs are radiation hard

- **1024-channel RDO : common hardware with adaptation based on FireFly transceivers from Samtec**
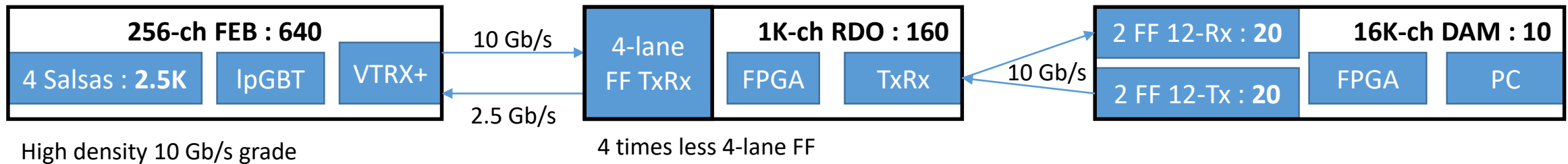 - ■ Single 4-lane bidirectional FireFly is enough to serve 4 FEBs
  - → Placed anywhere in user friendly area
  - ■ No particular restrictions on power consumption, cooling infrastructure, radiation, magnetic field
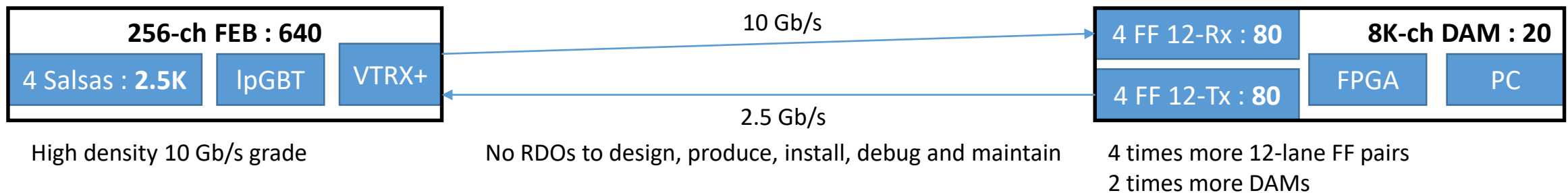
- **FEB with direct Salsa-VTRX+ interface**

256-ch FEB : 640	
4 Salsas : **2.5K**	VTRX+

4 x 1 Gb/s

1 Gb/s

4 4-lane FF TxRx : **640**	1K-ch RDO : 160	
	FPGA	TxRx

10 Gb/s

2 FF 12-Rx : **20**	16K-ch DAM : 10	
2 FF 12-Tx : **20**	FPGA	PC

Low density 1 Gb/s grade

- **FEB with lpGBT-VTRX+ interface**

256-ch FEB : 640		
4 Salsas : **2.5K**	lpGBT	VTRX+

10 Gb/s

2.5 Gb/s

4-lane FF TxRx	1K-ch RDO : 160	
	FPGA	TxRx

10 Gb/s

2 FF 12-Rx : **20**	16K-ch DAM : 10	
2 FF 12-Tx : **20**	FPGA	PC

High density 10 Gb/s grade

4 times less 4-lane FF

- **FEB with direct DAM interface**

256-ch FEB : 640		
4 Salsas : **2.5K**	lpGBT	VTRX+

10 Gb/s

2.5 Gb/s

4 FF 12-Rx : **80**	8K-ch DAM : 20	
4 FF 12-Tx : **80**	FPGA	PC

High density 10 Gb/s grade

No RDOs to design, produce, install, debug and maintain

4 times more 12-lane FF pairs
2 times more DAMs

How to proceed …

- Salsa team still needs to work on details
    - → Harmonizing unified and heterogeneous interfacing with 100 MHz EIC and 40 MHz CERN clock domains

- In parallel, concerned MPGD groups can meet during a session dedicated to FEBs and readout
    - → Status and more in depth discussion of technical questions

    - → Update on environment – especially space constraints
    - → Update on acceptable FEB form-factors
        - Channels per FEB
        - Size

    - → Discussion on power and perhaps on cooling
        - https://indico.bnl.gov/event/25107/contributions/97957/attachments/58092/99805/241024_IM_PowerAndVtrx.pdf

    - → FEB organization : single board or mother-board + mezzanine
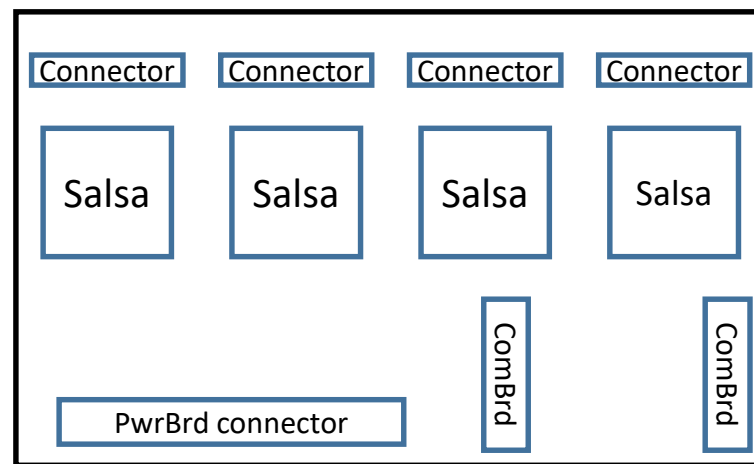
    - → How the work can be shared

- **Single board**

Mezzanine approach
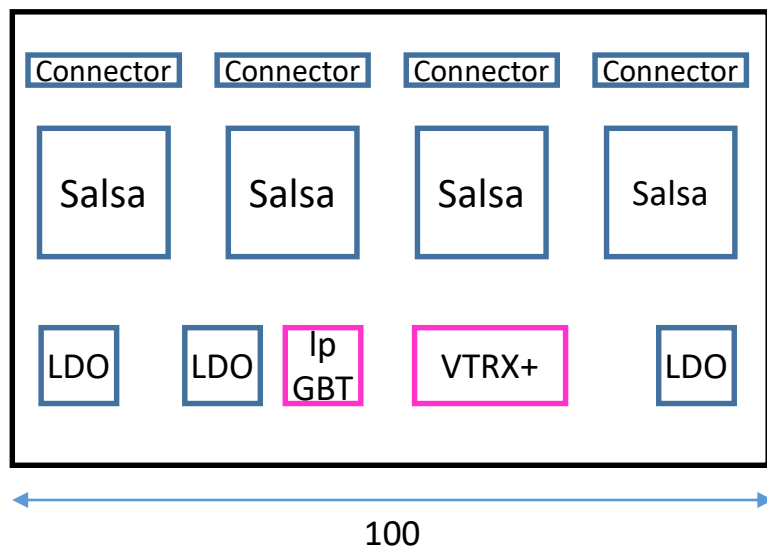
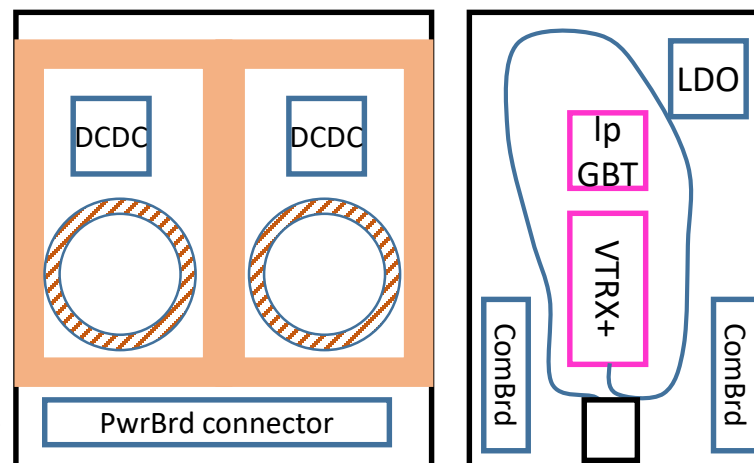→ Complex high density high speed
→ MPGD-specific form factor

→ FEB mezzanine
→ Low density low speed
→ MPGD-specific form factor

→ DC/DC mezzanine
→ 2 T tolerant low EMI
→ Common to all MPGDs ?

→ Communication mezzanine
→ high density high speed
→ Common to all MPGDs ?

Summary

- **CERN-proven components become available for MPGD frontends**
  - → VTRX+, lpGBT, DC/DC regulators
  - → Frontend design and readout architecture may benefit from this favorable evolution
    - Especially, if an intermediate control and aggregation RDO stage could be avoided

- **A dedicated "electronics" session would be welcome between concerned groups and people**
  - → Status update and technical discussion
  - → Possible discussion on work sharing
    - FEB design
      - Saclay has an expertise
    - Possibly communication mezzanine design
      - Saclay has an expertise
    - Possibly DC/DC mezzanine design
      - Saclay expects support from groups actively involved in powering studies
    - Power distribution
      - Saclay has an expertise
    - Colling
      - No particular studies have been conducted at Saclay
    - Other related services : *e.g.* slow control and monitoring

  - → If found relevant, can MPGD DSC organize the session ?