UNIVERSITY OF BIRMINGHAM

Shunt-LDO basics

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EIC-LAS and S-LDO interfaces discussion at Birmingham

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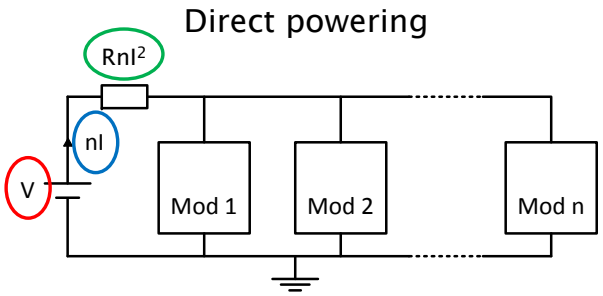
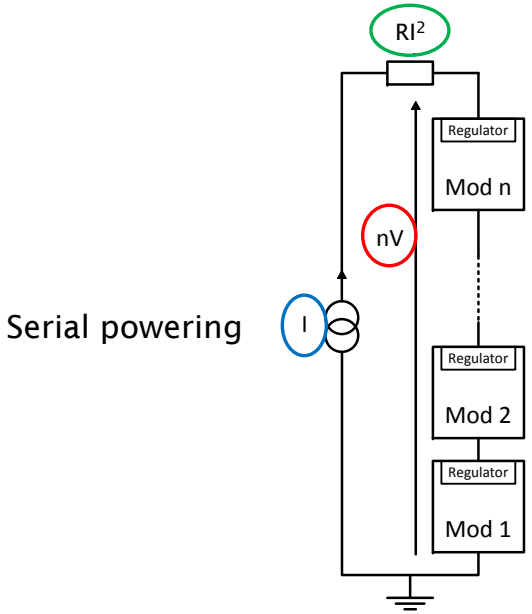
Introduction

- The ATLAS and CMS upgraded pixel trackers at the HL-LHC will use serial powering with regulators integrated in their 65 nm readout chip.
- The regulator they use is the Shunt-LDO.
- This regulator was originally designed in Bonn by Michael Karagounis in GF130 nm and it is integrated already in the FE-I4 that is the readout chip for the innermost layer (i.e. IBL) of the current ATLAS pixel detector.
  - Note the IBL does not use it for serial powering, more on this later.
- I will show now the original design. The regulator has been much further developed in the 65 nm version, with added features to guarantee safety of the serial powering chain. I believe the working principle however stayed the same.
- More on the original Shunt-LDO and proof of concept of serial powering for ATLAS in my PhD thesis: https://cds.cern.ch/record/1633150?ln=en

Serial powering basics

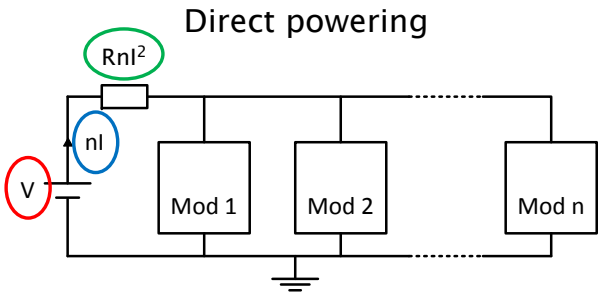
- Serial powering is a current based powering scheme, where modules are powered in series by a constant current.
  - The current to voltage conversion is done by regulators on module.
- In a serial powering chain made of n modules, the transmitted current is only the current needed by one module, I.
- For n modules powered in series, the current is reduced of a factor n with respect to a direct powering scheme → Higher power efficiency and reduced cable volume.
  - Cable cross-section and the power losses on the cables scale by the same factor.



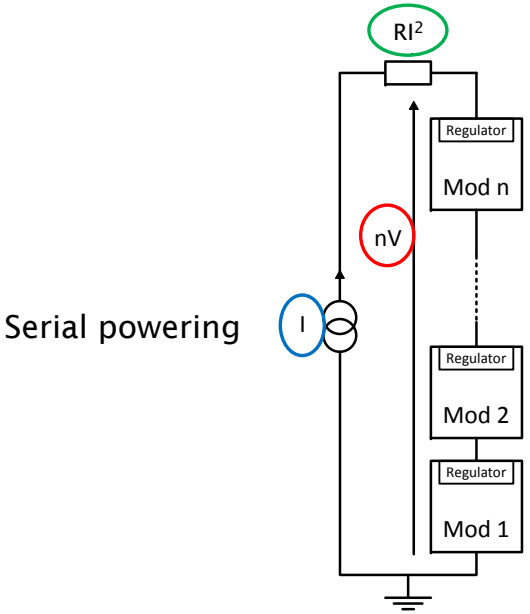


Serial powering basics

- As the modules are powered with a constant current, V_{drop} is not constrained as in a voltage based powering scheme.
  - It can in principle be chosen only depending on the output voltage capability of the current source and of the allowed power density (i.e. cooling capability).



- Higher V_{drop} can be allowed in the active area of the detector to reduce the material budget of the cables.
  - Outside the detector the voltage drop can be reduced to lower the power losses.

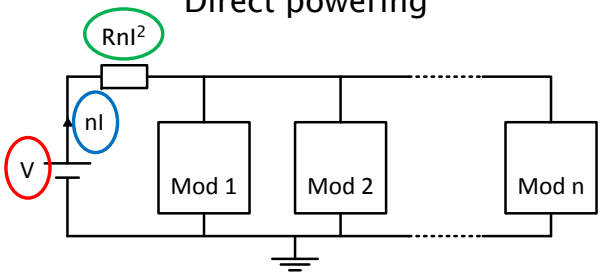


- With respect to voltage based powering schemes (incl. DC-DC), serial powering allows more flexibility in the optimization of material and power efficiency.

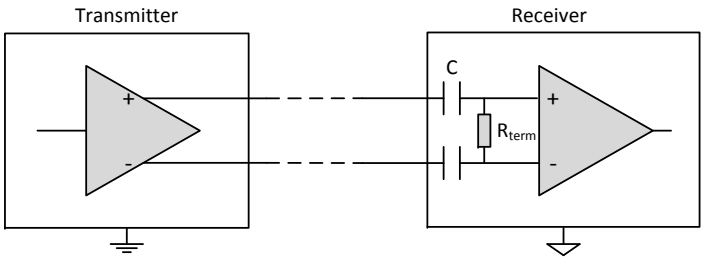
Serial powering basics

- The voltage across the chain is nV, where V is the voltage on a module.
- Each module sits at a different ground potential.
- AC coupled data transmission required.
  - DC balanced data protocol (e.g. 8b10b).
  - Self biased receiver inputs to set the common mode voltage.

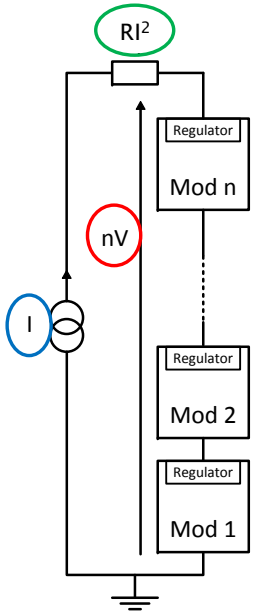
Direct powering



Sketch of a AC-coupled LVDS link

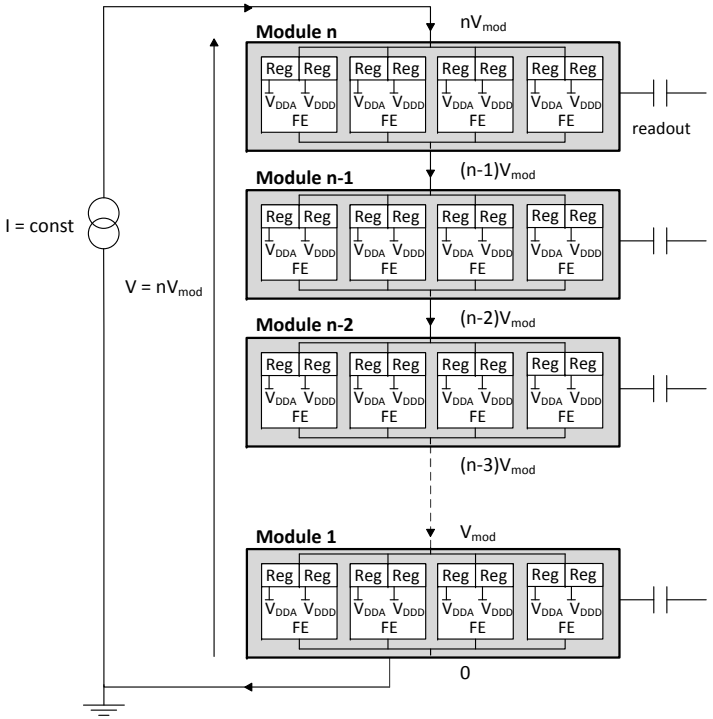


Serial powering

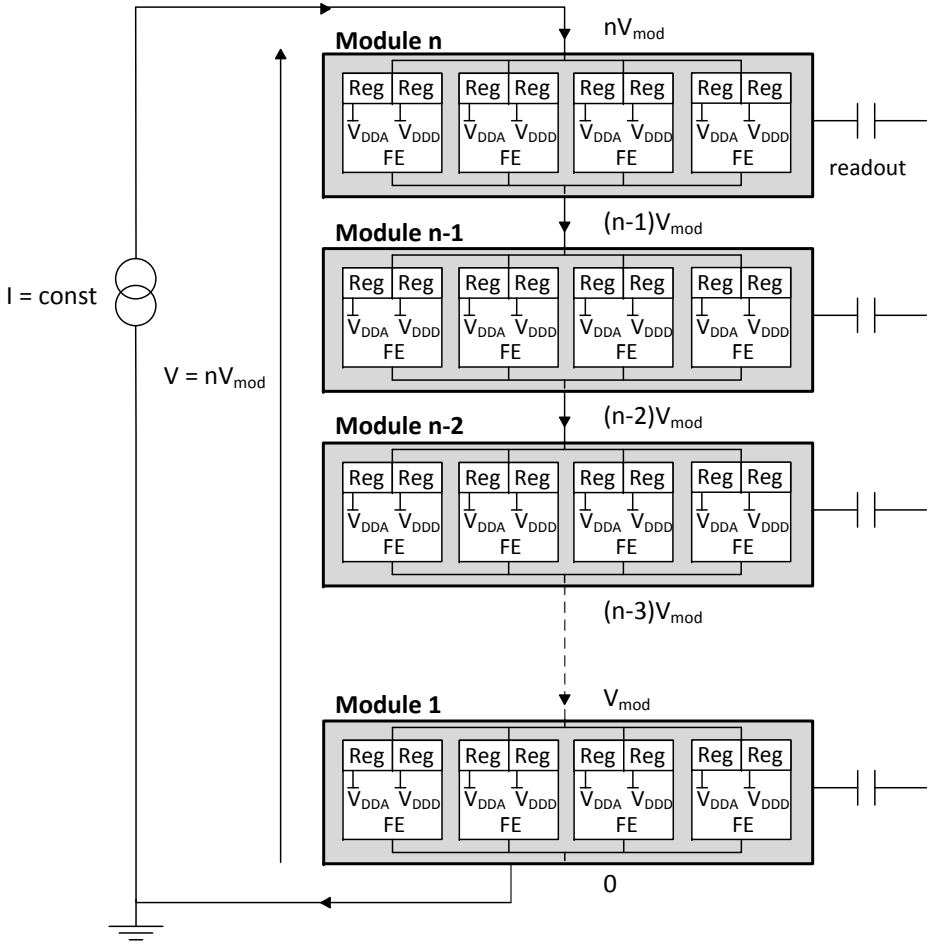


Example: ATLAS ITk detector

- The ATLAS pixel detector at the HL-LHC adopted serial powering (also the CMS pixel detector).
- Each module is made of a sensor bump bonded to a certain number of readout chips.
  - In the sketch, four readout chip per module (FE).
- The current flows in series between modules and in parallel between readout chips on a module.
- In each chip, two shunt-LDO regulators generate the analogue (V_{DDA}) and digital (V_{DDD}) voltages.



Serial powering chain of pixel modules



- The figure shows a sketch of the SP configuration proposed for the ATLAS pixel detector and demonstrated in the original proof of concept.
- **On-chip regulators are needed that can:**
  - **Operate in parallel;**
  - **Generate different output voltages out of the current supply;**
  - **Shunt additional current in case of device failure.**
- **The Shunt-LDO regulator was designed to match these requirements.**

Figure 4.1: Sketch of a SP chain, showing its main features. The modules are connected in series and powered via a constant current I. The voltage across the chain is n times the voltage across one module V_0. The current splits on module between the parallelly connected regulators on the FE chips, which generate the analog and digital voltages, respectively *VDDA* and *VDDD*. The data communication to and from the modules is AC-coupled.

Early regulators configurations

- Initial tests were done with the ATLAS FE-I3 pixel chip using a Shunt-LDO to generate a constant voltage out of the input current and then one or two LDO to generate the VDDD and VDDA voltages needed by the pixel chip.
- To add redundancy to the SP chain, all shunt regulators on module are operated in parallel.
- Beneficial for voltage regulation when using shunt regulators as the input resistances are connected in parallel, lowering the total resistance and improving the voltage stabilization.

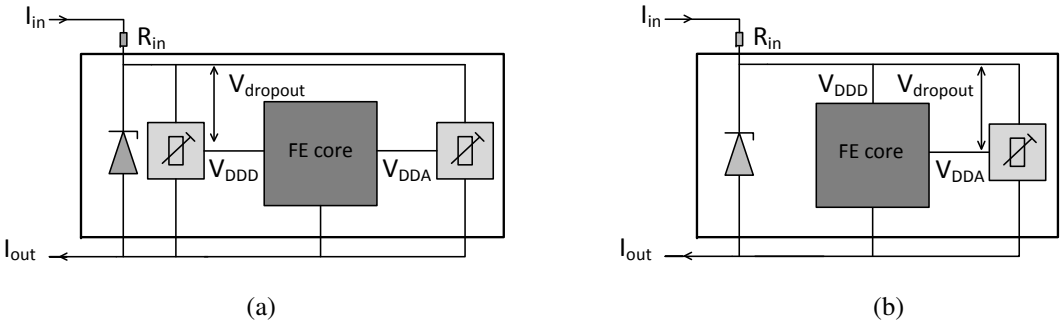
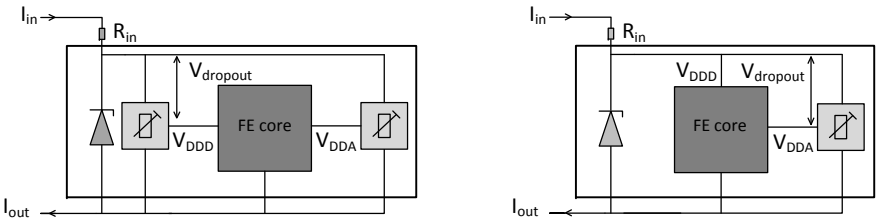


Figure 4.4: Schematic drawings of on-chip shunt and LDO regulators, represented respectively as a zener diode and variable resistors, to convert the input current into two stable voltages. These regulator configurations have been used with FE-I3 modules to generate $VDDD$ = 2.0 V and $VDDA$ = 1.6 V.

Early regulators configurations

- However, this connection can be critical.
  - Due to mismatch and process variation, the shunt regulators placed in parallel can have different V_{thres}.
  - As the input characteristics of shunt regulators is very steep, the regulator with lower V_{thres} can take all current at start- up and burn.
  - This could eventually lead to a chain reaction and destroy all regulators on module.
- Safe parallel operation of shunt regulators requires to choose the value of the input series resistance according to the spread in threshold voltage values, in order to mitigate the I-V characteristics.
- The use of this resistance lowers the power efficiencv and decreases the voltage stability.



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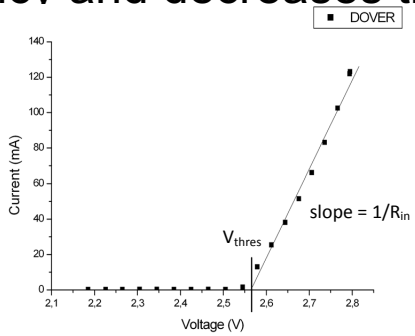


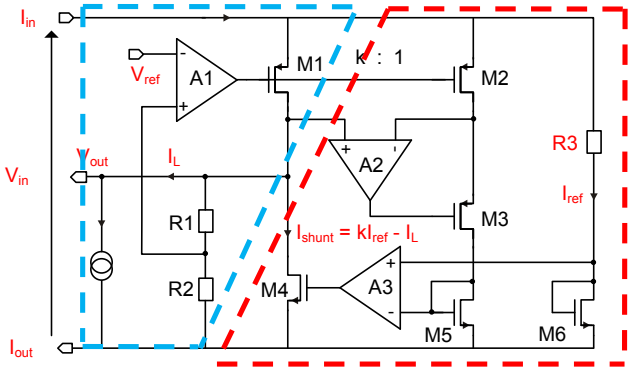
Figure 4.3: I-V characteristics of a shunt regulator integrated in the FE-I3 chip (DOVER). This regulator has $V_{thres} = 2.58\,\mathrm{V}$ and $R_{in} = 1.9\,\Omega$ [51].

The shunt-LDO regulator

- For this powering scheme, on-chip regulators are needed that can:
  - Operate in parallel;
  - Generate different output voltages out of the current supply;
  - Shunt additional current in case of device failure.

- The Shunt-LDO regulator was designed to match these requirements.
  - First version in the ATLAS pixel FEI4 chip (180 nm process).
  - Full SP version in the RD53 chip (65 nm process).

- It combines two regulation loops.
  - Shunt regulation circuitry → regulates the current to the chip.
  - LDO (Low Drop Out) regulation loop → generates the voltage for the chip.



The Shunt-LDO

- Combination of a LDO (Low Drop Out) regulator and a shunt regulator.
  - Shunt transistor is part of the LDO load.
  - R_{in} of the shunt is replaced by the LDO power transistor.

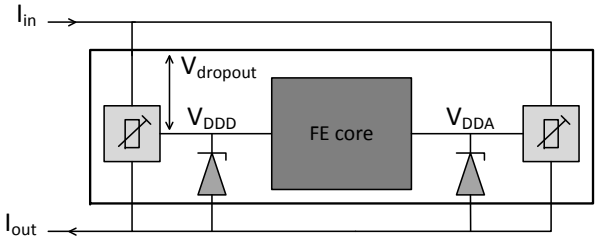
- LDO regulation loop → constant V_{out}

$$V_{out} = 2 \cdot V_{ref}$$

- Shunt regulation circuitry → const I_{load}
  - I_{ref} set by R3, depends on V_{in} (→ I_{in})
  - I_{M1} mirrored and drained in M5
  - I_{M1} and I_{ref} compared in A3
  - M4 shunts the current not drawn by the load

$$I_{in} \approx kI_{ref} \approx k\frac{V_{in} - V_{thM6}}{R3}$$

$$R_{in} \approx \frac{V_{in}}{I_{in}} \approx \frac{R3}{k}.$$



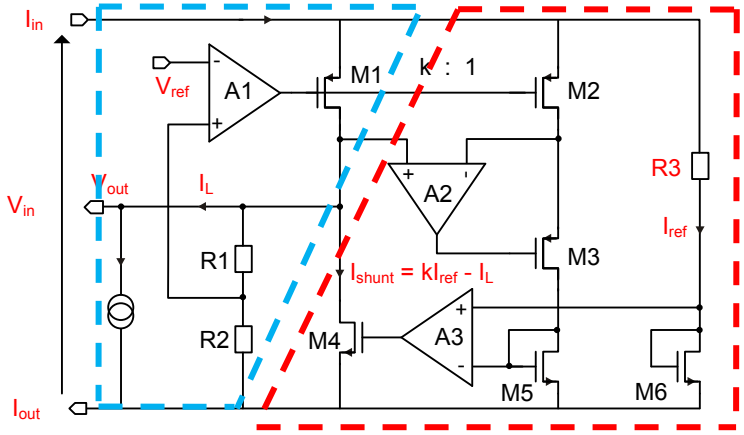


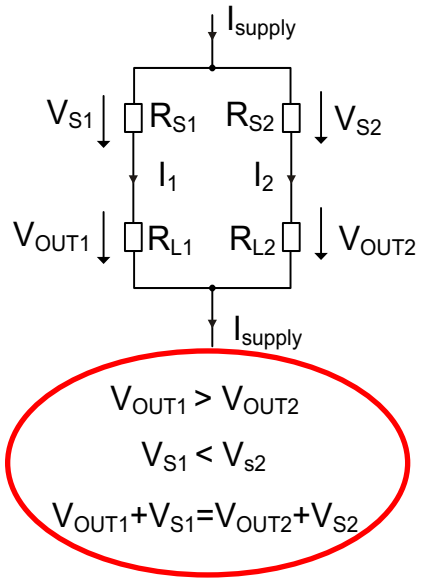
Figure 4.6: Simplified schematics of a Shunt-LDO regulator, explained in the text [46].

Shunt-LDO regulators in parallel

- The Shunt-LDO has an ohmic I-V characteristics → safe operation of Shunt-LDO regulators connected in parallel.
  - Even for different values of R_{in}, i.e. different R3
  - More robust design against process variation and mismatch.
  - Differences in the value of R3 lead to different shunt current values but do not destroy the regulator.
  - Shunt- LDO regulators can be placed in parallel even if they generate different output voltages: the difference between their output voltages is compensated by the $V_{dropout}$ across the pass transistor of the LDO regulator, M1.
  - Finally, should one of the parallelly placed regulators fail, the extra current can be shunted by the other regulators.

$$R_{in} \approx \frac{V_{in}}{I_{in}} \approx \frac{R3}{k}.$$

2 Shunt-LDOs in parallel: equivalent circuit



Shunt-LDO working modes

- The Shunt-LDO can operate as a standard LDO by disabling the current regulation loop.
- It can operate in partial-shunt mode, i.e. in LDO mode but with enabled current regulation loop.
  - The value of *R*3 is set in order to have a minimum current flow through the regulator in absence of a load.
  - This configuration can be used to reduce transients on the power line in voltage based powering schemes.
  - This is how the regulator is used in the FE-I4 in the IBL.

Table 4.3: Working modes of the Shunt-LDO regulator. The selection of the working mode is done by choosing either a constant voltage or current supply for the regulator, and by enabling or not the current regulation loop.

	Shunt-LDO mode	LDO mode	Partial shunt mode
Current regulation loop	enabled	disabled	enabled
Regulator input	I	V	V

Serially powered systems

Conventional voltage based supply schemes

Shunt-LDO and SP for ePIC SVT

- We decided to design an external Shunt-LDO in 180 nm process
  - Cheaper process; MPW runs every 3 months
  - No need to modify LES
- Per EIC LAS we need one Shunt-LDO for the global analogue supply, and one for the global digital supply
  - How to add redundancy in case of failure of one of these?
- Where to place the Shunt-LDO regulators on the FPC?
- Shunt-LDO specs might need updating to ER2 power figures
- How many SP chains? How many sensors per chain?