Fachhochschule Dortmund
University of Applied Sciences and Arts

Verification of the Shunt-Low-Dropout voltage regulator for the current based supply of the serially connected pixel detector modules of the ATLAS- and CMS-experiments at the High-Luminosity Large Hadron Collider

Master Thesis

for obtaining the academic degree

Master of Engineering (M.Eng.)

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Kurzfassung

Validierung eines Shunt-Low-Dropout-Spannungsreglers zur strombasierten Versorgung der seriell verschalteten Pixel-Detektormodule des ATLAS- und CMS-Experiments am High-Luminosity Large Hadron Collider.

Diese Ausarbeitung dokumentiert die Verifikation des Shunt-Low-Dropout-Spannungsreglers für den Einsatz im ATLAS- und CMS-Projekt. Im Rahmen einer Kooperation zwischen der Fachhochschule Dortmund und dem Forschungsinstitut CERN in Genf wird eine integrierte CMOS Schaltung zur seriellen, strombasierten Spannungsregelung der Pixeldetektormodule entwickelt. Der Fokus dieser Masterthesis ist die simulationstechnische Verifikation unter Berücksichtigung der spezifizierten Einsatzbedingungen in den Experimenten und umfasst - neben einer Einführung in den Shunt-LDO Regler auf Basis des Testchip C - die Vorstellung und Dokumentation der erarbeiteten Simulationsergebnisse.

Abstract

Verification of the Shunt-Low-Dropout voltage regulator for the current based supply of the serially connected pixel detector modules of the ATLAS- and CMS-experiments at the High-Luminosity Large Hadron Collider.

The thesis in hand covers the verification of the Shunt-Low-Dropout voltage regulator for the purpose of a serial, current-based power supply of the pixel detector modules in the ATLAS- and CMS-experiment at CERN-institute in Geneva. The development of this regulator is part of a cooperation between the University of Applied Science in Dortmund and CERN. This elaboration focuses on the simulation-based verification with emphasis on the specified operating conditions in the experiments and the documentation of the results. A further part of this report is an introduction of the RD53B-microchip based on the test chip C.

Contents

Acronyms

ATLAS	Experiment resp. detector at LHC
CERN	Conseil européen pour la recherche nucléaire (European Organization for Nuclear Research)
CMS	Experiment resp. detector at LHC
DAC	Digital-to-Analog-Converter
LDO	Low-Dropout-Spannungsregler
LHC	Large Hadron Collider
HL-LHC	Project to increase luminosity of the LHC
NMOS	n-type metal-oxide semiconductor
OP	Operational amplifier
OVP	Overvoltage Protection
PCB	Printed Circuit Board
PMOS	p-type metal-oxide semiconductor
SLDO	Shunt-Low-Dropout-voltage regulator
CMOS	Complementary metal oxide semiconductors
Vref	Reference voltage
Vout	Output voltage
Vofs	Offset voltage
Vin	Input voltage
Vth	Threshold voltage
VGS	Gate-Source voltage
VDS	Drain-Source voltage
VGD	Gate-Drain voltage

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1 Introduction

The elaboration in hand is the master thesis for the attainment of the academic degree “Master of Engineering (M.Eng)“ in electrical engineering at the University of Applied Science and Arts Dortmund. It deals with a crucial component of the pixel detector modules for the ATLAS- and the CMS-experiment, installed at the Large Hadron Collider (LHC) at Geneva/Switzerland, which is developed for the High-Luminosity upgrade.

This upgrade aims for an considerably increase in luminosity, which imposes higher demands on the pixel detector modules used in the ATLAS and CMS-experiment at CERN. To handle the expected hit rates, the chips have to be designed for higher integration densities, smaller pixel sizes, faster transmission speed and higher radiation exposure. An efficient power supply of the modules with the actual powering system is no longer possible. For this reason, a new approach is developed which is based on the serial connection of the pixel modules, which are powered by a constant current source. The readout chips are driven by a Shunt-Low-Dropout voltage regulator, which consists of an LDO and a shunt circuit to generate a constant voltage from the constant current. To achieve a high degree of reliability and robustness, simulation-based verification is a crucial part of the development process for the new power supply system. This documentation illustrates the results of the numerous specified simulations of the RD53B test chip C Shunt-LDO-Regulator, which were realized in a test bench with the Cadence Virtuoso EDA software.

The main part of this thesis consists of the development of the above-mentioned test bench, which emulates the most important operating scenarios of the chip when used in the ATLAS and CMS-experiment. Diligent simulation work is necessary to identify errors and misbehavior within the circuitry before entering the layout and tape-out process. Furthermore, the perception of worst-case operating influences like extreme temperatures and variation in the production process is substantial to avoid circuit malfunction during the utilization in the experiment. Although the software capabilities for circuit simulation are extensive, they cannot completely represent the actual behavior of a circuit under all conditions and influences. Therefore the testing conditions defined in the test bench are also verified in a measuring arrangement of the produced prototypes. This part of verification is the subject of an another master thesis[5].

Because of an ongoing cycle of submission and tape-out, multiple iterations of test chips are produced and result in a consecutive verification process.

2 The ATLAS- & CMS-Project

2.1 ATLAS

2.1.1 About the experiment

ATLAS is one of the four major experiments at the 27 km long Large Hadron Collider (LHC) at CERN. It is a general-purpose particle physics experiment run by an international collaboration and, together with CMS, is designed to exploit the full discovery potential and the huge range of physics opportunities that the LHC provides. ATLAS is testing the fundamental predictions of the standard model of physics, which includes the current understanding of what the components of matter are and how they interact with each other. Groundbreaking discoveries for the explanation of how the universe works, like the Higgs-Boson and physics beyond the standard model are archived at the ATLAS-experiment. With a collaboration of over 3000 authors from 183 institutions and 38 countries ATLAS is one of the largest collaborative endeavors ever attempted in science[6].

2.1.2 The detector

With a cylindrical dimension of 46 m in length, 25 m in diameter and a weight of 7000 metric tons, the ATLAS detector is the largest ever constructed. It is a multi-layered instrument designed to detect the tiniest but also most energetic particles. It consists of six different detecting subsystems, wrapped concentrically in layers around the collision point to determine parameters like trajectory, momentum and energy of particles, while allowing them to be individually identified and measured. A magnet system forces charged particles to move on a circular orbit to measure their momentum. The particle beams can reach energies up to seven trillion eV and velocities up to 99,9% of light speed. The amount of data generated from this collisions equals 20 simultaneous telephone conversation held by every person on earth. Only one in a million collisions are potentially interesting for further investigations. The detector is able to identify relevant events to handle to the enormous amounts of data[6].

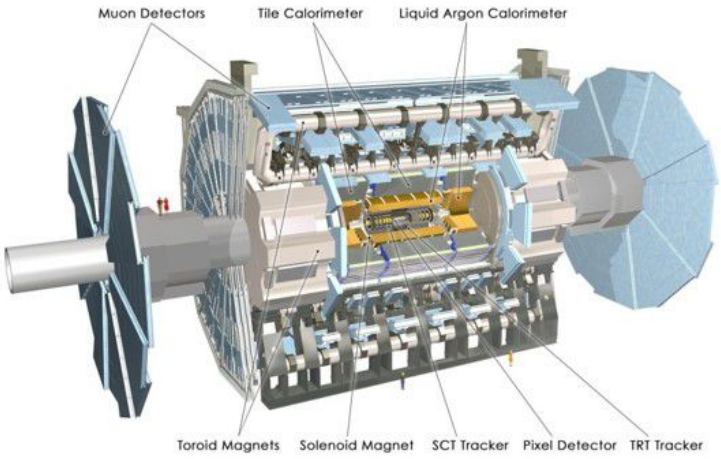

Figure 2.1: The ATLAS-Detector[1]

2.2 CMS

The CMS (Compact Muon Solenoid) detector is, like its ATLAS counterpart, a general-purpose detector. That means it is designed to observe any new physics phenomena that might occur at the LHC. CMS records parameters from particle collisions like momentum and energy to recreate the conditions which were dominating at the time of impact. It weighs 14000 metric tons and measures 21 m in length and 15 m in height. It is especially designed to detect muons and has the most powerful solenoid magnet ever made[2].

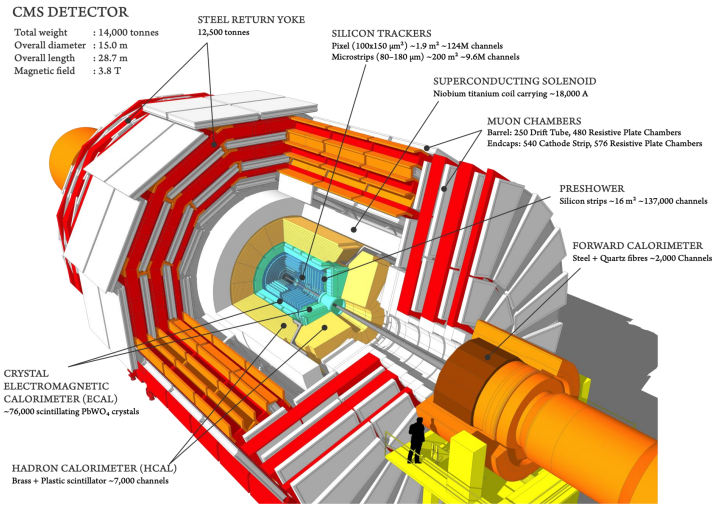

Figure 2.2: The CMS-Detector[2]

2.3 The concept of serial powering

Serial powering of the detector modules limits the total supply current to the maximum load current of a single module. In comparison to a parallel powering scheme, where the total supply current scales with the number of modules, this leads to a smaller amount of total current. On the other hand, a regulator circuitry is required to generate a constant supply voltage out of the constant current. Serial powering furthermore demands precautions for redundancy to avoid a total system malfunction in case of failure of one module. For this purpose, several regulators per module are driven in parallel to prevent a break in the serial power chain. To reduce thermal strain it is important to distribute power consumption equally across the chips and modules[7].

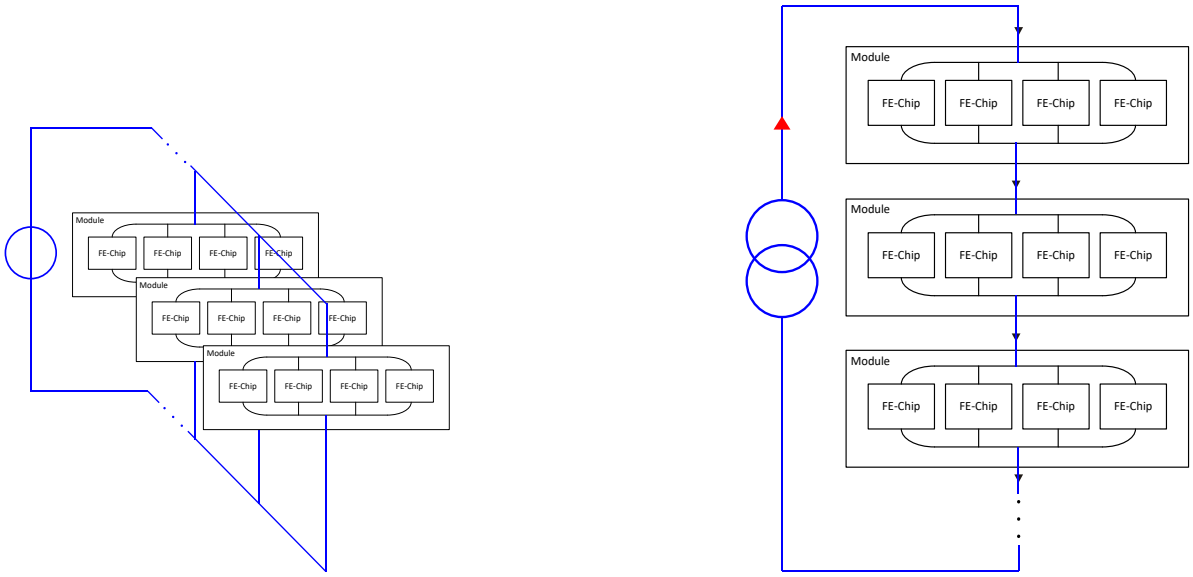

Figure 2.3: Serial and parallel powering scheme[3]

First approaches of the serial powering concept were based on a shunt regulator. A problem resulting from the parallel operation of several shunt regulators with a very steep voltage to current characteristic is an unbalanced current distribution across the regulators. Due to effects like variations in bandgap reference voltages, corner variation, ground shifts and resistor mismatches, parallel placed shunt regulators will not generate identical output voltages. A major part of the supply current will take path through the regulator with the lowest output voltage and may cause fatal damage due to thermal overload. To counteract this, a resistor can be added to the current input to decrease the current-voltage slope of the input voltage. As a consequence, the current distribution between parallel regulators is evened out. As a tribute the slope resistor decreases power efficiency. This leads to the concept of a Shunt-LDO regulator, which combines the functionality of an LDO voltage regulator for a constant output voltage and a shunt regulator to ensure a constant current flow through the regulator. The LDO operates similar to a variable resistance and hence as a substitution of the resistor which was implemented in the shunt regulator.

3 RD53B test chip C

3.1 SLDO Regulator

The SLDO regulator concept is based on two control loops which are supplied by a current source. First, the LDO regulator circuit generates a constant output voltage for the digital and analog components of the pixel detector modules. The second one is the shunt circuit that is used to control the current flow. Due to exposition to radiation , all used transistors have to feature a particular resistance against influences from this exposure. The TSMC 65 nm CMOS technology is used for the implementation, because this technology is characterized by a high radiation resistance. The circuitry is built up with thin gate oxide layer transistors, which should not be powered with voltages exceeding 1.32 V. The controller is supplied with a current of up to 2 A, resulting in a maximum input voltage of 2 V. To ensure that the voltage limit of each transistor is not topped out, the transistors are cascoded.

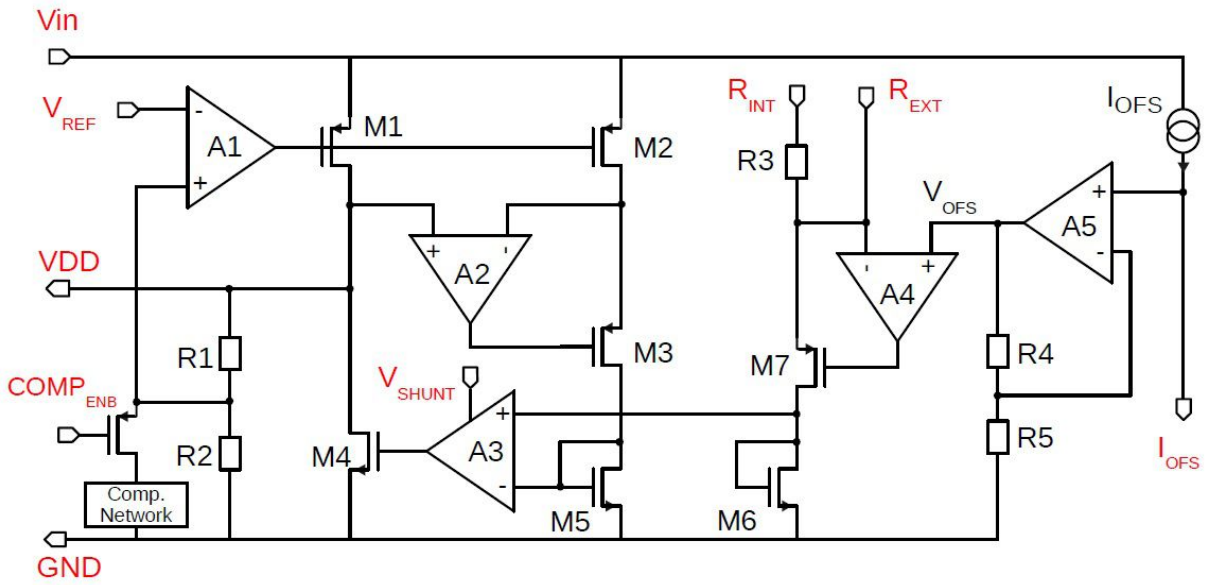

Figure 3.1: SLDO Regulator[4]

The LDO circuit on the left hand side is made up of the pass device M1, the operational amplifier A1 and the voltage divider with the resistors R1 and R2, which is used to set a specific voltage at the output. A desired reference voltage V_{ref}, generated by a bandgap circuit, is given to the inverting input of A1. The voltage divider returns half of the output voltage as a negative feedback back to the non-inverting input of A1. The amplifier determines the voltage difference between the two inputs and regulates the pass device to output twice the reference voltage at the regulator output. Transistors M1 and M2 form a current mirror to detect the current flow

through the pass transistor M1. A fraction of the current in a ratio of k:1 is mirrored to transistor M2 and is converted into a voltage by the transistor M5, which is given to the inverting input of A3. The amplifier controls the device M4 to drain current that does not flow through the load into ground or into the next module when serial connection is applied. The current through the transistor M6 serves as a reference current, which is defined by the resistor R3. If the input voltage V_{in} is higher than the offset voltage V_{ofs}, the generated reference current is linearly dependent on V_{in}. In case the current through device M5 is smaller than the reference current, M4 is controlled to ensure a higher current flow through it and vice versa. The amplifier A4 has a negative feedback path and operates as a virtual short circuit, i.e. M7 is driven to apply the offset voltage to the inverting input. The reference current is calculated accordingly:

$$I_{ref} = \frac{U_{in} - V_{ofs}}{R_3}$$

The amplifier A2 improves the accuracy of the current mirror and works, likewise A4, as a virtual short circuit. This means that the devices M1 and M2 have the same V_{GS} and V_{DS} voltage to reach a high current mirror accuracy with the short channel transistors, which have a relatively small output impedance. This is especially important during the start-up phase when the transistors are not yet saturated. Furthermore, this ensures an approximately even distribution of the current and is particularly significant for the operation of several, parallel connected chips. In addition, the offset voltage has an effect on the current distribution and backs up an optimization of the power consumption in case of a chip failure. For the simulation tests, the regulator will be supplied with a maximum input current up to 2 A. The digital and analog loads are reproduced by a resistor or a current source and can be set between 0 A and a maximum of 1 A. The reference voltage for the LDO circuit is specified to 600 mV and the offset voltage to 800 mV (for high-power mode, see. 3.1.1). Both voltages are generated by bandgap circuits. Assuming that the output voltage of the controller is twice the reference voltage, a value of 1.2 V is obtained. The external resistor to generate the reference current is set to 600 Ω and has to provide a low temperature drift and tolerance. Above an input voltage of 1.4 V all devices are in saturation and therefore the regulator is in steady state.[8, 11].

3.1.1 Low- & High-Power mode

During the installation- and maintenance process the chip is running without the full cooling capacity. For this purpose, a low-power mode with a higher offset voltage of 1.2 V is implemented to reduce current flow and therefore power consumption and thermal dissipation. In normal operating conditions, the chip is driven in a high-power mode with a specified offset voltage of 800 mV. To realize this switch between different voltages two serial resistors are used to generate the low-power offset voltage by the reference current. To setup the high-power mode one of the resistors is shorted to ground by an integrated transistor and the voltage drop decreases accordingly.

3.2 Bandgap Scheme

A bandgap circuit generates a reference voltage which operates with very small influence from its supply voltage and temperature. A constant reference is important for the regulator to generate the specified output voltage under all operating conditions. The bandgap scheme for the RD53-project demands special requirements: It needs to be operated with up to 2 V, although it is designed with thin-gate transistors. To assure this, all transistors are cascoded, like in most circuit parts of the RD53-chip. A further criterion is high radiation resistance. Because of this demand, the bandgap scheme can not be designed with diodes, which would cause the reference voltage to drift with radiation dose. An alternative concept is the usage of MOS-transistors operated in weak inversion, because in this operating region the characteristics are similar to diodes. The current through a transistor in weak inversion rises exponentially with U_{GS}. A disadvantage of MOS-transistors is their dependency on process corners, which will lead to an output voltage that is independent of the supply voltage and temperature, but is affected by process corner variations instead.

To compensate the influence of process corner variations, a trimming option is implemented with logic circuits. This conflicts with the demand of using operating voltages up to 2 V, because logic CMOS-circuitry, like inverters, are not able to withstand the resulting overvoltages. Therefore, two bandgap circuits are combined to fulfill all stated requirements. The preregulator bandgap is designed to operate at 2 V, but delivers low accuracy without trimming, with a total variation of up to ±25 mV, caused by all possible influences like temperature, supply voltage, mismatch and radiation. This variation is not suitable for the high-accuracy specifications of the pixel chip. However, this bandgap circuit is used as reference of a small LDO regulator which is called preregulator in the framework of this project and delivers an output voltage of 1.2 V. Due to the earlier mentioned variations the real output voltage of the preregulator is between 1.15 V and 1.25 V. This output voltage is used as supply voltage for a second bandgap circuit with higher precision. Furthermore, the above-mentioned voltage variation is adequate in the scope of the specifications for all circuits supplied by the preregulator due to their sufficient power supply rejection ration. In addition, it is possible to implement a trimming feature for the high precision bandgap based on CMOS logic since the supply voltage is not exceeding 1.25 V.

3.2.1 Implementation of trimming

The trimming of the core bandgap is realized with a reference current generator which converts a constant voltage delivered from the bandgap into a constant current. For this purpose, an external resistor R_{iref} is used to ensure temperature independence. The reference current generated this way is replicated with current mirrors and used for different applications inside the chip, for example to generate V_{ref} and V_{ofs}.

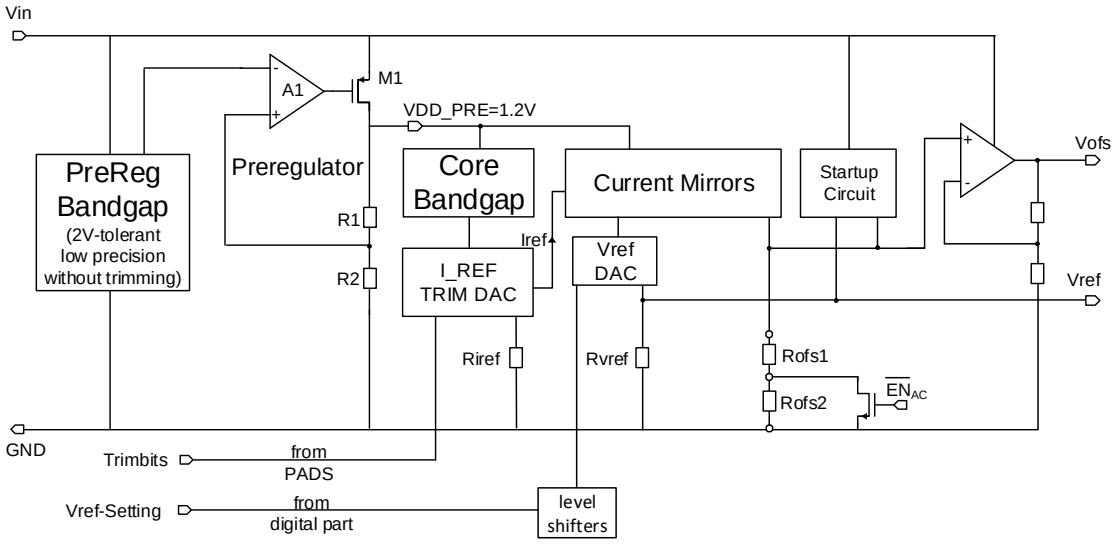

Figure 3.2: Bandgaps Scheme[4]

3.3 Overvoltage Protection

To protect the regulator from potentially destructive input voltages above 2 V a protection circuit is implemented. For this purpose, a shunt regulator with an PMOS pass device is used to provide an alternative path for supply currents currents up to 2 A at high supply voltages. This additional current flow limits the input voltage to 2 V. For any input voltages under 2 V the OVP is not active. The preregulator voltage of 600 mV is used as a reference on the non-inverting input. When the potential on the inverting input of the OP Amplifier is lower than the reference voltage on the non-inverting input the voltage difference between both inputs is positive. Due to the high gain factor of the amplifier the output voltage can reach high values up to the supply voltage. In this case, gate and source of the pass device have approximately the same potential and no current will flow through the transistor. When the feedback voltage, which is set by a voltage divider, exceeds 600 mV the voltage difference between the inputs is negative. This leads to a reduction of the amplifiers output voltage and as a result to a higher source-gate voltage of the PMOS pass device. The pass device now shunts a fraction of the input current to ground and the input voltage is limited to

$$V_{in} = V_{RefPre} \cdot (1 + \frac{R1}{R2})$$

The voltage divider is designed to deliver a voltage of 600 mV to the inverting input at an input voltage of 2 V.

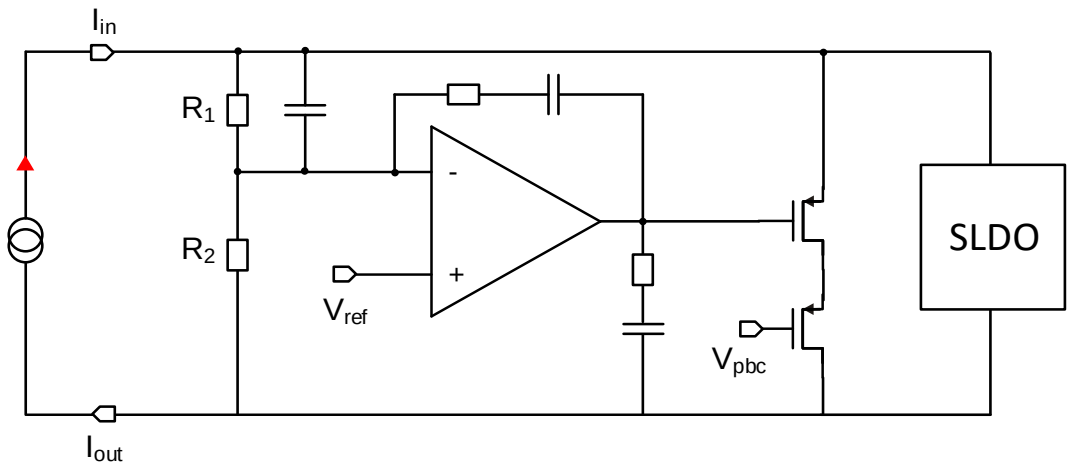

Figure 3.3: Overvoltage Protection[4]

3.4 Start-Up Circuit

During the start-up of the regulator the offset voltage V_{ofs} is 0 V. The consequence is a low input impedance of the regulator. To counteract this effect, the offset voltage is linked to the input voltage until the specified offset voltage has ramped up. As a result, the input resistance of the SLDO gets high-impedance. The goal of this feature is to bring the regulator in its specified operating point even with small input currents. Subsequent to the start-up phase, the regulator should be stable and able to maintain its designated operating parameters.

The reference current I_{ref}, which is used to generate the offset voltage through R_{ofs}, is not yet stable during start-up phase. The idea behind the circuit is to bring V_{ofs} close to the input voltage until ramp-up is complete. For that purpose, an additional current I_{extra} is used to compensate I_{ref}. This current has to be limited to the start-up phase because otherwise the specified reference current of 4 µA would be affected. The defined condition for the start-up circuit to shut down is an input voltage above 1 V.

This shutdown is realized with three current mirrors. A NMOS current mirror is implemented as a high-swing cascode with low-Vt transistors to ensure a faster current flow in comparison to the PMOS current mirror that is composed with two cascoded gate-drain connected transistors. Due to the serial circuit of two gate-drain connections, the left PMOS current mirror switches

to the active state under following condition :

$$2 \cdot U_{dsat} + 2 \cdot U_{th}$$

The NMOS current mirror in comparison demands less voltage due to its high-swing characteristics:

$$2 \cdot U_{dsat} + U_{th,lvt}$$

In addition, the threshold voltages are smaller as a consequence of the use of lvt transistors. The mirrored current I_{startN} from the NMOS part can not flow into the first PMOS part and hence is conducted through the second PMOS current mirror which is, likewise the NMOS part, implemented as a high-swing cascode with lvt-transistors. The current is then mirrored into R_{ofs}. When the input voltage has risen to values above 1.2 V that are large enough to deliver the specified reference current of 4 µA, the first PMOS current mirror switches to active and the current I_{startP} can flow. The resistors are dimensioned to deliver a current which is higher than I_{startN}, so current from the NMOS part gets soaked up from the now active PMOS current mirror. As a consequence, the current through the high-swing PMOS part I_{extra} is zero and the start-up circuit has shut down.

A further problem are oscillations, which occur for low offset voltages. For specific values of V_{ofs} the input voltage can be below 1 V. The start-up circuit will be active until V_{in} reaches 1 V and will then switch off. As a result, V_{ofs} drops to its nominal value which, for small input currents, means that the input voltage is reduced to values smaller than 1 V. For this reason, the start-up circuit switches on again which result in an oscillation behavior. These oscillations continues until the input current is high enough to keep V_{in} above 1 V even if the start-up circuit is not active. To counteract this, the preregulator reference voltage is used as a further criterion for the shutdown of the start-up circuit. V_{refPre} is linked to the gates of two NMOS transistors. When the preregulator bandgap reaches its operating point of 600 mV, these transistors will short the left-sided transistors of the NMOS high-swing current mirror and hence interrupt the current flow. A disadvantage of this solution is that the circuit is not able to reach the nominal operating point for some corners and start-up fails.

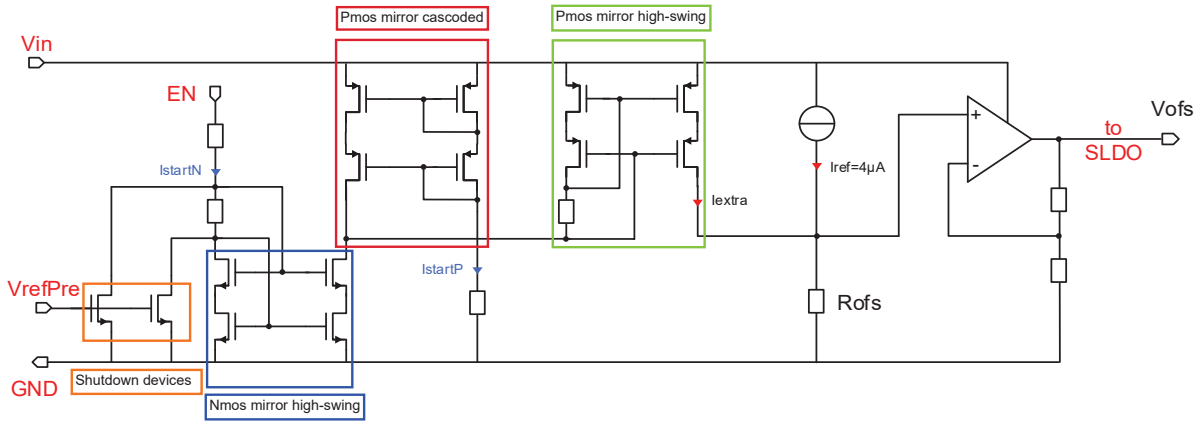

Figure 3.4: Start-Up circuit[4]

3.5 Specifications

Technical Specifications	
Input Voltage (LDO Mode)	1.4 V - 2 V
Input Current (Shunt Mode)	max. 2 A
Load Current	max. 1 A
Output Voltage (configurable)	0.7 V - 1.2 V
Output Capacity	min. 2.2 µF
Input Capacity	6 µF
Line Regulation (LDO Mode Vin 1.4 V (Shunt Mode Iin 1 A - 2 A)	<10 mV
Load Regulation (load range between 0 A and 1 A)	<10 mV
Static Output Variation after Trimming	<10 mV
Static Output Variation at Nominal Load: $\lvert\Delta Vout\rvert$	<10 mV
Dynamic Output Voltage Variation at Load Transient: $\frac{\Delta Iload}{\Delta trise}$	± 30 mV

Table 1: Specification of the Controller[11]

4 Simulation Results

The following chapter shows the simulation results of the regulator in various operating conditions. For this purpose, a test bench was built with the Cadence Virtuoso software. All simulations consider the process variations (ff, ss, fs, sf, tt) of the transistors and prove the functionality of the circuit for different temperature conditions $-40\,°C$, $-20\,°C$, $27\,°C$, $60\,°C$. This covers the functionality of the circuits in a wide range of possible scenarios. In the chapters 4.11 and 4.12 the circuit is operated with a piece-wise linear current source (ipwlf). This allows to create a transient current waveform with time-current values that can be set manually. The file path of the pwl-file is entered in the source settings. By modifying the source it is possible to adjust it so that the filename can be stored in a design variable. By doing this, a single schematic can be used to run several simulations with different load profiles. In the corner settings different load profiles can be added[9].

4.1 Trimming

Due to variations in process corners the reference current differs between the chips. Therefore, a trimming option similar to the one in the bandgap circuit [3.2] is implemented. An Iref-Generator circuit is supplied with the output voltage of the trimmable core bandgap, which is the reference voltage. A 4-Bit digital word *IrefSet<3:0>* is used as an input of the current generator to adjust the reference current accordingly to the occurring variations. The 4-Bit word implies that there are 16 different trimming settings. The parameter is determined with a transient simulation of the offset voltage under the following conditions: The trimming process is individually executed

- Simulation time: 15 ms
- Temperature: 27 °C
- Process variations: ff, ss, fs, sf, tt
- rload : 1.2 GΩ
- iRefSet: 0 to 15
- itpower: 1 A
- rise-time: 10 µs

for every chip at room temperature. This can limit the accuracy of the trimming for different temperatures, regardless an individual trimming for all specified operating temperatures is not applicable. The transient simulation examines the offset voltage for all process variations and presents the value for iRefSet with a offset voltage closest to the specified 800 mV. Fig. 4.1 to 4.5 visualize the trimming process.

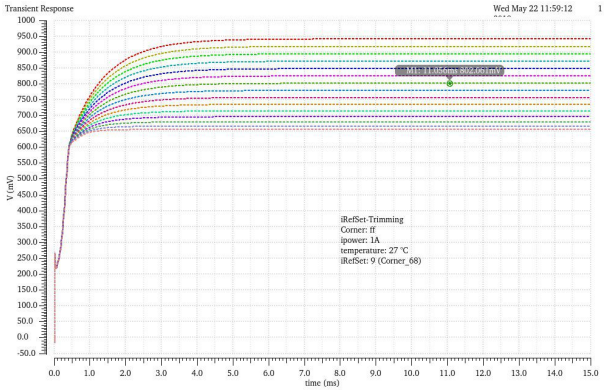

Figure 4.1: Trimming at 27 °C for ff-corner

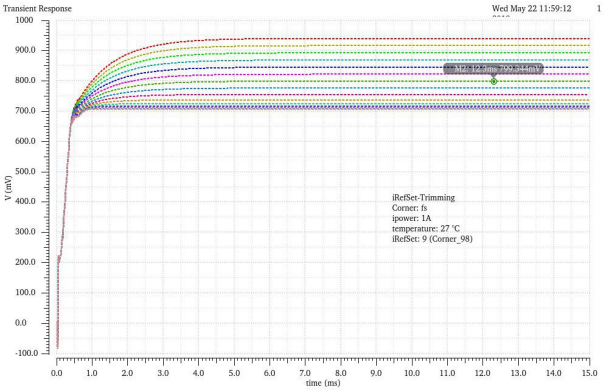

Figure 4.2: Trimming at 27 °C for fs-corner

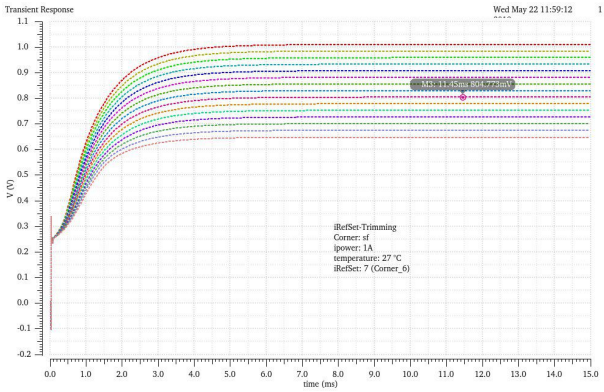

Figure 4.3: Trimming at 27 °C for sf-corner

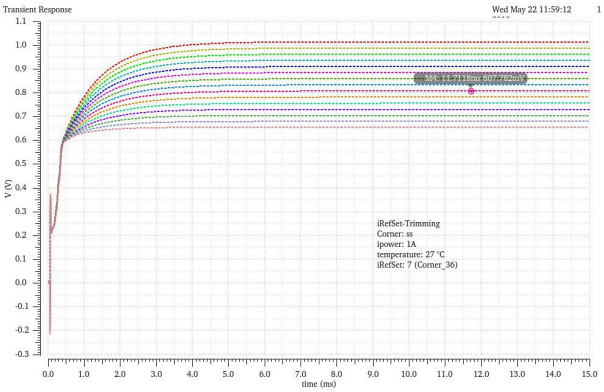

Figure 4.4: Trimming at 27 °C for ss-corner

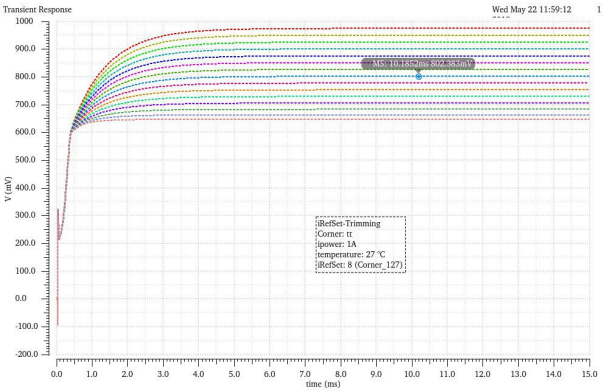

Figure 4.5: Trimming at 27 °C for tt-corner

Table 2 shows the determined values for the trimming-parameter iRefSet and the offset voltage according to the simulation:

Corner	iRefSet	Vofs
ff	9	802.06 mV
fs	9	799.34 mV
sf	7	804.77 mV
ss	7	807.78 mV
tt	8	802.38 mV

Table 2: Values for iRefSet and V_{ofs} over all process corners

4.2 Handling of convergence issues and the use of nodeset files

During the development of the test bench and the first simulation runs, a severe problem with convergence could be observed. Due to the increased complexity of the SLDO circuitry, the algorithm of the Cadence simulator had massive difficulties to calculate DC-solutions for the circuit and therefore to find an operating point. This leads to tests with a large amount of simulation errors up to a threshold where results could not longer be considered as valid. Dealing with this issue was not trivial and demanded a high amount of effort while setting up the test bench. After many approaches, the use of precalculated nodeset files exposed to be the best way to reach acceptable simulation results, nevertheless this problem still cannot be rated as completely solved. There can be issues left, especially when it comes to dc-sweep based simulations.

To generate the nodeset-files, a transient analysis is used to calculate an operating point and save it to a textfile. Transient simulations have significantly less problems to achieve convergence and can therefore be used to calculate an initial condition for a subsequent dc-analysis. Figures 4.6 and 4.7 show the setup process for creating nodeset files in the simulation options of ADE-XL.

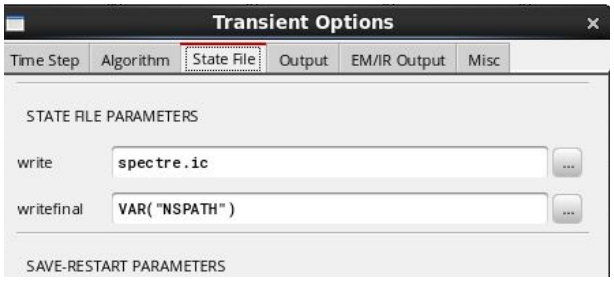

Figure 4.6: Settings to write a nodeset file

Figure 4.7: Settings to read a nodeset file

The analysis option in the test editor of ADE-XL offers the possibility to consign a file path to write and read external data. If only a single simulation with a fixed set of parameters is used, this method is sufficient. The test bench for the SLDO verification however uses a vast amount of different conditions like corners and temperatures. Convergence characteristics are different across all corners and temperatures and for this reason, an individual nodeset file for at least every temperature-corner combination is required. This results in a total of 20 different nodesets. For maximum optimization even more files could be generated by additionally considering the input current and all four specified load currents. As this would generate 160 independent nodeset files, it is not feasible in the work of this thesis. To provide an individual nodeset for every combination of process corner and temperature, all cases must be simulated separately. That means that every test has at least 20 different corner setups, which is the main reason for the high complexity of this test bench.

An important target was to use the nodeset files similar to a design variable in Cadence, as this would ensure an efficient and reliable way to cover all conditions. To do so, the complete file path in figure 4.7 must be stored in a global variable, which then is used in the corner setup. This variable can be used for the read- and write path settings. In addition to that, a global variable must be set to the path of the folder where the nodeset files are saved. This folder has then again to be listed in the simulation files of ADE-XL 4.8.

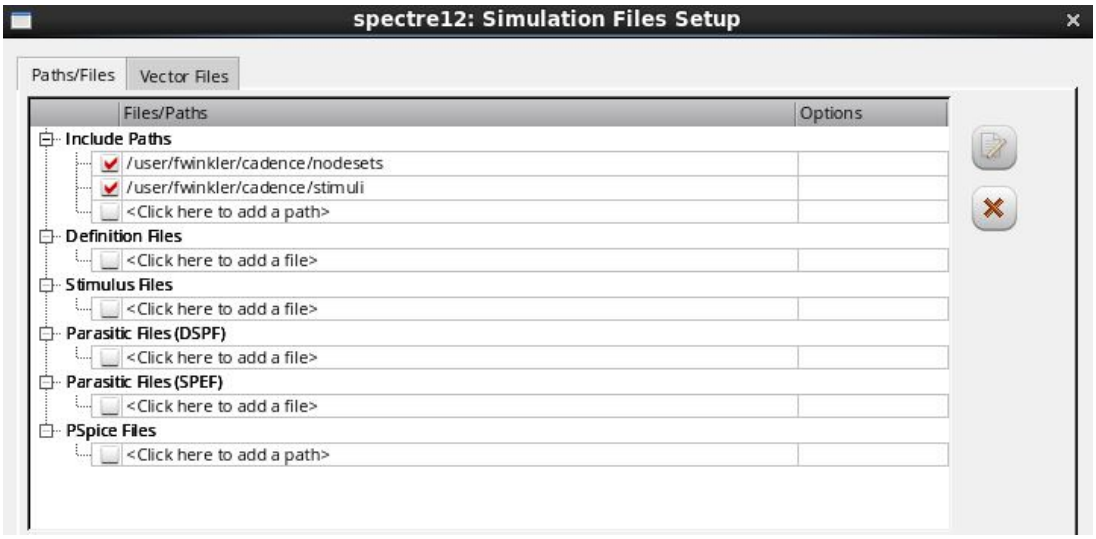

Figure 4.8: Setup for external simulation file paths in ADE-XL

Although this method is quite tedious, it is currently the best option to achieve better simulation results for the SLDO circuit. After a consultation of the Cadence support it was confirmed that the software itself does not offer any possibility to automatize the described process.

4.3 Temperature Sweep

To determine the influence of temperature variations on the regulator, a transient simulation with an input current of 1 A, a load resistance of 1.2 GΩ and a temperature sweep from −40 °C to 60 °C is performed. The main voltages of the chip (V_{in}, V_{out}, V_{ref} and V_{ofs}) are observed for all process corners. Figures 4.9 to 4.13 visualize the results.

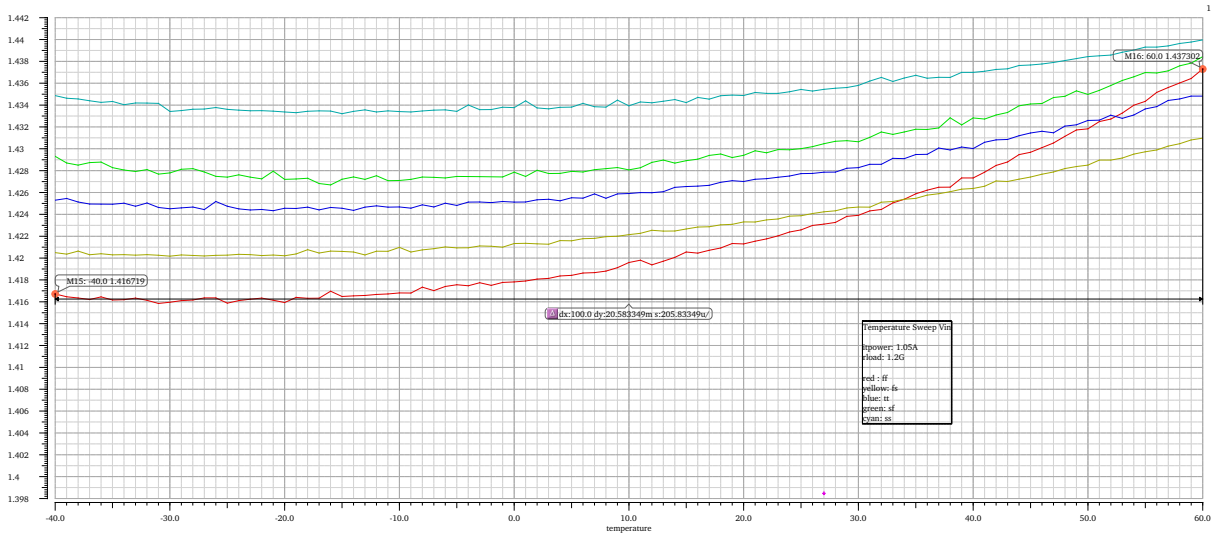

Figure 4.9: Temperature sweep V_{in}

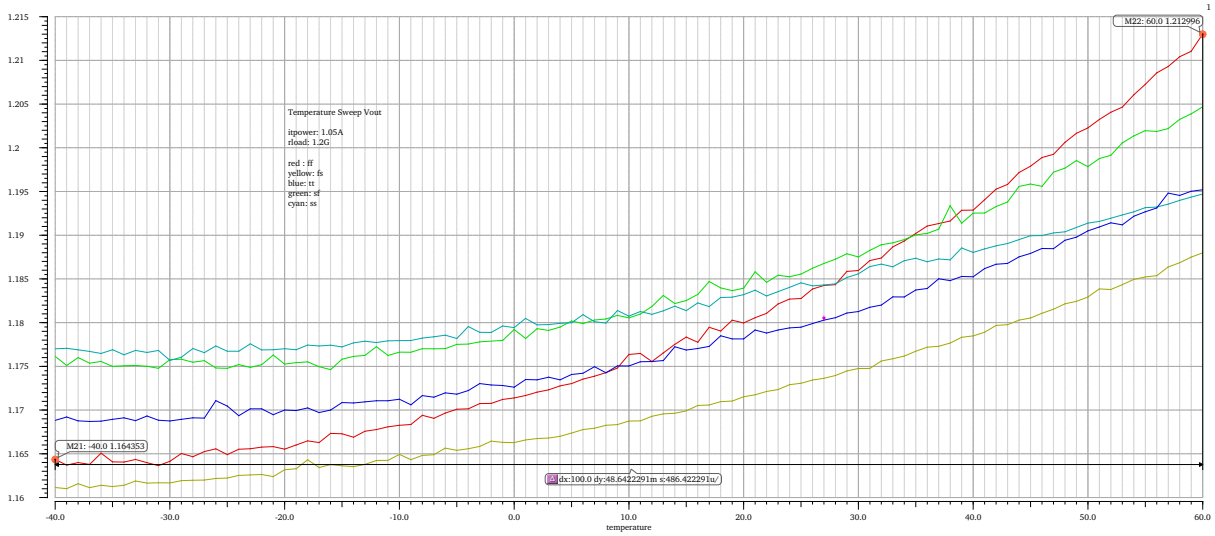

Figure 4.10: Temperature sweep V_{out}

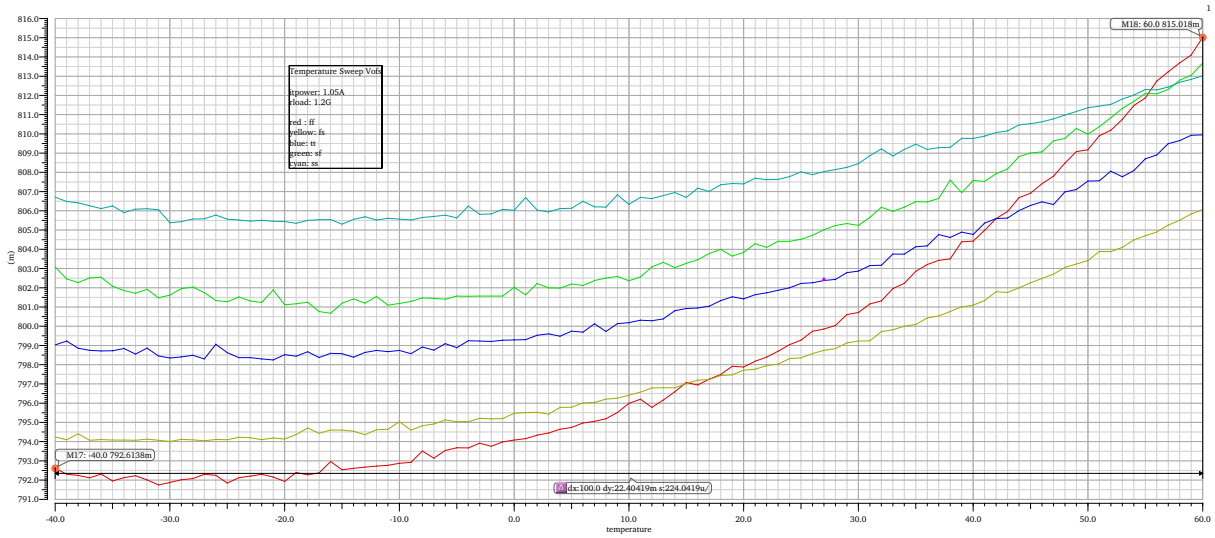

Figure 4.11: Temperature sweep V_{ofs}

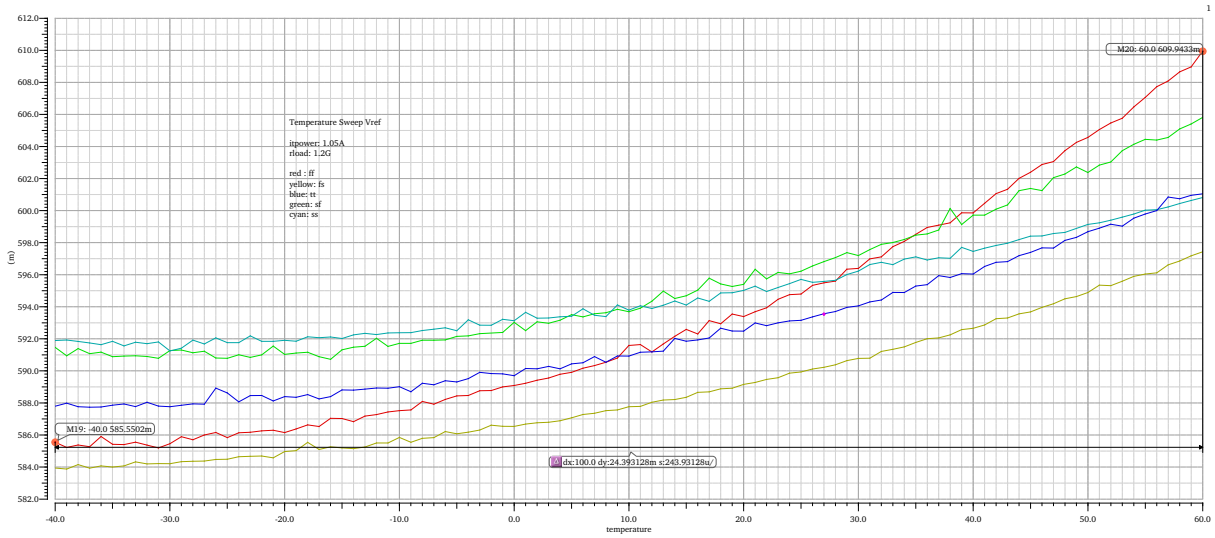

Figure 4.12: Temperature sweep V_{ref}

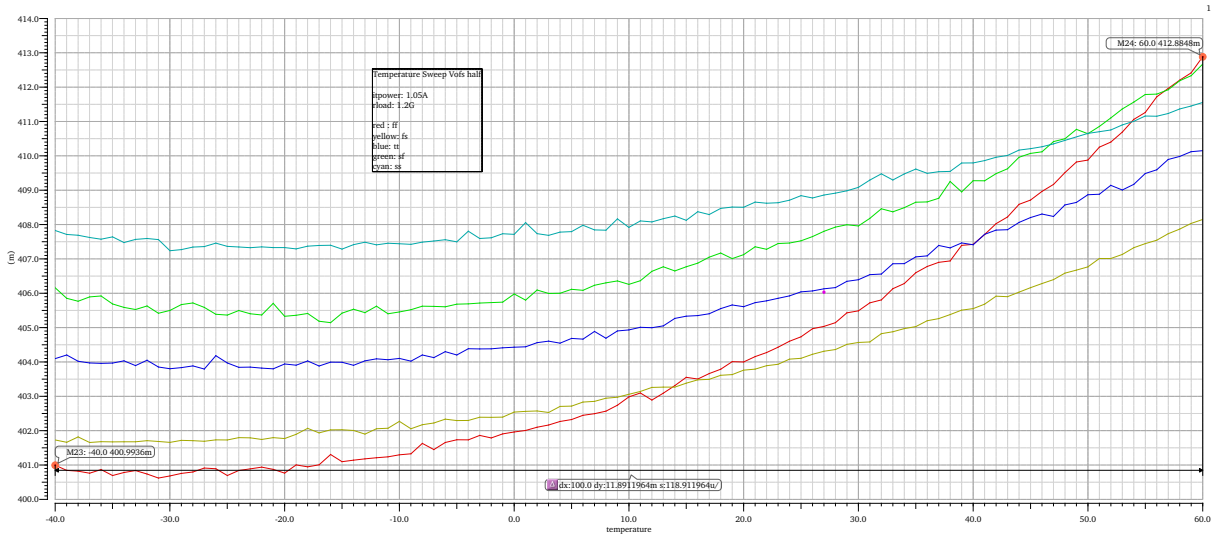

Figure 4.13: Temperature sweep $V_{ofshalf}$

Table 3 summarizes the temperature drift for every signal across all process corners.

	ff	**fs**	**sf**	**ss**	**tt**
Vin	20.58 mV	10.47 mV	9.12 mV	5.1 mV	9.53 mV
Vout	48.64 mV	26.85 mV	28.55 mV	17.70 mV	26.37 mV
Vref	24.39 mV	13.48 mV	14.35 mV	8.92 mV	13.26 mV
Vofs	22.40 mV	11.81 mV	10.60 mV	6.31 mV	10.92 mV
Vofshalf	11.89 mV	6.42 mV	6.51 mV	3.72 mV	6.05 mV

Table 3: Temperature variation for all corners

4.4 Voltage Limits

This simulation examines the voltage limits of the devices, which are confined by the specifications of the utilized 65 nm node from TSMC. The technology is designed for voltages up to 1.32 V (NMOS), respectively −1.32 V (PMOS). To prevent the devices from breakthrough and overvoltage damage, it is necessary to keep V_{DS}, V_{GS} and V_{GD} voltages within these specifications. The simulation is implemented across all process corners with the following parameters:

- ipower: 1.05 A, 2 A
- rload : 1.2 GΩ, 240 Ω, 12 Ω, 1.2 Ω
- Temperatures: −40 °C, −20 °C, 27 °C, 60 °C
- Process variations: ff, ss, fs, sf, tt

Check asserts can be used to detect device overvoltages. Conditions are defined for V_{DS}, V_{GS}

and V_{GD} equally, which check all adjusted operating parameters and report voltage overloads. The following conditions are set:

- v(g,s) > 1.32 || v(g,s) < -1.32
- v(g,d) > 1.32 || v(g,d) < -1.32
- v(d,s) > 1.32 || v(d,s) < -1.32

Table 4 shows the results of the simulation and provides information about where voltages are exceeding their specific limits. Problems can be recognized in instance *I10*, which is the Start-Up circuit for the offset voltage, where devices like the transistor *M15* reach a V_{DS} up to 1.61 V (ss-corner, −40 °C). Further violations occur for the power transistors and the control of the overvoltage protection (instance *I13, I17, I20 I24, I30*) and in instance *I38*, which is the error amplifier to improve the accuracy of the offset voltage. The specific devices can be determined with the given instance names in the Cadence schematic of testchip C. There are issues with simulation errors for some corners with specific temperatures due to the lack of calculating an operating point. The usage of transient nodeset files, like described in section 4.2, improves this situation.

Instance	Violations	Model	Maximum	Occurrences	Conditions for maximum
/I0/I20/I0/M2	32	nch	v(d, s) = 1.58165	sf, ss - all temps, all loads, ipower 2 A	−40 °C, ss_lib, 2 A, 1.2 GΩ, 240
/I0/I0/I38/M6	32	pch	v(d, s) = -1.44426	fs, ss, tt - all temps, all loads, ipower 2 A	−40 °C, ss_lib, 2 A, 1.2 GΩ, 240
/I0/I863/I10/M11	128	pch	v(g, d) = -1.41467, v(g, s) = -1.41467	fs, sf, ss, tt - all temps, all loads, ipower 2 A	−40 °C, ss_lib, 2 A, 1.2 GΩ
/I0/I863/I10/M12	126	pch	v(g, d) = -1.41229, v(g, s) = -1.41229	fs, sf, ss, tt - all temps, all loads, ipower 2 A	−40 °C, ss_lib, 2 A, 240 Ω
/I0/I863/I10/M13	42	pch_lvt	v(d, s) = -1.36959	fs, sf , ss, tt - all temps, all loads, ipower 2 A	−20 °C, ss_lib, 2 A, 1.2 GΩ
/I0/I863/I10/M15	72	nch_lvt	v(d, s) = 1.61441	all corners, all temps, all loads, ipower 2 A	−40 °C, ss_lib, 2 A, 1.2 GΩ
/I0/I863/I10/M26	127	pch	v(g, d) = -1.41129, v(g, s) = -1.41467	fs, sf, ss, tt - all temps, all loads, ipower 2 A	−40 °C, ss_lib, 2 A, 240 Ω
/I0/I863/I10/M30	140	pch_lvt	v(d, s) = -1.54479, v(g, d) = 1.50258	all corners, all temps, ipower 2 A	−40 °C, ss_lib, 2 A, 1.2 GΩ, 240
/I0/I13/M0[0:4]	60	pch_hvt	v(d, s) = -1.34312	sf (27 °C and 60 °C), ss (60 °C) - all loads, ipower 2 A	60 °C, sf_lib, 2 A, 12 Ω
/I0/I17/M0[0:4]	60	pch_hvt	v(d, s) = -1.34312	sf (27 °C and 60 °C), ss (60 °C) - all loads, ipower 2 A	60 °C, sf_lib, 2 A, 12 Ω
/I0/I24/M0[0:4]	60	pch_hvt	v(d, s) = -1.34312	sf (27 °C and 60 °C), ss (60 °C) - all loads, ipower 2 A	60 °C, sf_lib, 2 A, 12 Ω
/I0/I30/M0[0:4]	60	pch_hvt	v(d, s) = -1.34312	sf (27 °C and 60 °C), ss (60 °C) - all loads, ipower 2 A	60 °C, sf_lib, 2 A, 12 Ω

Table 4: Device checks with maximum values

4.5 Load Transients

Load transients shall simulate the regulator's behavior during load changes. If the load current increases or decreases abruptly, the output voltage will drop or rise accordingly. This test examines how fast the controller returns to its steady state and furthermore determines the positive and negative peaks of the output voltage. A current source is used to draw a stable load current, which changes from 0 A to 500 mA and additionally from 250 mA to 750 mA. Rise and fall times are set to 1 ns to model fast switching frequencies, which can appear in the digital part of the chip. Negative voltage peaks occurs when the load current increases rapidly and can be calculated by the delta of the peak- and the steady voltage. Y_{min} covers the negative peaks, while the positive ones are saved in the variable Y_{max}. Positive voltage peaks are observed for fast load current drops. To calculate the correct minimum and maximum voltage value *ymin* and *ymax*, Cadence calculator functions are used[11]:

$$Y_{min} = \text{value}(\text{VT}(\text{"/Vout"})\ \text{5e-07}) - \text{ymin}(\text{VT}(\text{"/Vout"})) \tag{4.1}$$

$$Y_{max} = \text{ymax}(\text{VT}(\text{"/Vout"})) - \text{value}(\text{VT}(\text{"/Vout"})\ \text{5e-07}) \tag{4.2}$$

The settled value for V_{out} is interpolated at 0.5 µs transient simulation time. Other parameters are set as follows:

- ipower: 1.05 A, 2 A
- iload : 250 mA to 750 mA and from 0 A to 500 mA
- Temperatures: −40 °C, −20 °C, 27 °C, 60 °C
- Process variations: ff, ss, fs, sf, tt

The plots 4.14 to 4.17 show the behavior of the output voltage. The voltage peaks *ymin* and *ymax* are around 25 mV in average for the negative amplitude and around 29 mV for the negative peak in most corners. The maximum values of 30.12 mV (*ymin*) and 36.36 mV (*ymax*) are reached with −40 °C, 1.05 A, ss-corner and a load switch from 250 mA to 750 mA. Variations occur for the different input currents of 1.05 A and 2 A, which is a result of different voltage drops across the wire bonds of the chip[11]. Furthermore, it can be observed that the output voltage has variations from around 47 mV up to 51 mV. This is a consequence of the temperature drift of all chip voltages, which is illustrated in section 4.3.

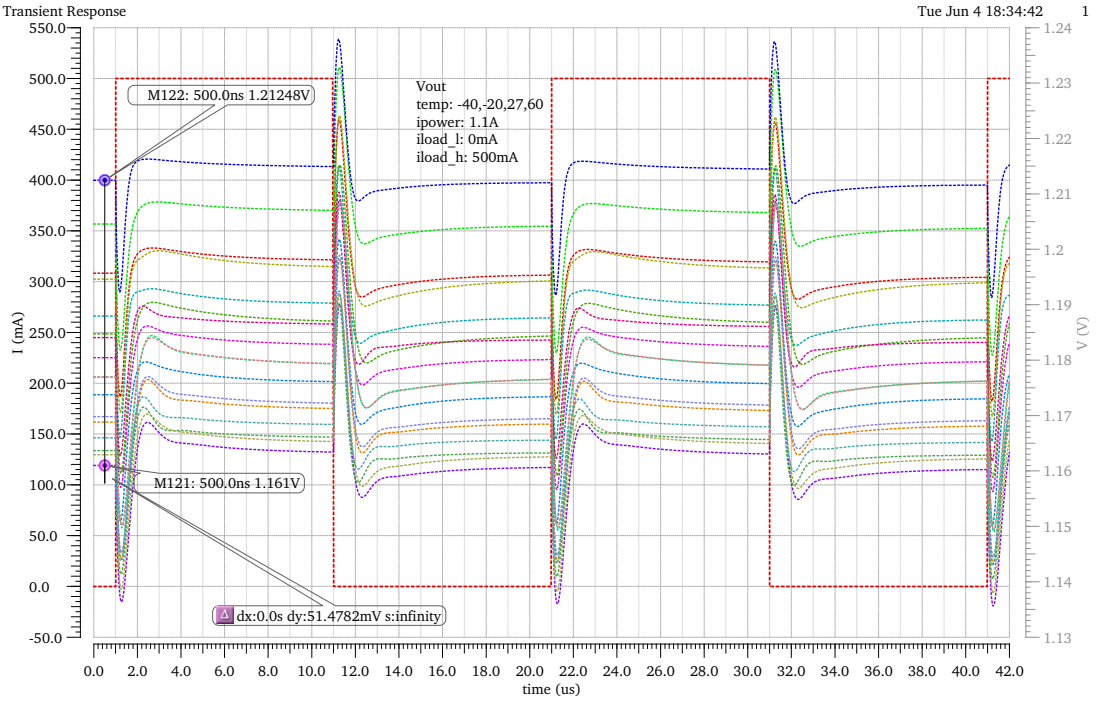

Figure 4.14: Load Transients for ipower = 1.05 A and iload from 0 A to 500 mA

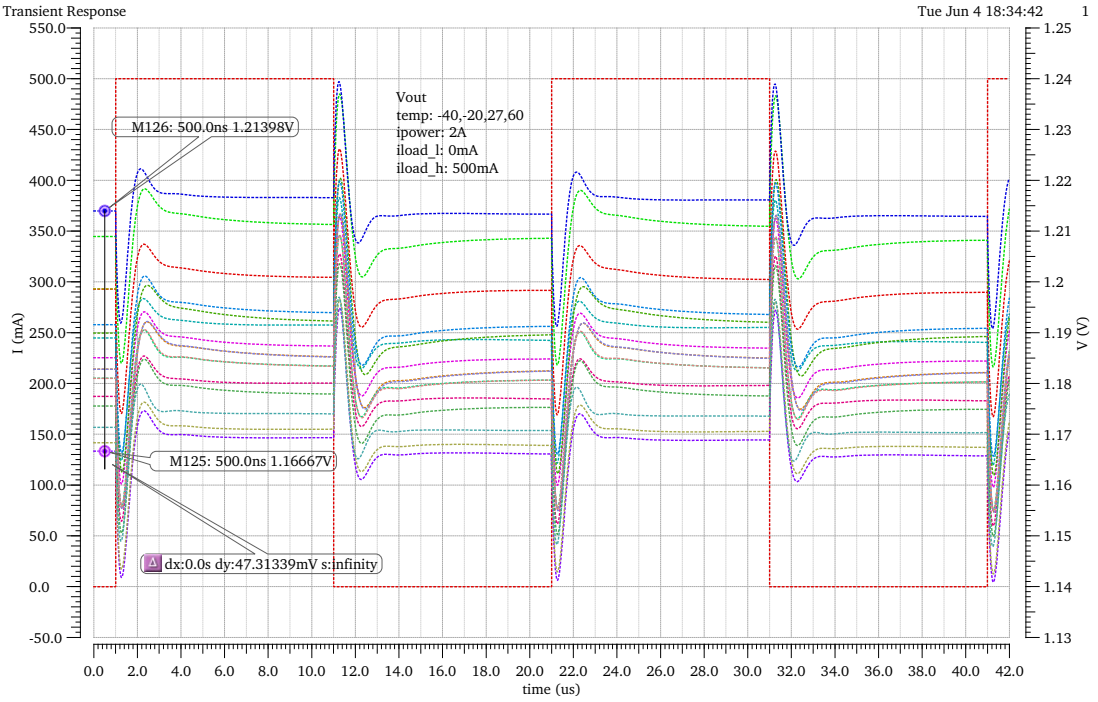

Figure 4.15: Load Transients for ipower = 2 A and iload from 0 A to 500 mA

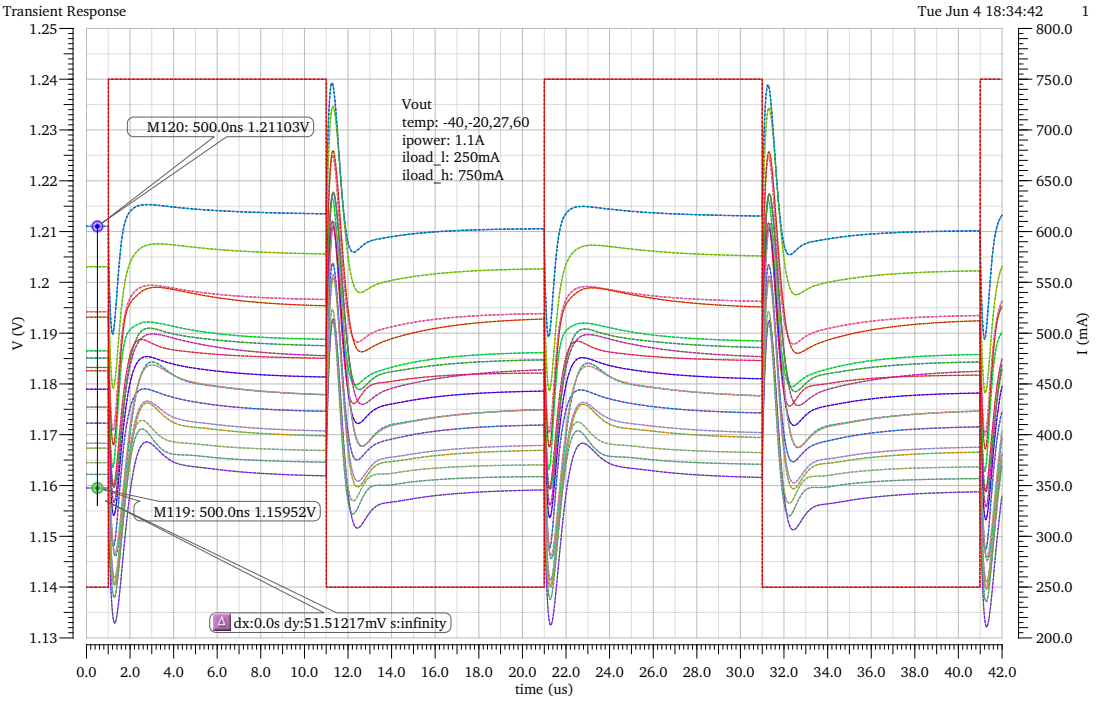

Figure 4.16: Load Transients for ipower = 1.05 A and iload from 250 mA to 750 mA

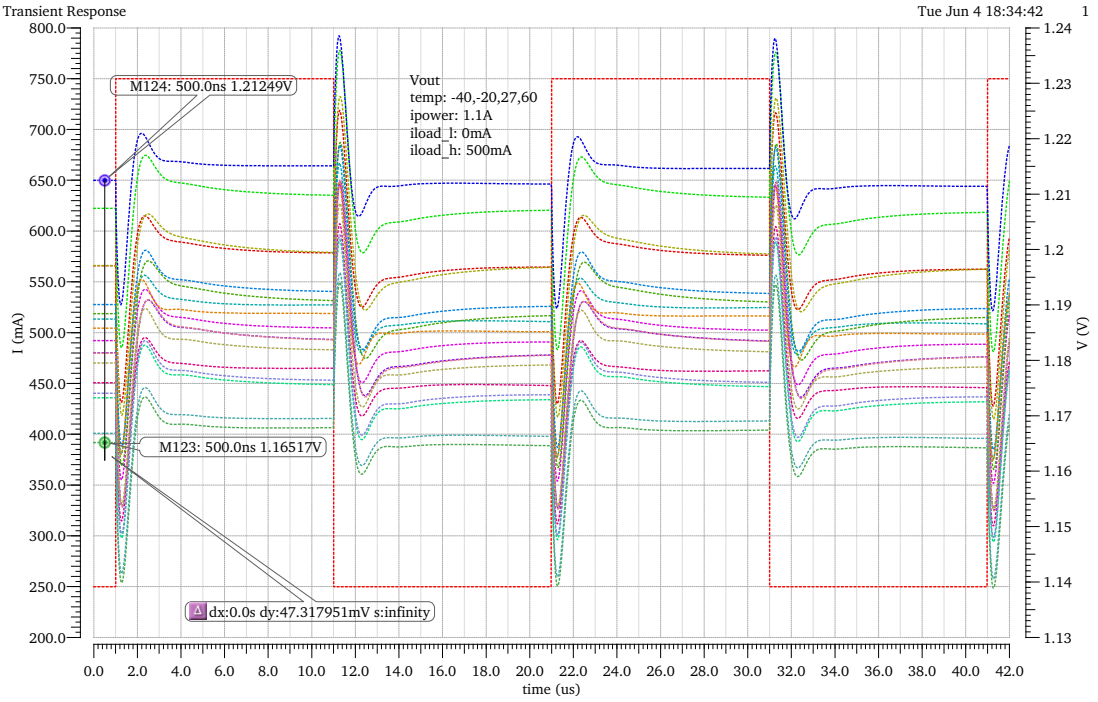

Figure 4.17: Load Transients for ipower = 2 A and iload from 250 mA to 750 mA

Table 5 shows the calculated voltage peaks for the values Y_{min} and Y_{max} for all specified operating parameters:

Corner	Ilhigh	Illow	ipower	Temp	Process	Ymin	Ymax
CDynamicLoad_-40_ff_0	0.5	0	1.05	-40	ff_lib	23.19e-3	26.56e-3
CDynamicLoad_-40_fs_0	0.5	0	1.05	-40	fs_lib	25.37e-3	29.15e-3
CDynamicLoad_-40_sf_0	0.5	0	1.05	-40	sf_lib	25.85e-3	29.33e-3
CDynamicLoad_-40_tt_0	0.5	0	1.05	-40	tt_lib	25.64e-3	29.26e-3
CDynamicLoad_-20_ff_0	0.5	0	1.05	-20	ff_lib	23.07e-3	26.57e-3
CDynamicLoad_-20_fs_0	0.5	0	1.05	-20	fs_lib	25.03e-3	28.97e-3
CDynamicLoad_-20_sf_0	0.5	0	1.05	-20	sf_lib	25.67e-3	29.3e-3
CDynamicLoad_-20_ss_0	0.5	0	1.05	-20	ss_lib	27.53e-3	31.6e-3
CDynamicLoad_-20_tt_0	0.5	0	1.05	-20	tt_lib	25.39e-3	29.16e-3
CDynamicLoad_27_ff_0	0.5	0	1.05	27	ff_lib	22.26e-3	26.26e-3
CDynamicLoad_27_fs_0	0.5	0	1.05	27	fs_lib	23.69e-3	28.07e-3
CDynamicLoad_27_ss_0	0.5	0	1.05	27	ss_lib	25.93e-3	30.54e-3
CDynamicLoad_27_tt_0	0.5	0	1.05	27	tt_lib	24.23e-3	28.51e-3
CDynamicLoad_60_ff_0	0.5	0	1.05	60	ff_lib	21.18e-3	25.48e-3
CDynamicLoad_60_fs_0	0.5	0	1.05	60	fs_lib	22.66e-3	27.15e-3
CDynamicLoad_60_sf_0	0.5	0	1.05	60	sf_lib	23.65e-3	28.31e-3
CDynamicLoad_60_tt_0	0.5	0	1.05	60	tt_lib	23.17e-3	27.69e-3

Corner	Ilhigh	Illow	ipower	Temp	Process	Ymin	Ymax
CDynamicLoad_-40_fs_1	0.5	0	2	-40	fs_lib	25.8e-3	28.19e-3
CDynamicLoad_-40_sf_1	0.5	0	2	-40	sf_lib	25.91e-3	28.12e-3
CDynamicLoad_-40_ss_1	0.5	0	2	-40	ss_lib	28.11e-3	30.53e-3
CDynamicLoad_-20_ff_1	0.5	0	2	-20	ff_lib	23.49e-3	25.65e-3
CDynamicLoad_-20_fs_1	0.5	0	2	-20	fs_lib	25.83e-3	28.27e-3
CDynamicLoad_-20_sf_1	0.5	0	2	-20	sf_lib	26e-3	28.23e-3
CDynamicLoad_-20_ss_1	0.5	0	2	-20	ss_lib	28.19e-3	30.62e-3
CDynamicLoad_-20_tt_1	0.5	0	2	-20	tt_lib	25.69e-3	28e-3
CDynamicLoad_27_fs_1	0.5	0	2	27	fs_lib	25.52e-3	28.05e-3
CDynamicLoad_27_sf_1	0.5	0	2	27	sf_lib	25.93e-3	28.24e-3
CDynamicLoad_27_ss_1	0.5	0	2	27	ss_lib	28.01e-3	30.49e-3
CDynamicLoad_27_tt_1	0.5	0	2	27	tt_lib	25.51e-3	27.9e-3
CDynamicLoad_60_ff_1	0.5	0	2	60	ff_lib	23.16e-3	25.47e-3
CDynamicLoad_60_fs_1	0.5	0	2	60	fs_lib	25.04e-3	27.64e-3
CDynamicLoad_60_sf_1	0.5	0	2	60	sf_lib	25.67e-3	28.05e-3
CDynamicLoad_60_ss_1	0.5	0	2	60	ss_lib	27.67e-3	30.16e-3
CDynamicLoad_60_tt_1	0.5	0	2	60	tt_lib	25.15e-3	27.6e-3
CDynamicLoad2_-40_ff_0	0.75	0.25	1.05	-40	ff_lib	25.08e-3	30.33e-3
CDynamicLoad2_-40_fs_0	0.75	0.25	1.05	-40	fs_lib	27.38e-3	33.3e-3
CDynamicLoad2_-40_ss_0	0.75	0.25	1.05	-40	ss_lib	30.12e-3	36.36e-3
CDynamicLoad2_-20_ff_0	0.75	0.25	1.05	-20	ff_lib	24.83e-3	30.19e-3
CDynamicLoad2_-20_fs_0	0.75	0.25	1.05	-20	fs_lib	26.88e-3	32.94e-3
CDynamicLoad2_-20_sf_0	0.75	0.25	1.05	-20	sf_lib	27.65e-3	33.39e-3
CDynamicLoad2_-20_ss_0	0.75	0.25	1.05	-20	ss_lib	29.56e-3	35.99e-3
CDynamicLoad2_-20_tt_0	0.75	0.25	1.05	-20	tt_lib	27.33e-3	33.2e-3
CDynamicLoad2_27_ff_0	0.75	0.25	1.05	27	ff_lib	23.63e-3	29.48e-3
CDynamicLoad2_27_fs_0	0.75	0.25	1.05	27	fs_lib	25.05e-3	31.47e-3
CDynamicLoad2_27_sf_0	0.75	0.25	1.05	27	sf_lib	26.29e-3	32.65e-3
CDynamicLoad2_27_ss_0	0.75	0.25	1.05	27	ss_lib	27.46e-3	34.34e-3
CDynamicLoad2_27_tt_0	0.75	0.25	1.05	27	tt_lib	25.71e-3	32.05e-3
CDynamicLoad2_60_ff_0	0.75	0.25	1.05	60	ff_lib	22.21e-3	28.27e-3
CDynamicLoad2_60_fs_0	0.75	0.25	1.05	60	fs_lib	23.72e-3	30.07e-3
CDynamicLoad2_60_sf_0	0.75	0.25	1.05	60	sf_lib	24.88e-3	31.57e-3
CDynamicLoad2_60_ss_0	0.75	0.25	1.05	60	ss_lib	25.97e-3	32.8e-3
CDynamicLoad2_60_tt_0	0.75	0.25	1.05	60	tt_lib	24.32e-3	30.79e-3
CDynamicLoad2_-40_fs_1	0.75	0.25	2	-40	fs_lib	26.26e-3	28.94e-3
CDynamicLoad2_-40_sf_1	0.75	0.25	2	-40	sf_lib	26.27e-3	28.71e-3
CDynamicLoad2_-40_ss_1	0.75	0.25	2	-40	ss_lib	28.42e-3	31.09e-3

Corner	Ilhigh	Illow	ipower	Temp	Process	Ymin	Ymax
CDynamicLoad2_-40_tt_1	0.75	0.25	2	-40	tt_lib	26.01e-3	28.51e-3
CDynamicLoad2_-20_fs_1	0.75	0.25	2	-20	fs_lib	26.28e-3	28.99e-3
CDynamicLoad2_-20_sf_1	0.75	0.25	2	-20	sf_lib	26.34e-3	28.81e-3
CDynamicLoad2_-20_ss_1	0.75	0.25	2	-20	ss_lib	28.45e-3	31.16e-3
CDynamicLoad2_-20_tt_1	0.75	0.25	2	-20	tt_lib	26.03e-3	28.58e-3
CDynamicLoad2_27_fs_1	0.75	0.25	2	27	fs_lib	25.86e-3	28.68e-3
CDynamicLoad2_27_sf_1	0.75	0.25	2	27	sf_lib	26.2e-3	28.77e-3
CDynamicLoad2_27_ss_1	0.75	0.25	2	27	ss_lib	28.14e-3	30.92e-3
CDynamicLoad2_27_tt_1	0.75	0.25	2	27	tt_lib	25.76e-3	28.41e-3
CDynamicLoad2_60_ff_1	0.75	0.25	2	60	ff_lib	23.55e-3	26.11e-3
CDynamicLoad2_60_fs_1	0.75	0.25	2	60	fs_lib	25.28e-3	28.17e-3
CDynamicLoad2_60_sf_1	0.75	0.25	2	60	sf_lib	25.89e-3	28.52e-3
CDynamicLoad2_60_ss_1	0.75	0.25	2	60	ss_lib	27.7e-3	30.51e-3
CDynamicLoad2_60_tt_1	0.75	0.25	2	60	tt_lib	25.33e-3	28.04e-3

Table 5: Calculated results for load transients

4.6 Line Regulation

The line regulation characterizes the regulators ability to keep the specified output voltage constant while the input varies. The line regulation is defined as[11]:

$$\text{Line Regulation} = \frac{\Delta V_{out}}{\Delta V_{in}}$$

The following equation is used for the test bench:

$$\frac{\Delta V_{Out}}{\Delta V_{in}} = \frac{V_{out}(2\,\text{A}) - V_{out}(1.05\,\text{A})}{0.95\,\text{V}}$$

The output voltage variance is determined between the maximum voltage value at a supply current of 2 A and the regulator input voltage at 1.05 A, after all devices are in the saturated region[11]. Ideally, the output voltage is not dependent from the input voltage and therefore the line regulation is small. It must be considered, whether the line regulation is calculated with reference to the chip ground or the PCB ground. Due to the voltage drop across the wire bonds (resistance approx. 6 mΩ), the correct line regulation of the regulator has to be calculated referring to the chip ground. Therefore an adjustment to the above-noted formula is made:

$$LineReg_{ChipGND} = V_{out}(2\,\text{A}) - Chip_{GND}(2\,\text{A}) - V_{out}(1.05\,\text{A}) - Chip_{GND}(1.05\,\text{A})$$

Figure 4.18 illustrates the voltage drop across the wire bonds.

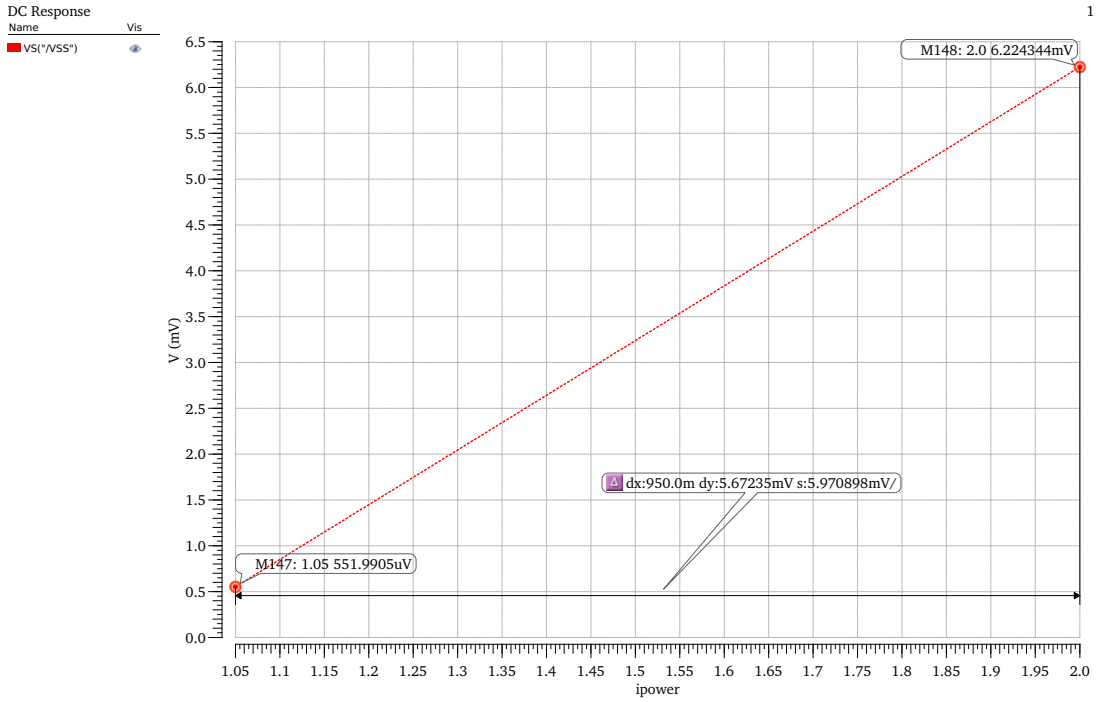

Figure 4.18: Voltage drop across the wire bonds between chip and PCB-ground

A DC sweep analysis is operated with following parameters:

- rload: 1.2 GΩ, 240 Ω, 12 Ω, 1.2 Ω
- Temperatures: −40 °C, −20 °C, 27 °C, 60 °C
- Process variations: ff, ss, fs, sf, tt

Table 6 covers the results for line regulation both to chip and PCB-ground. For both cases all results are significantly below the specified limit of 10 mV. In addition to the table, all results are plotted in figure 4.19 to 4.20. It can be recognized that there are virtually no changes to the output voltage for an increasing input current. The general variance of about 47 mV is caused by the temperature drift of V_{out}, described in section 4.3.

Corner	**rload**	**Temp**	**Process**	**LineReg_PCB**	**LineReg_Chip**
CLineReg_-40_fs_0	1.2G	-40	fs_lib	5.662e-3	-37.96e-6
CLineReg_-40_fs_1	240	-40	fs_lib	5.662e-3	-38.15e-6
CLineReg_-40_fs_2	12	-40	fs_lib	5.655e-3	-41.79e-6
CLineReg_-40_fs_3	1.2	-40	fs_lib	5.557e-3	-115.8e-6
CLineReg_-40_sf_0	1.2G	-40	sf_lib	5.907e-3	207.2e-6
CLineReg_-40_sf_1	240	-40	sf_lib	5.907e-3	207.2e-6
CLineReg_-40_sf_2	12	-40	sf_lib	5.903e-3	206.1e-6
CLineReg_-40_ss_0	1.2G	-40	ss_lib	5.915e-3	215.4e-6
CLineReg_-40_ss_1	240	-40	ss_lib	5.915e-3	215.4e-6

Corner	rload	Temp	Process	LineReg_PCB	LineReg_Chip
CLineReg_-40_ss_2	12	-40	ss_lib	5.911e-3	214.1e-6
CLineReg_-40_ss_3	1.2	-40	ss_lib	5.868e-3	197.4e-6
CLineReg_-40_tt_0	1.2G	-40	tt_lib	5.893e-3	192.9e-6
CLineReg_-40_tt_1	240	-40	tt_lib	5.893e-3	192.8e-6
CLineReg_-40_tt_2	12	-40	tt_lib	5.889e-3	191.8e-6
CLineReg_-40_tt_3	1.2	-40	tt_lib	5.85e-3	178.8e-6
CLineReg_-20_fs_0	1.2G	-20	fs_lib	5.431e-3	-269.2e-6
CLineReg_-20_fs_1	240	-20	fs_lib	5.43e-3	-269.4e-6
CLineReg_-20_fs_2	12	-20	fs_lib	5.424e-3	-273.6e-6
CLineReg_-20_fs_3	1.2	-20	fs_lib	5.321e-3	-352.1e-6
CLineReg_-20_sf_0	1.2G	-20	sf_lib	5.801e-3	101.1e-6
CLineReg_-20_sf_1	240	-20	sf_lib	5.801e-3	101e-6
CLineReg_-20_sf_2	12	-20	sf_lib	5.797e-3	99.65e-6
CLineReg_-20_ss_0	1.2G	-20	ss_lib	5.839e-3	138.8e-6
CLineReg_-20_ss_1	240	-20	ss_lib	5.839e-3	138.8e-6
CLineReg_-20_ss_2	12	-20	ss_lib	5.834e-3	137.1e-6
CLineReg_-20_ss_3	1.2	-20	ss_lib	5.785e-3	114.2e-6
CLineReg_-20_tt_0	1.2G	-20	tt_lib	5.76e-3	59.57e-6
CLineReg_-20_tt_1	240	-20	tt_lib	5.759e-3	59.49e-6
CLineReg_-20_tt_2	12	-20	tt_lib	5.755e-3	58.03e-6
CLineReg_-20_tt_3	1.2	-20	tt_lib	5.709e-3	36.93e-6
CLineReg_27_fs_0	1.2G	27	fs_lib	3.705e-3	-1.995e-3
CLineReg_27_fs_1	240	27	fs_lib	3.704e-3	-1.995e-3
CLineReg_27_fs_2	12	27	fs_lib	3.694e-3	-2.004e-3
CLineReg_27_fs_3	1.2	27	fs_lib	3.511e-3	-2.172e-3
CLineReg_27_sf_0	1.2G	27	sf_lib	5.006e-3	-694e-6
CLineReg_27_sf_1	240	27	sf_lib	5.006e-3	-694.2e-6
CLineReg_27_sf_2	12	27	sf_lib	4.999e-3	-698.2e-6
CLineReg_27_sf_3	1.2	27	sf_lib	4.911e-3	-764.9e-6
CLineReg_27_ss_0	1.2G	27	ss_lib	5.187e-3	-512.7e-6
CLineReg_27_ss_1	240	27	ss_lib	5.187e-3	-512.9e-6
CLineReg_27_ss_2	12	27	ss_lib	5.181e-3	-516.6e-6
CLineReg_27_ss_3	1.2	27	ss_lib	5.097e-3	-577.3e-6
CLineReg_27_tt_0	1.2G	27	tt_lib	4.604e-3	-1.096e-3
CLineReg_27_tt_1	240	27	tt_lib	4.603e-3	-1.097e-3
CLineReg_27_tt_2	12	27	tt_lib	4.596e-3	-1.101e-3
CLineReg_27_tt_3	1.2	27	tt_lib	4.495e-3	-1.182e-3
CLineReg_60_ff_1	240	60	ff_lib	1.496e-3	-4.204e-3

Corner	rload	Temp	Process	LineReg_PCB	LineReg_Chip
CLineReg_60_ff_2	12	60	ff_lib	1.481e-3	-4.218e-3
CLineReg_60_fs_0	1.2G	60	fs_lib	983.2e-6	-4.717e-3
CLineReg_60_fs_1	240	60	fs_lib	982.4e-6	-4.718e-3
CLineReg_60_fs_2	12	60	fs_lib	966.9e-6	-4.733e-3
CLineReg_60_fs_3	1.2	60	fs_lib	654.2e-6	-5.043e-3
CLineReg_60_sf_0	1.2G	60	sf_lib	4.373e-3	-1.327e-3
CLineReg_60_sf_1	240	60	sf_lib	4.373e-3	-1.327e-3
CLineReg_60_sf_2	12	60	sf_lib	4.362e-3	-1.336e-3
CLineReg_60_sf_3	1.2	60	sf_lib	4.182e-3	-1.497e-3
CLineReg_60_ss_0	1.2G	60	ss_lib	3.995e-3	-1.705e-3
CLineReg_60_ss_1	240	60	ss_lib	3.994e-3	-1.705e-3
CLineReg_60_ss_2	12	60	ss_lib	3.986e-3	-1.712e-3
CLineReg_60_ss_3	1.2	60	ss_lib	3.845e-3	-1.836e-3
CLineReg_60_tt_0	1.2G	60	tt_lib	2.875e-3	-2.825e-3
CLineReg_60_tt_1	240	60	tt_lib	2.875e-3	-2.825e-3
CLineReg_60_tt_2	12	60	tt_lib	2.864e-3	-2.834e-3
CLineReg_60_tt_3	1.2	60	tt_lib	2.666e-3	-3.021e-3

Table 6: Line Regulation results with reference to PCB- and Chip-ground

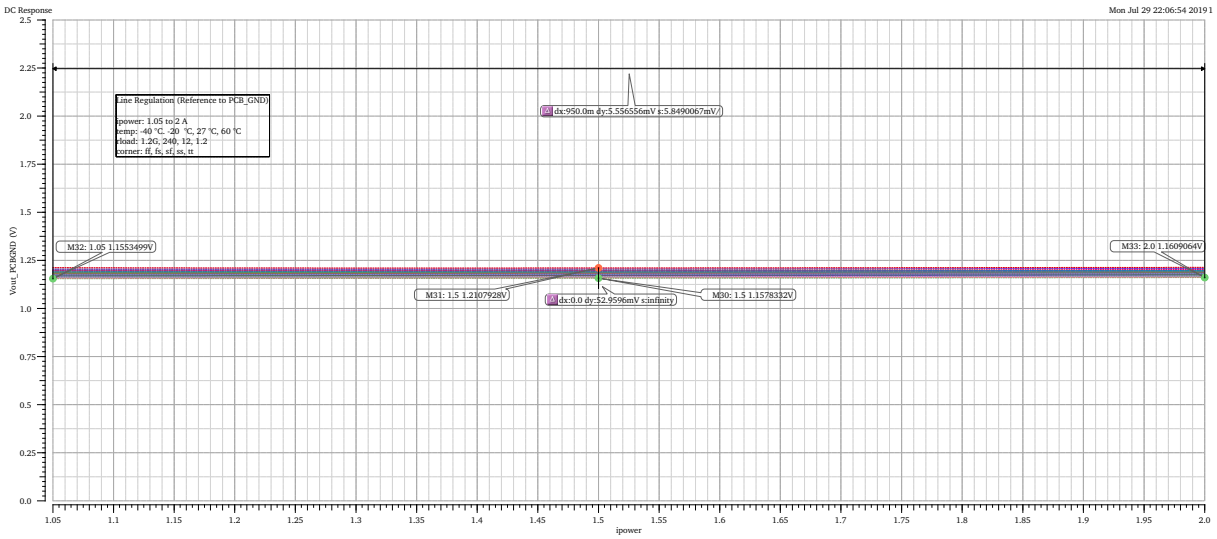

Figure 4.19: Line Regulation (Reference PCB-ground) for all corners and temperatures

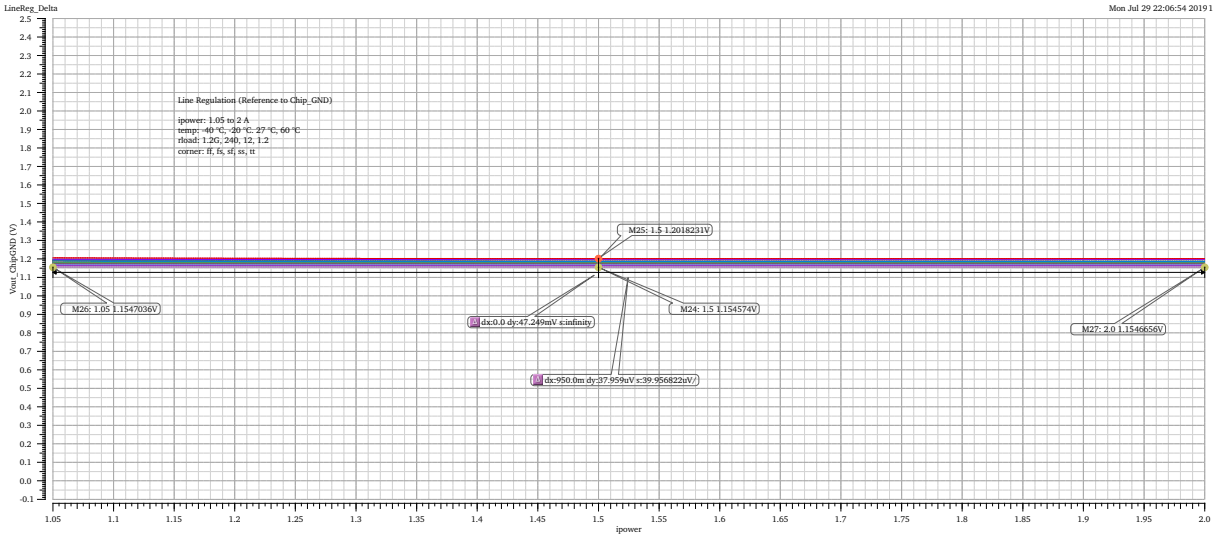

Figure 4.20: Line Regulation (Reference Chip-ground) for all corners and temperatures

4.7 Load Regulation

Load regulation characterizes the ability of a power supply to keep a constant output voltage at changing load currents. Ideally the output voltage should be independent of the load and the value of the load regulation is zero.

$$\text{Load Regulation} = \frac{V_{minLoad} - V_{maxLoad}}{\Delta I_{Load}} \tag{4.3}$$

With a DC analysis and a sweep of the load current from 0 A to 1 A the load regulation of the regulator is investigated and is calculated with the following formula[11]:

$$\text{Load Regulation} = \text{VS("/Vout") 1) - value(VS("/Vout") 0))} \tag{4.4}$$

Below are the parameters which are set:

- iload from 0 A to 1 A
- ipower: 1.05 A, 2 A
- Temperatures: $-40\,°\text{C}$, $-20\,°\text{C}$, $27\,°\text{C}$, $60\,°\text{C}$
- Process variations: ff, ss, fs, sf, tt

All results are below 10 mV and within the specification. The highest load regulation is 420.8 µV (1.05 A, 60 °C, ff) while the best value is 12.74 µV (2 A, −40 °C, ss). Table 7 is listing the complete results.

Corner	ipower	Temp	Process	LoadReg
CLoadReg_-40_ff_0	1.05	-40	ff_lib	41.51e-6
CLoadReg_-20_ff_0	1.05	-20	ff_lib	64.35e-6
CLoadReg_27_ff_0	1.05	27	ff_lib	202.5e-6
CLoadReg_60_ff_0	1.05	60	ff_lib	420.8e-6
CLoadReg_-40_fs_0	1.05	-40	fs_lib	112.9e-6
CLoadReg_-20_fs_0	1.05	-20	fs_lib	118e-6
CLoadReg_27_fs_0	1.05	27	fs_lib	228.3e-6
CLoadReg_60_fs_0	1.05	60	fs_lib	393.6e-6
CLoadReg_-20_sf_0	1.05	-20	sf_lib	35e-6
CLoadReg_27_sf_0	1.05	27	sf_lib	94.51e-6
CLoadReg_-40_ss_0	1.05	-40	ss_lib	32.09e-6
CLoadReg_-20_ss_0	1.05	-20	ss_lib	40.13e-6
CLoadReg_27_ss_0	1.05	27	ss_lib	86.45e-6
CLoadReg_-40_tt_0	1.05	-40	tt_lib	29.74e-6
CLoadReg_-20_tt_0	1.05	-20	tt_lib	41.13e-6
CLoadReg_27_tt_0	1.05	27	tt_lib	116.6e-6
CLoadReg_-40_fs_1	2	-40	fs_lib	17.23e-6
CLoadReg_-20_fs_1	2	-20	fs_lib	18.13e-6
CLoadReg_27_fs_1	2	27	fs_lib	22.23e-6
CLoadReg_60_fs_1	2	60	fs_lib	27.19e-6
CLoadReg_-40_sf_1	2	-40	sf_lib	13.67e-6
CLoadReg_-20_sf_1	2	-20	sf_lib	14.81e-6
CLoadReg_27_sf_1	2	27	sf_lib	17.33e-6
CLoadReg_60_sf_1	2	60	sf_lib	14.19e-6
CLoadReg_-40_ss_1	2	-40	ss_lib	12.74e-6
CLoadReg_-20_ss_1	2	-20	ss_lib	13.2e-6
CLoadReg_27_ss_1	2	27	ss_lib	15.49e-6
CLoadReg_60_ss_1	2	60	ss_lib	17.92e-6
CLoadReg_-40_tt_1	2	-40	tt_lib	14.94e-6
CLoadReg_-20_tt_1	2	-20	tt_lib	16.28e-6
CLoadReg_27_tt_1	2	27	tt_lib	20.38e-6
CLoadReg_60_tt_1	2	60	tt_lib	24.97e-6

Table 7: Load Regulation results for ipower = 1.05 A and 2 A for all conditions

In addition to the table, again all results are plotted in figures 4.21 to 4.22.

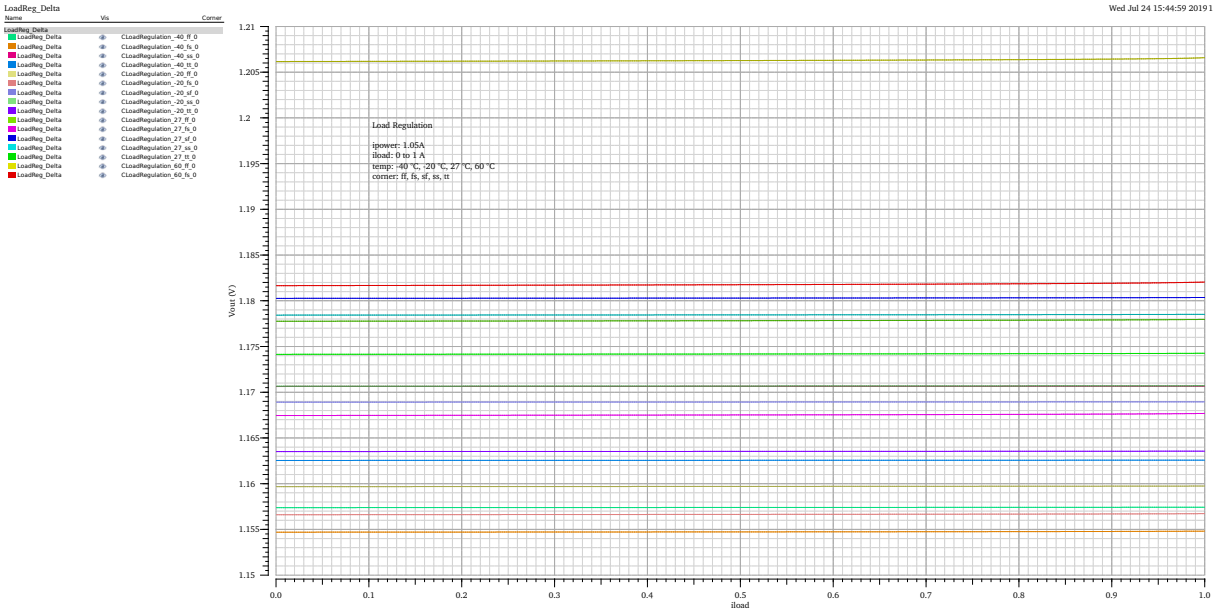

Figure 4.21: Load Regulation for ipower = 1.05 A

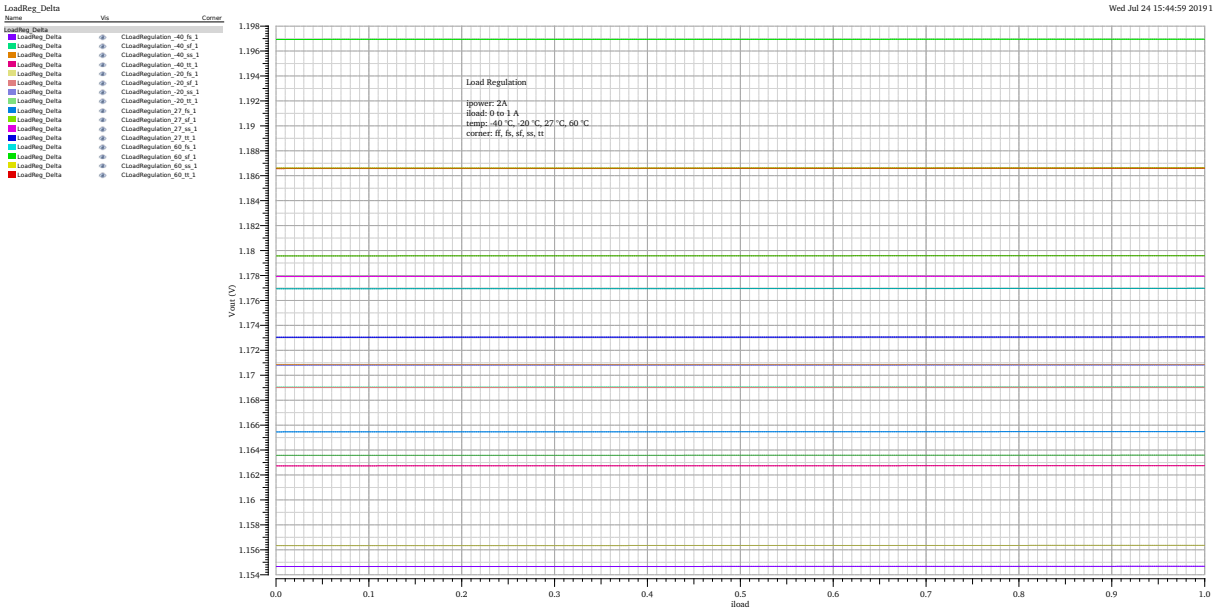

Figure 4.22: Load Regulation for ipower = 2 A

4.8 Start-Up Simulation

The Start-Up simulation checks the reaction of the input and output voltage during the ramp-up phase of the input current. The input current is increased from 0 A to 1.1 A and from 0 A to 2 A as a separate condition. Different rise times of 100 ns, 1 ms and 100 ms are applied and

the signals of V_{in} and V_{out} are plotted. The voltages ideally should rise without oscillations and peaks to their stabilized referenced values. The simulation is operated with the following parameters:

- itpower: 0 A to 1.1 A and from 0 A to 2 A
- rload: 1.2 GΩ, 240 Ω, 12 Ω, 1.2 Ω
- trise: 100 ns, 1 ms, 100 ms
- Temperatures: −40 °C, −20 °C, 27 °C, 60 °C
- Process variations: ff, ss, fs, sf, tt

The figures 4.23 to 4.26 illustrate the simulation results of V_{in} and V_{out} for an input current of up to 1.1 A and a rise time of 100 ns. Apart from a peak of about 2.12 V, no oscillations are observable. The temperature drift (see. 4.3) causes a general variance for V_{in} of about 33 mV, and about 54 mV for V_{out} respectively. Oscillation issues can be observed in figures 4.31 to 4.34 for a rise time of 100 ms, both for the input and the output voltage and for all input currents. Some corners are oscillating from 5 ms to 45 ms and then reaches a stable state. In general, all occurring oscillations are temporary and the voltages are settling down at their specified values for all tested conditions. So while this might not be completely optimal, a proper operability of the start-up circuit should be ensured.

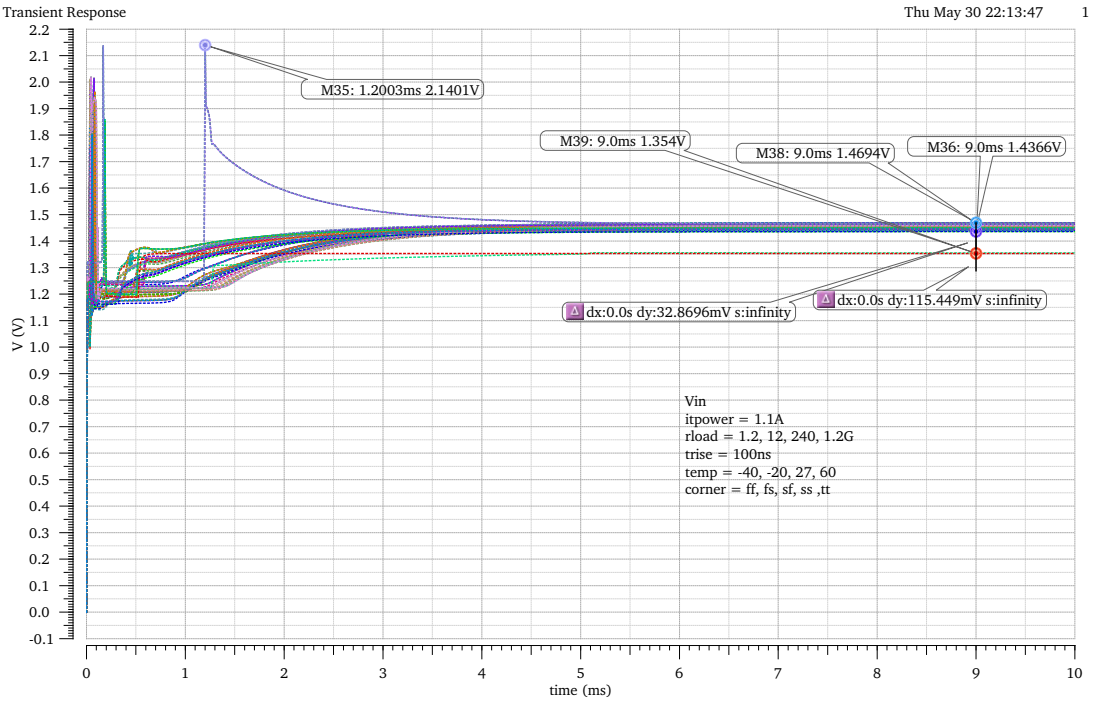

Figure 4.23: Vin start-up behavior with trise = 100 ns and itpower = 1.1 A

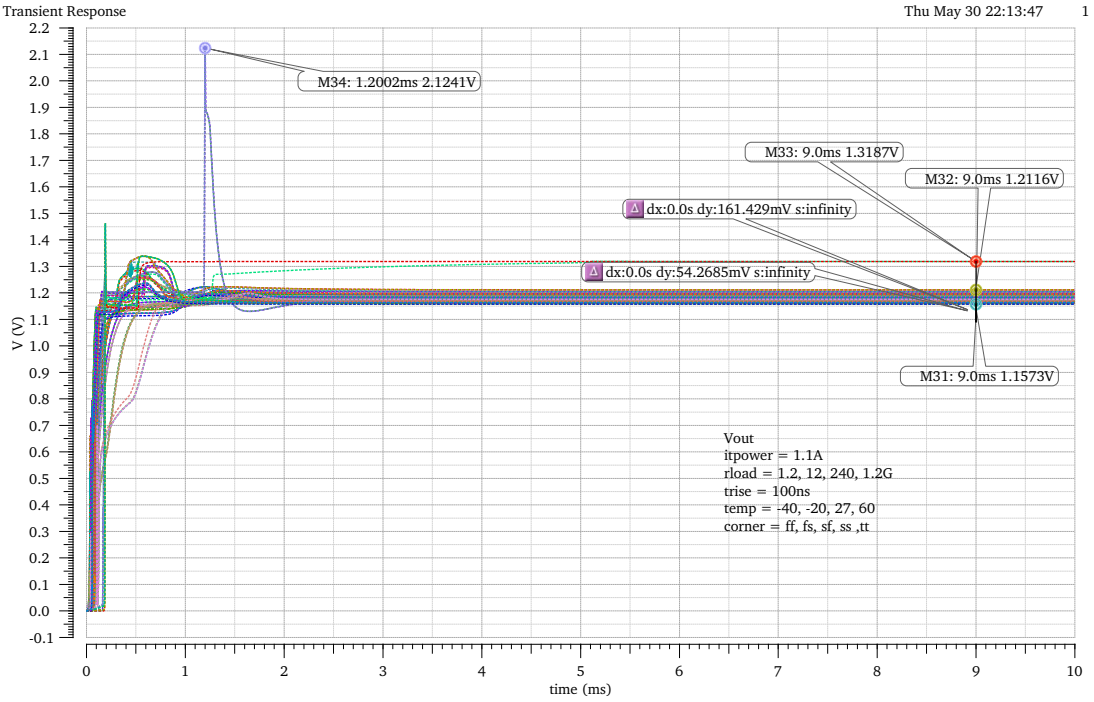

Figure 4.24: Vout start-up behavior with trise = 100 ns and itpower = 1.1 A

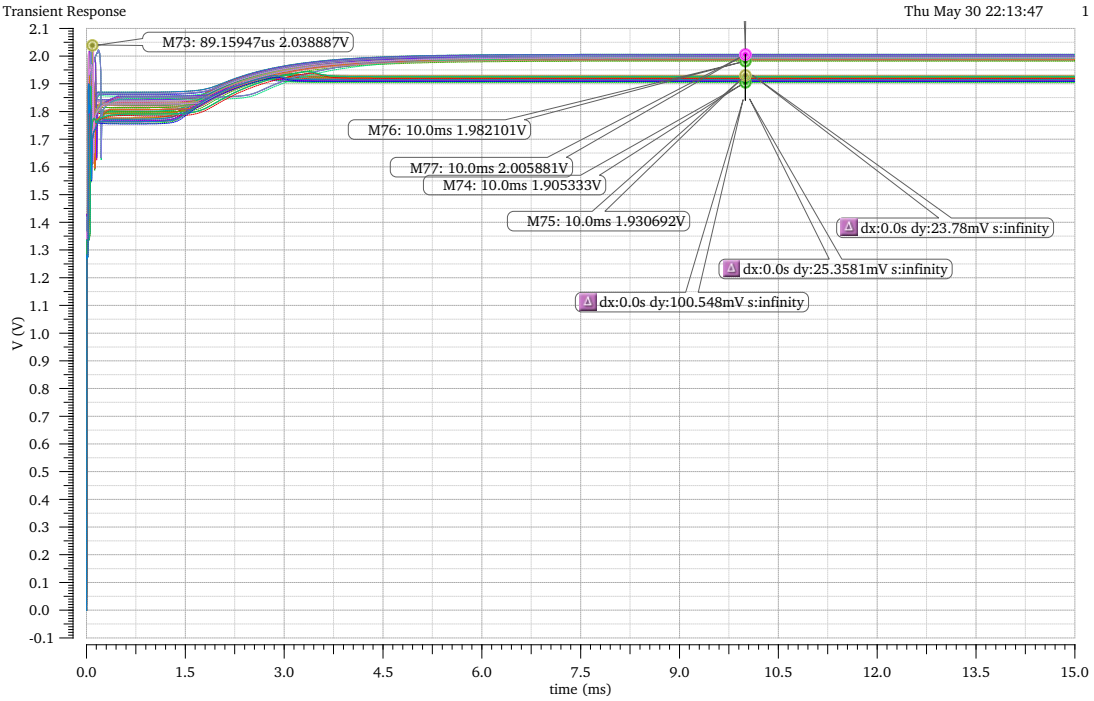

Figure 4.25: Vin start-up behavior with trise = 100 ns and itpower = 2 A

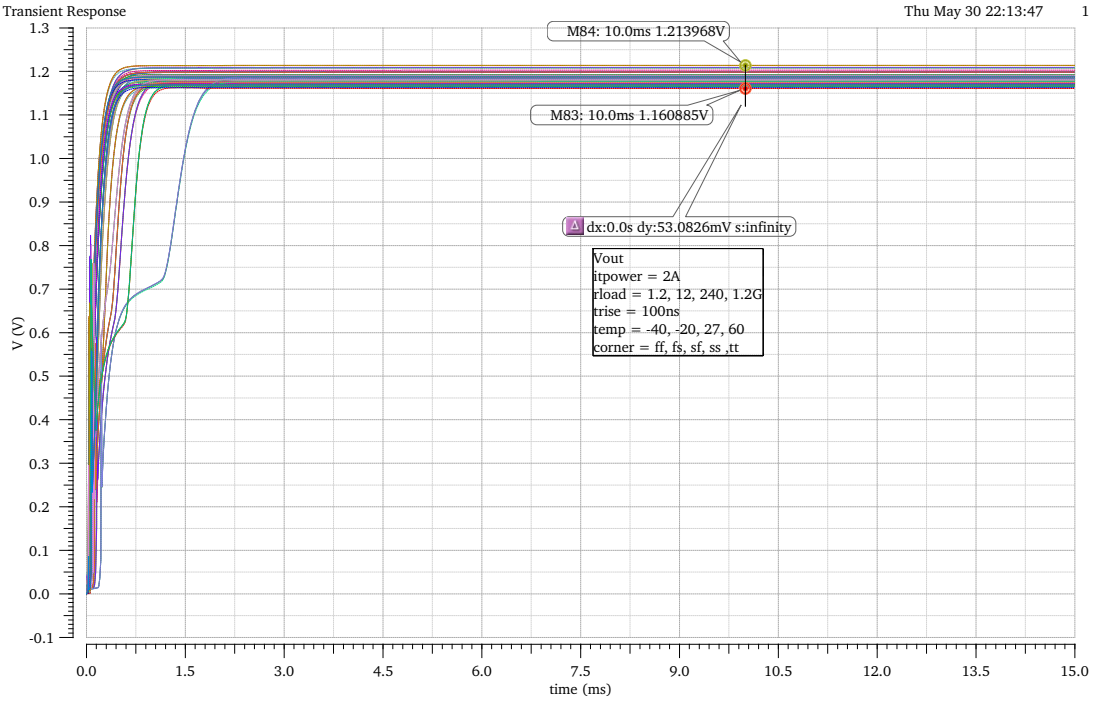

Figure 4.26: Vout start-up behavior with trise = 100 ns and itpower = 2 A

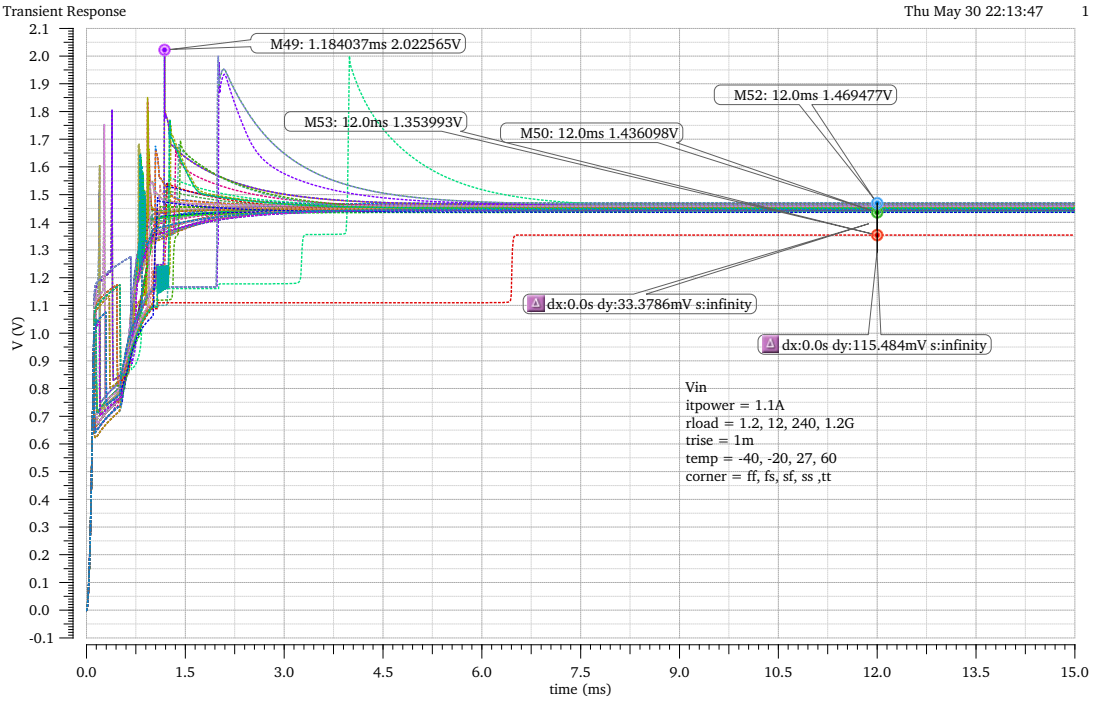

Figure 4.27: Vin start-up behavior with trise = 1 ms and itpower = 1.1 A

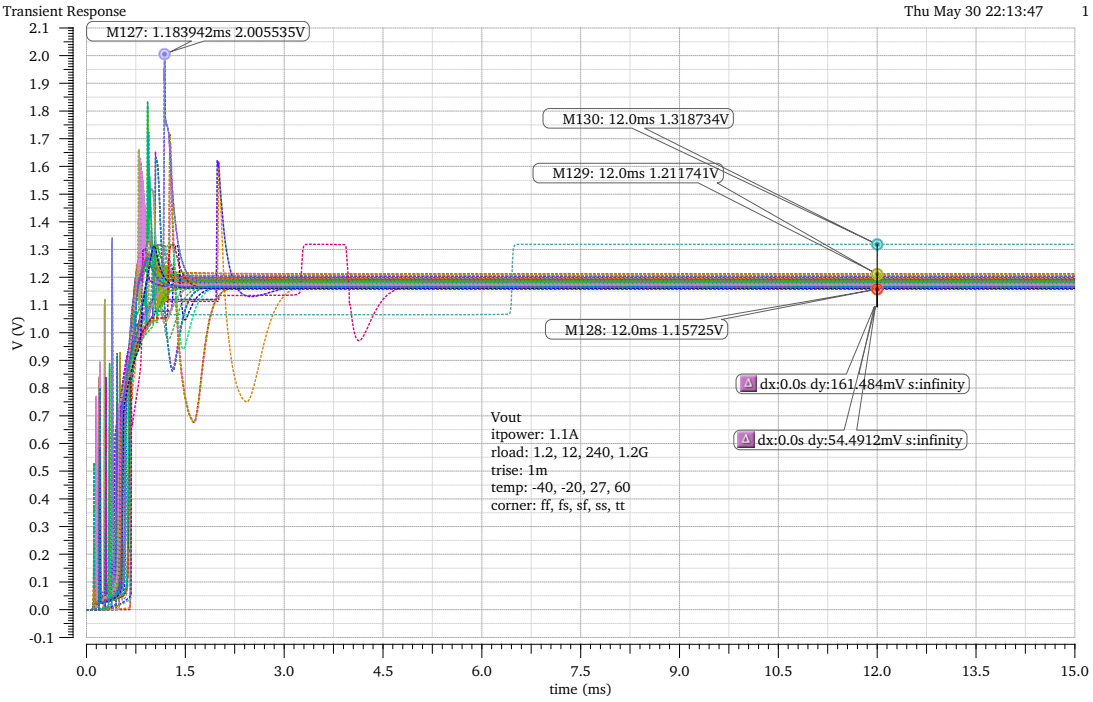

Figure 4.28: Vout start-up behavior with trise = 1 ms and itpower = 1.1 A

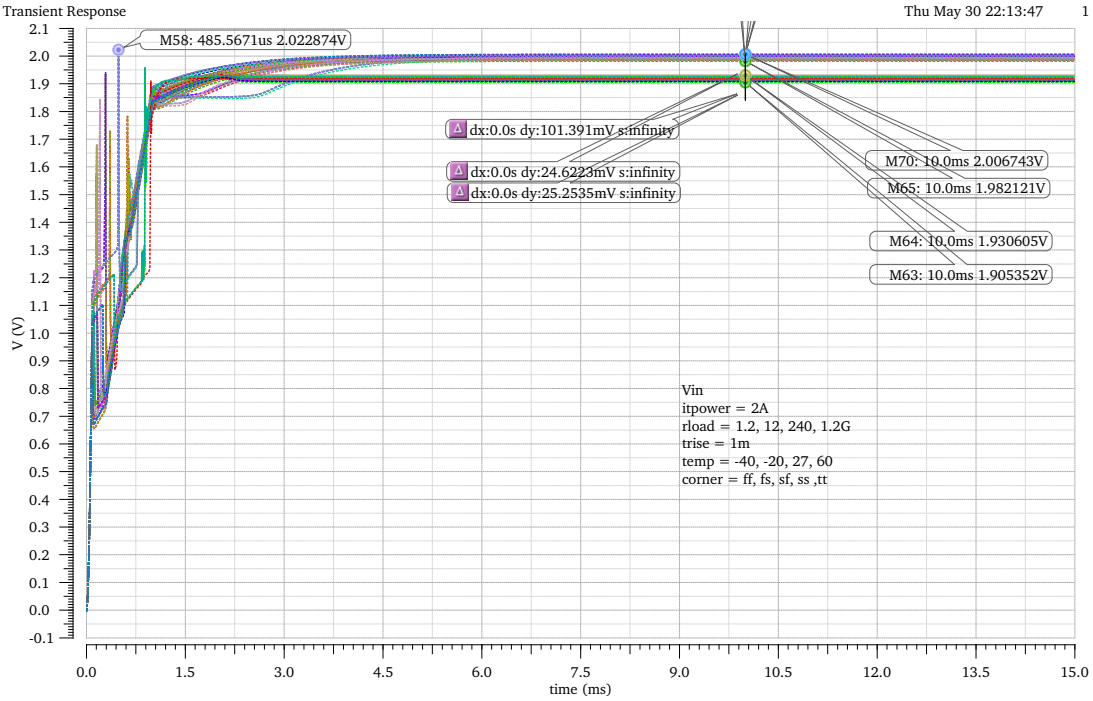

Figure 4.29: Vin start-up behavior with trise = 1 ms and itpower = 2 A

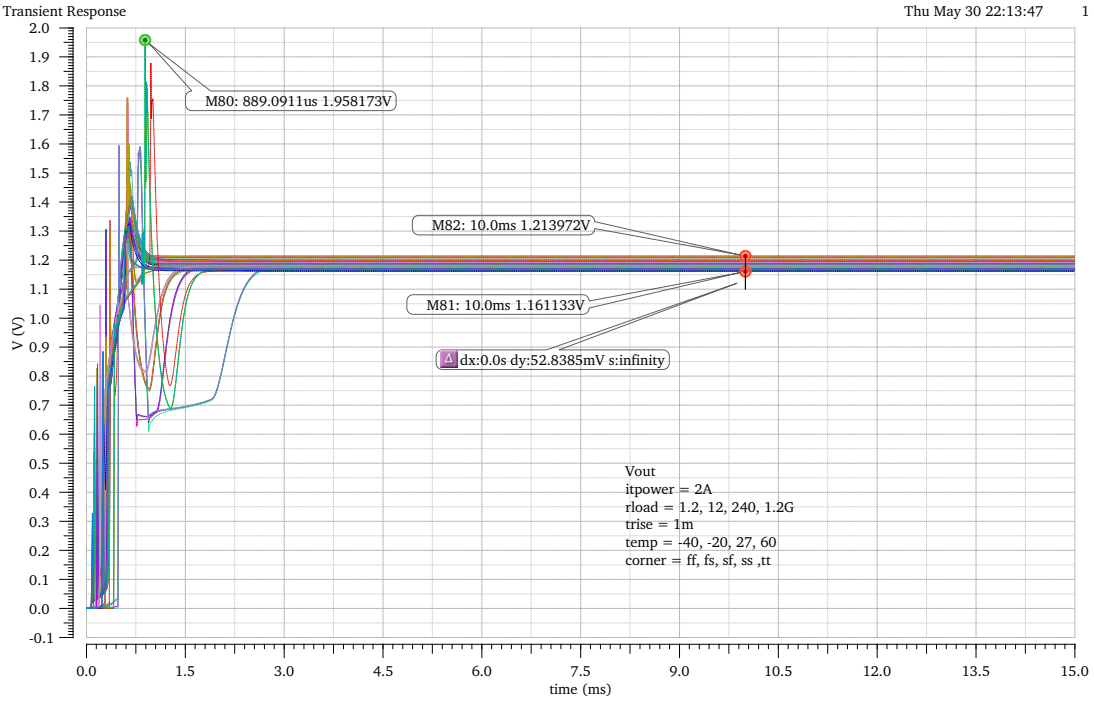

Figure 4.30: Vout start-up behavior with trise = 1 ms and itpower = 2 A

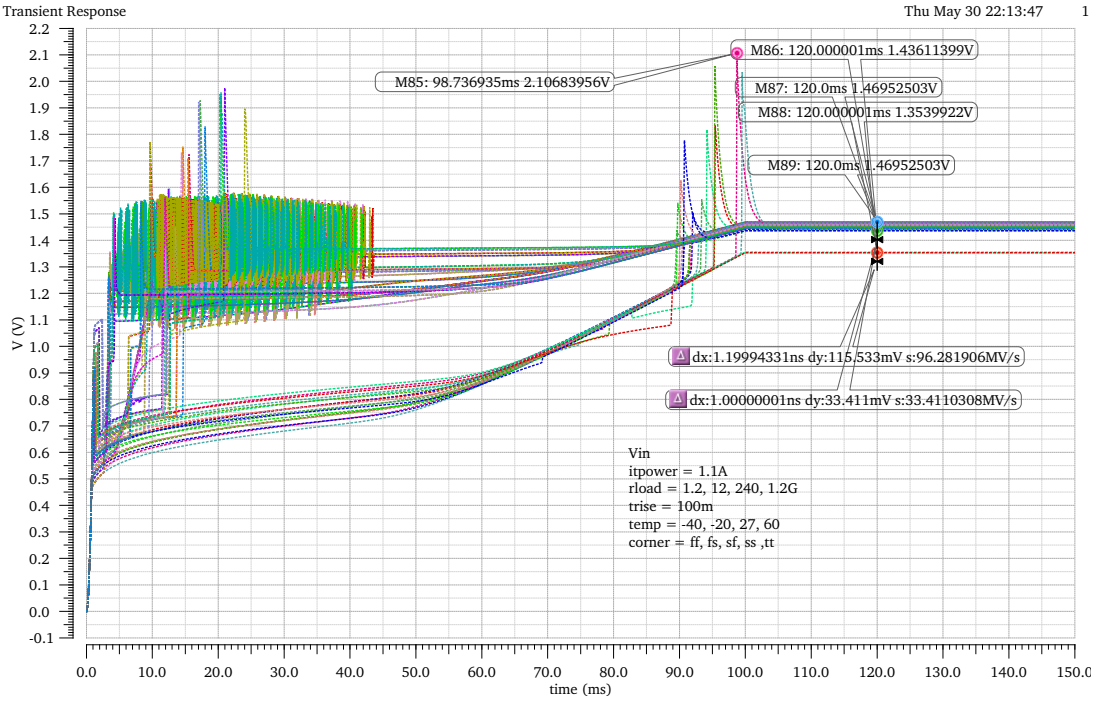

Figure 4.31: Vin start-up behavior with trise = 100 ms and itpower = 1.1 A

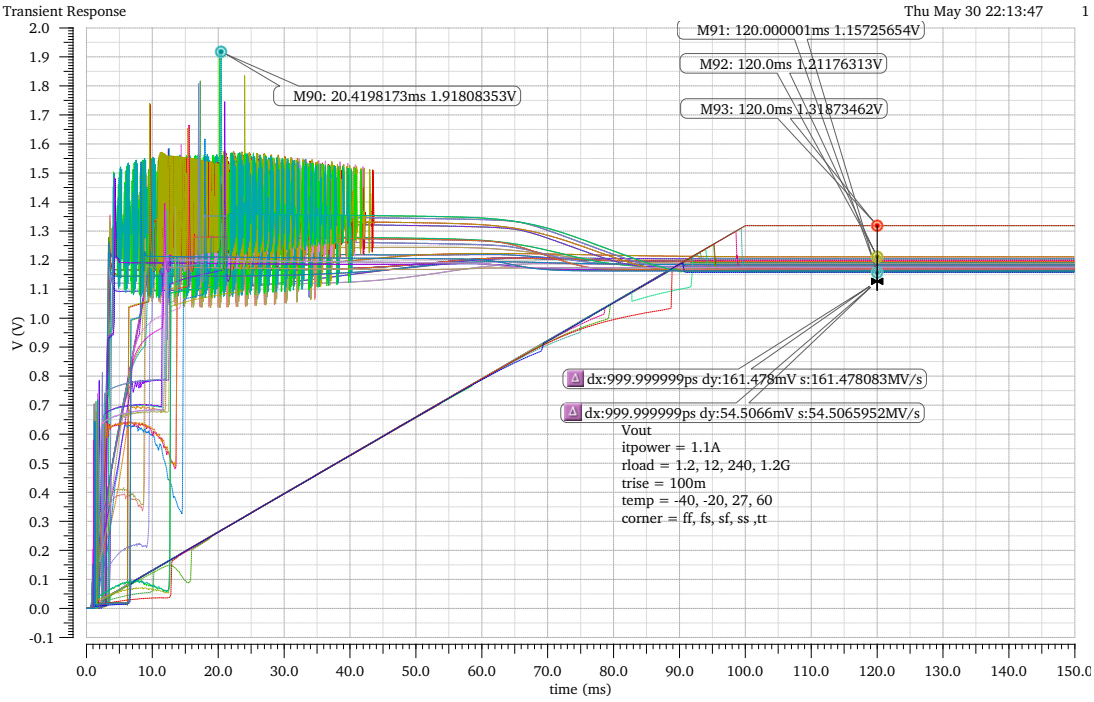

Figure 4.32: Vout start-up behavior with trise = 100 ms and itpower = 1.1 A

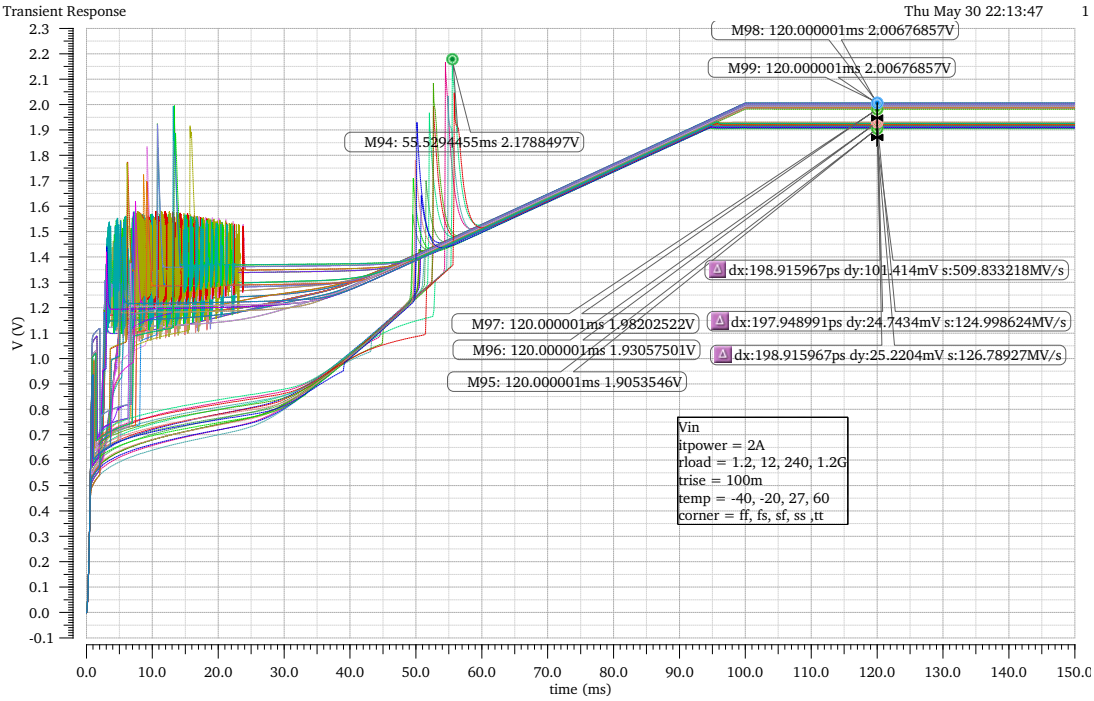

Figure 4.33: Vin start-up behavior with trise = 100 ms and itpower = 2 A

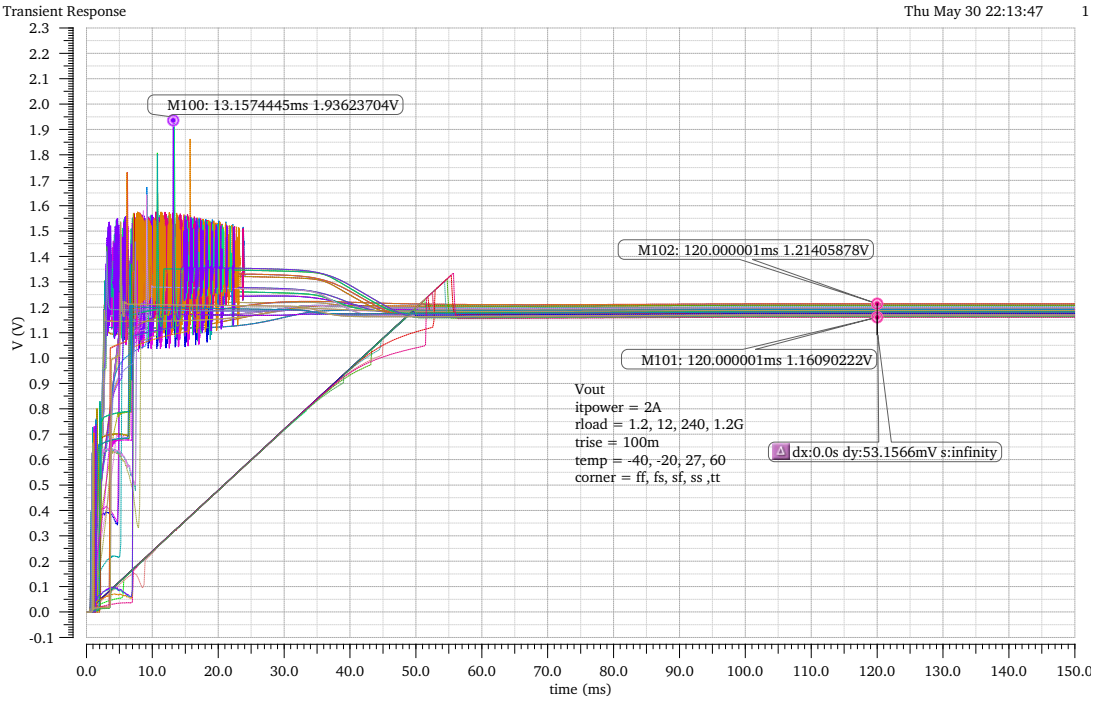

Figure 4.34: Vout start-up behavior with trise = 100 ms and itpower = 2 A

4.9 Rext Sweep

The reference current of the SLDO is defined by a resistor Rext shown in 3.1. The internal resistor used on previous iterations of the RD53-chip will not be part of the final iteration and therefore a switching option between these resistors is no longer provided in test chip C. Resistors which are implemented directly on the chip suffers from a high temperature variation and are not sufficient for the generation of the reference current. With the use of external components, small tolerance ranges and low temperature dependency can be achieved. By varying the external resistor the reference current changes, which affects the regulators input impedance and hence the slope of the input voltage. The intersection of V_{in} with the y-axis marks the offset voltage. The simulation presented in this section determines the influence of different slopes on the offset voltage. Ideally, the offset would stay the same at varying slopes or reference resistor values respectively. Figure 4.35 shows the slopes for different Rext values under optimal conditions.

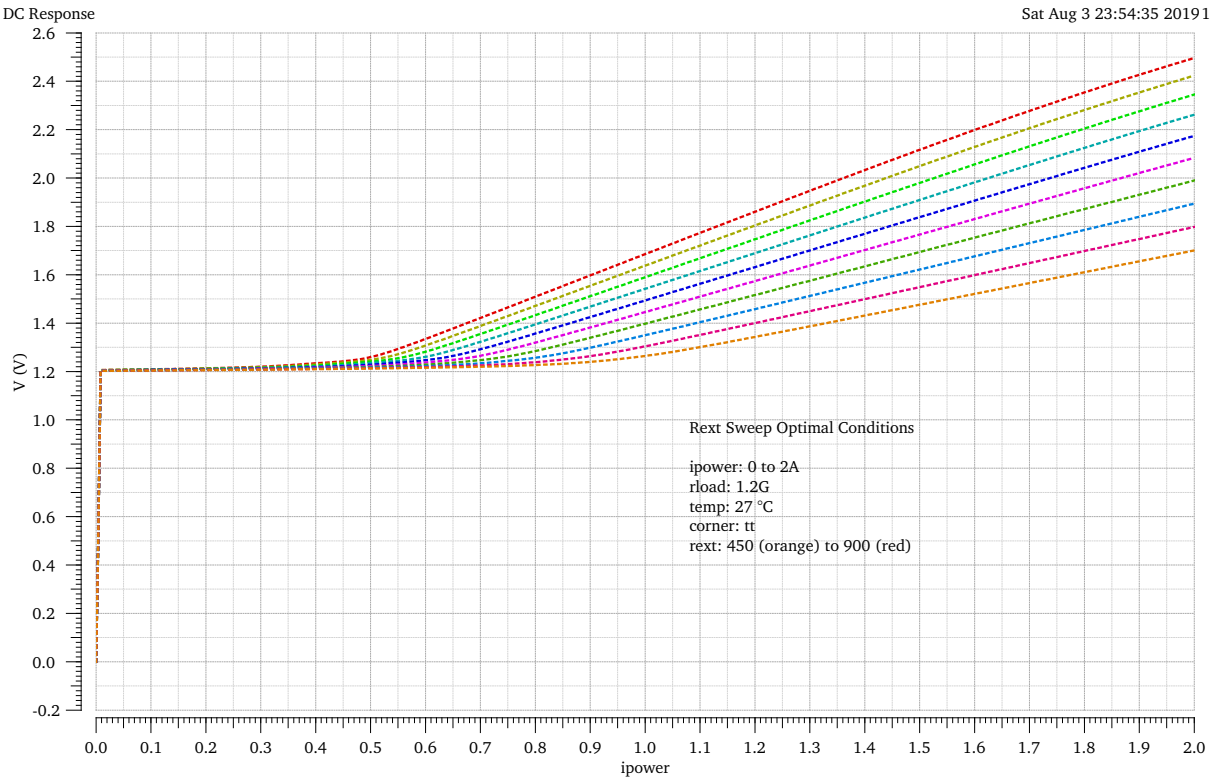

Figure 4.35: Rext sweep for optimal conditions

The plot shows the input current sweep from 0 A to 2 A with resistance values between 450 Ω and 900 Ω in steps of 50 Ω simulated for 27 °C, tt process corner and a load of 1.2 GΩ. The offset voltage can be taken from the y-axis interception of the separate slopes and matches with the specified value of about 800 mV. This behavior would be desirable for all simulated conditions. The slope of V_{in} is calculated as follows[11]:

$$\text{Rslope\_average} = \text{average(deriv (clip (VS("/Vin") 1.2 2)))}$$

The function clip selects the value range of the input current between 1.2 A and 2 A and calculates the slope by using the deriv-function. The average value is determined from the selected range and stored in the variable Rslope. The offset is determined with the following equation[11].

$$\text{Vofs} = \text{value(VS("/Vin") 1.2)} - (\text{Rslope\_average} \cdot 1.2)$$

The output voltage is approximated as a linear function, in the form of:

$$y = m \cdot x + V_{ofs}$$

and the offset is determined from the y-axis intercept. The equation can be solved according to V_{ofs} with the slope m (Rslope_average) and two points $x1$ (1.2 A) and $y1$ (value(VS("/Vin") 1.2)) on the function[11]. The simulation is performed with the following parameters:

- ipower: 0 A to 2 A
- Rext: variation from 450 Ω to 900 Ω in steps of 50 Ω
- rload: 1.2 GΩ, 240 Ω, 12 Ω, 1.2 Ω
- Temperatures: −40 °C, −20 °C, 27 °C, 60 °C
- Process variations: ff, ss, fs, sf, tt

The tables 8 to 11 are showing the minimum, the maximum and the average slopes for each resistance value and the calculated offset voltage. Furthermore, the changes of the slopes and the offset for increasing resistance values are plotted. Ideally, the offset voltage remains at a constant value of 800 mV. The slope depends linearly on the external resistor. The calculated offset voltage varies in the range of 782.7 mV to 978.9 mV.

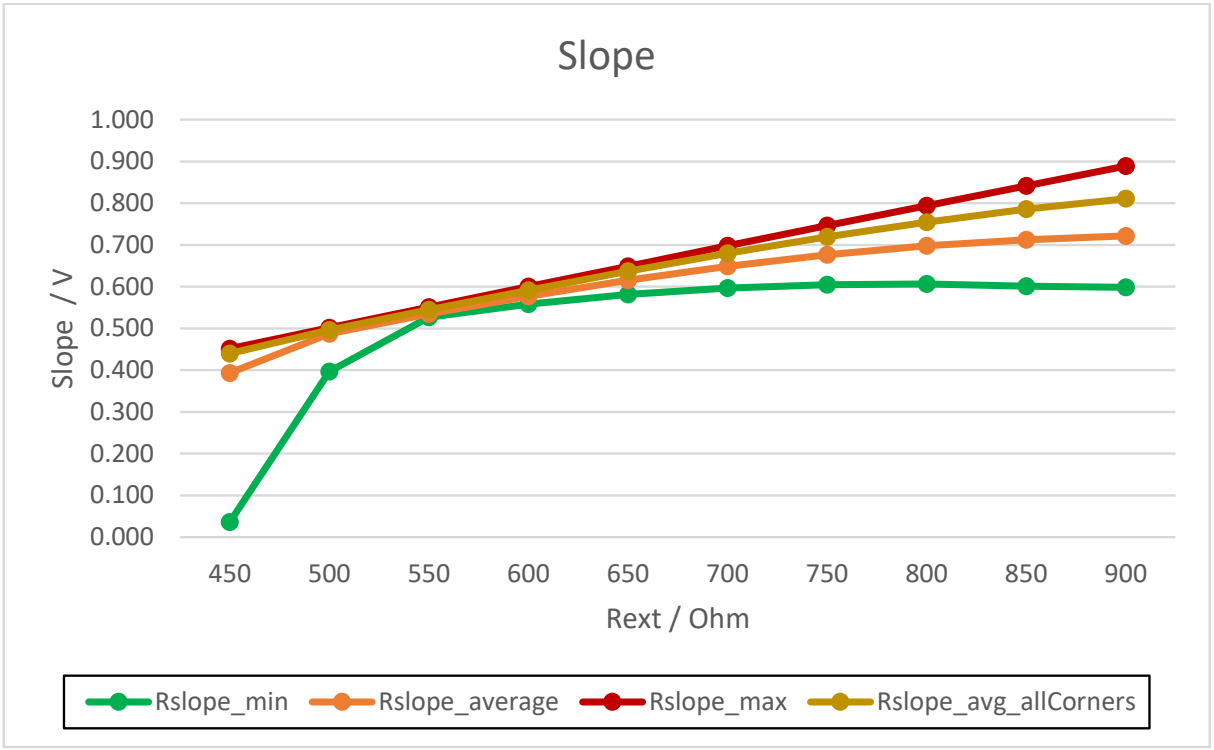

Figure 4.36: Minimum, average and maximum slopes for different Rext

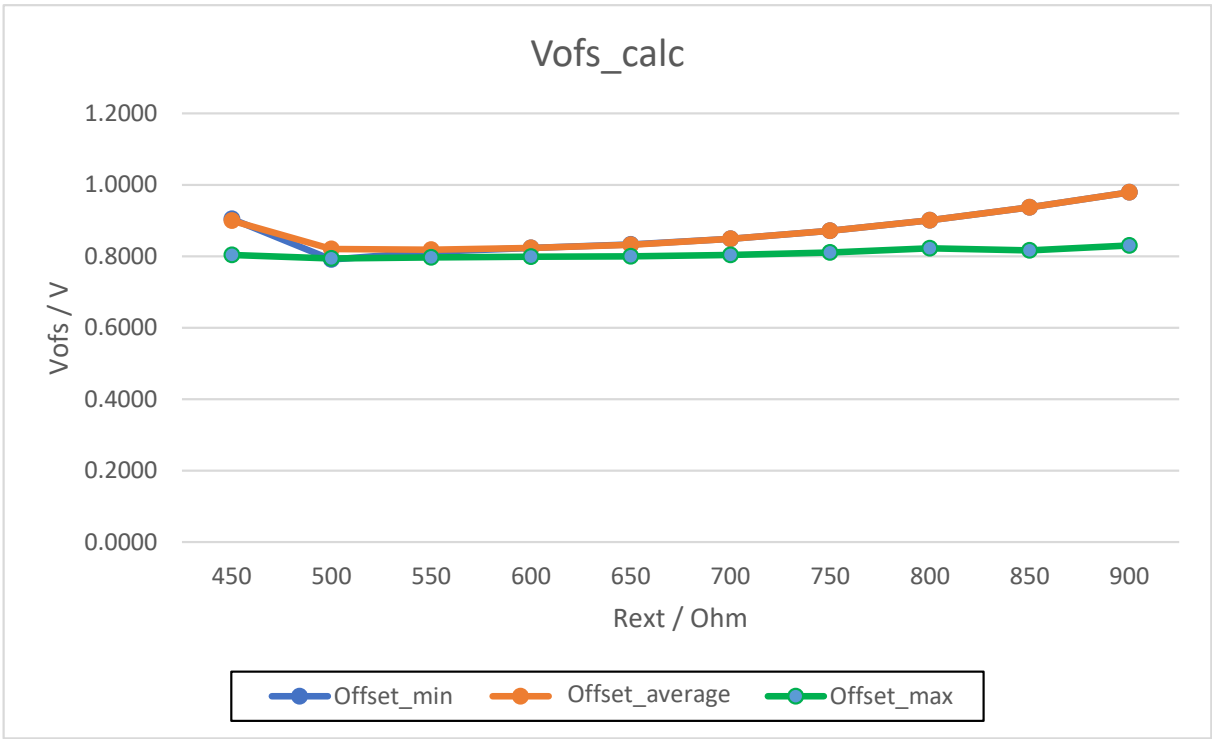

Figure 4.37: Calculated V_{ofs} for different Rext

The variance of the calculated offset voltage is the consequence of the unsteady slopes. In Table 8 the minimum values of the slopes for every Rext is shown. Although it is expected that the slope is constant over the whole sweep range, it is perceptible that for 450 Ω and 500 Ω the minimal slope values 36.5 mV and 395.2 mV are distinctly lower than expected. Figure 4.38 shows this behavior.

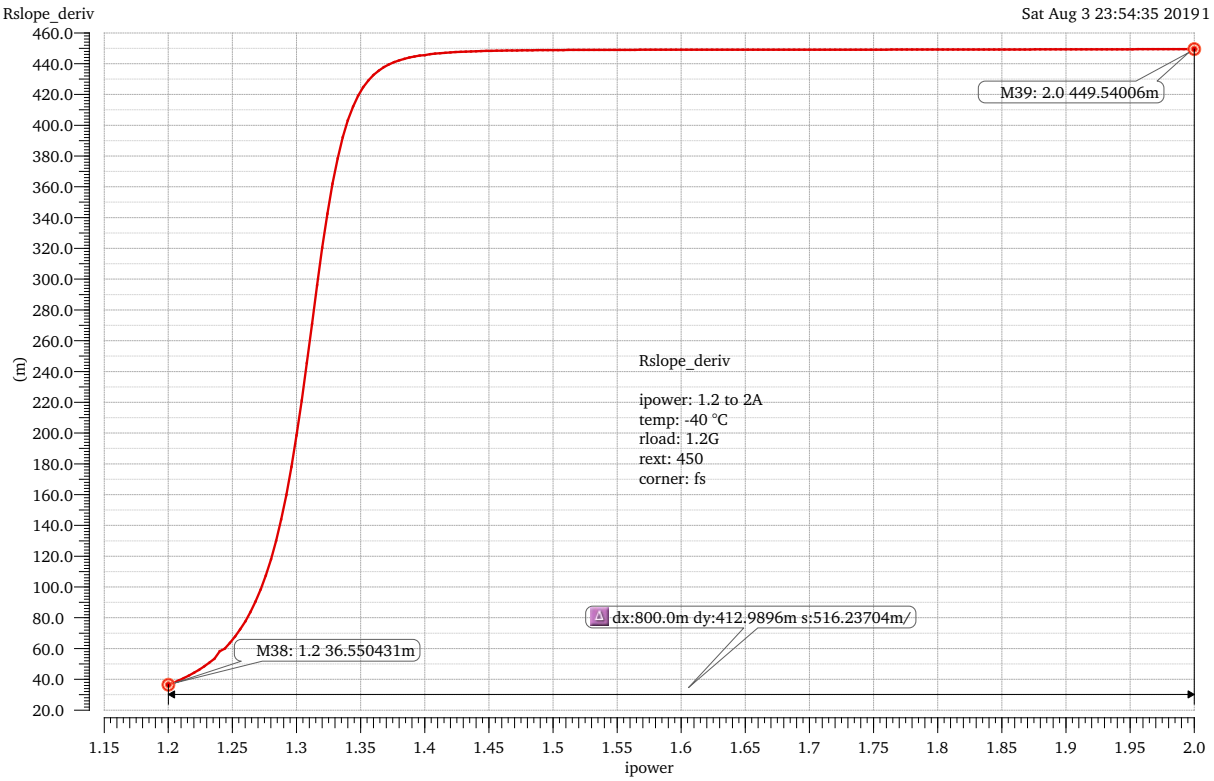

Figure 4.38: Plot of the slope for Rext = 450 Ω, −40 °C, no load and fs-corner

It can be seen that the slope has a ramp-up phase beginning at 1.2 V with an exponential rise until 1.4 V, where all devices are saturated and the slope settles at around the expected 449.5 mV and remains constant up to 2 A. It has to be considered that this has an influence on the average slope calculation. For corners with slope ramp-ups likewise Plot 4.38, the average slope will be lower than expected. This leads to an imprecise calculation of the offset voltage in some cases. Table 9 contains the lowest average slopes. To verify the overall dependency of the offset voltage from the slope and resistor variations, the V_{ofs} signal for all conditions is plotted in figure 4.39

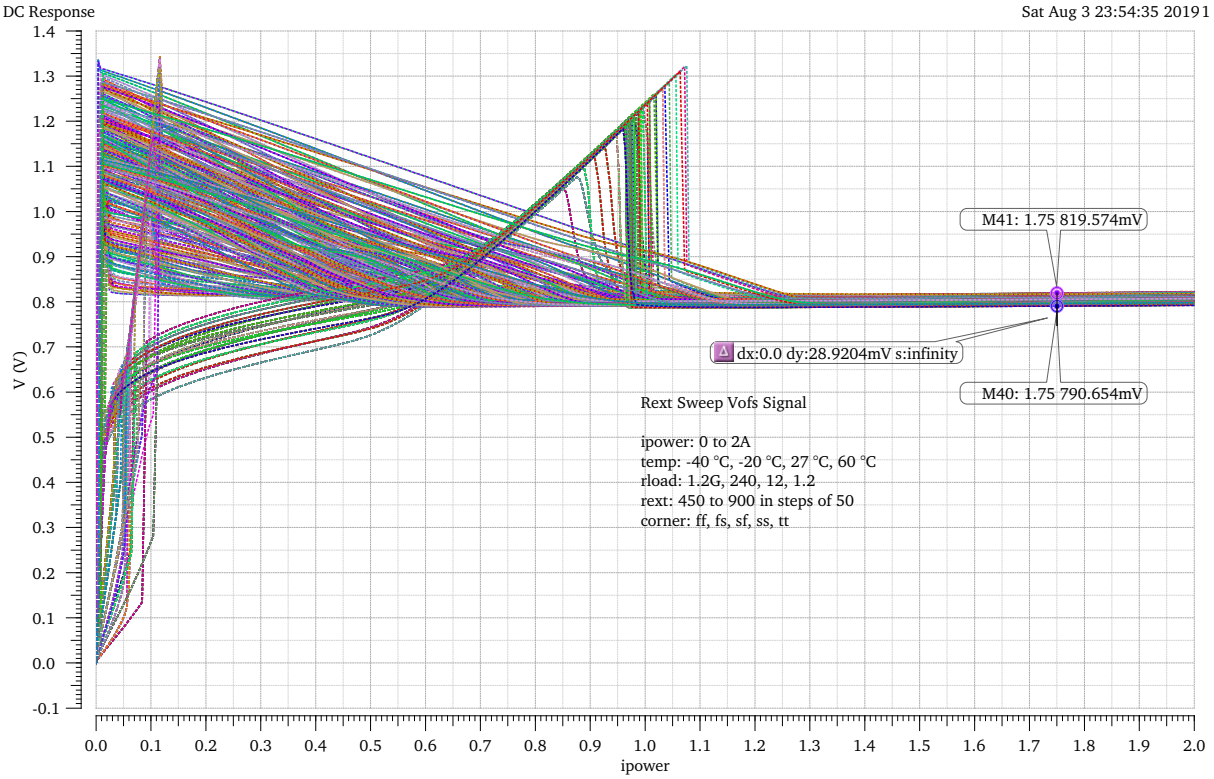

Figure 4.39: Signal of V_{ofs} for all conditions

The values for the offset voltage varies from 790.65 mV (Rext 450 Ω, −20 °C, rload 1.2 GΩ, ff) to 819.57 mV (Rext 900 Ω, 60 °C, rload 1.2 GΩ, sf). This is a variation 28.92 mV and a sufficient result. When taking the general temperature drift of all chip voltages into account (see. 4.3), the offset voltage can be considered as virtually independent from changes in slope and resistance value.

Rext	**Rslope_min**	**Offset(Rslope_min)**	**Corner**
450	36.5e-3	904.5e-3	-40 °C, 1.2G, fs
500	396.2e-3	790.9e-3	-40 °C, 1.2, fs
550	526.5e-3	812.4e-3	60 °C, 12, ff
600	558.3e-3	823.5e-3	60 °C, 1.2G, ff
650	581.0e-3	833.3e-3	60 °C, 1.2G, ff
700	596.5e-3	849.2e-3	60 °C, 1.2G, ff
750	605.1e-3	871.6e-3	60 °C, 1.2G, ff
800	606.4e-3	900.7e-3	60 °C, 1.2G, ff
850	600.7e-3	936.6e-3	60 °C, 1.2G, ff
900	598.7e-3	978.9e-3	60 °C, 1.2G, ff

Table 8: Minimal slopes and calculated offset voltage for different Rext

Rext	Rslope_average	Offset(Rslope_average)	Corner
450	393.4e-3	900.0e-3	-40 °C, 1.2, fs
500	487.5e-3	820.0e-3	60 °C, 1.2G, ff
550	534.3e-3	818.4e-3	60 °C, 12, ff
600	577.2e-3	823.5e-3	60 °C, 1.2G, ff
650	615.7e-3	832.2e-3	60 °C, 12, ff
700	648.8e-3	849.2e-3	60 °C, 1.2G, ff
750	676.2e-3	871.6e-3	60 °C, 1.2G, ff
800	697.5e-3	900.7e-3	60 °C, 1.2G, ff
850	712.6e-3	936.6e-3	60 °C, 1.2G, ff
900	721.6e-3	978.9e-3	60 °C, 1.2G, ff

Table 9: Lowest average slopes and calculated offset voltage for different Rext

Rext	Rslope_max	Offset(Rslope_max)	Corner
450	451.5e-3	803.3e-3	27°C, 1.2, ss
500	501.4e-3	793.8e-3	-40 °C, 1.2, sf
550	550.8e-3	797.3e-3	-20 °C, 1.2, ss
600	599.9e-3	798.7e-3	27 °C, 1.2, ss
650	649.0e-3	800.2e-3	27 °C, 1.2, ss
700	697.6e-3	803.5e-3	27 °C, 1.2, ss
750	745.9e-3	810.2e-3	27 °C, 1.2, ss
800	793.8e-3	822.1e-3	27 °C, 1.2, ss
850	841.2e-3	816.4e-3	-20 °C, 1.2, ss
900	888.8e-3	830.3e-3	-20 °C, 1.2, ss

Table 10: Maximum slopes and calculated offset voltage for different Rext

Rext	Rslope_all
450	440e-3
500	496.3e-3
550	544.7e-3
600	591.6e-3
650	636.8e-3
700	679.6e-3
750	719.1e-3
800	754.7e-3
850	785.4e-3
900	810.5e-3

Table 11: Average slopes across all corners and calculated offset voltage for different Rext

4.10 Overvoltage Protection

As was described in section 3.3 the OVP-circuit should protect the regulator from peaks of the input voltage above 2 V. To test the functionality a plot from the Rext Sweep simulation (4.9) with enabled OVP is displayed for all corners, temperatures and loads and different external resistance values.

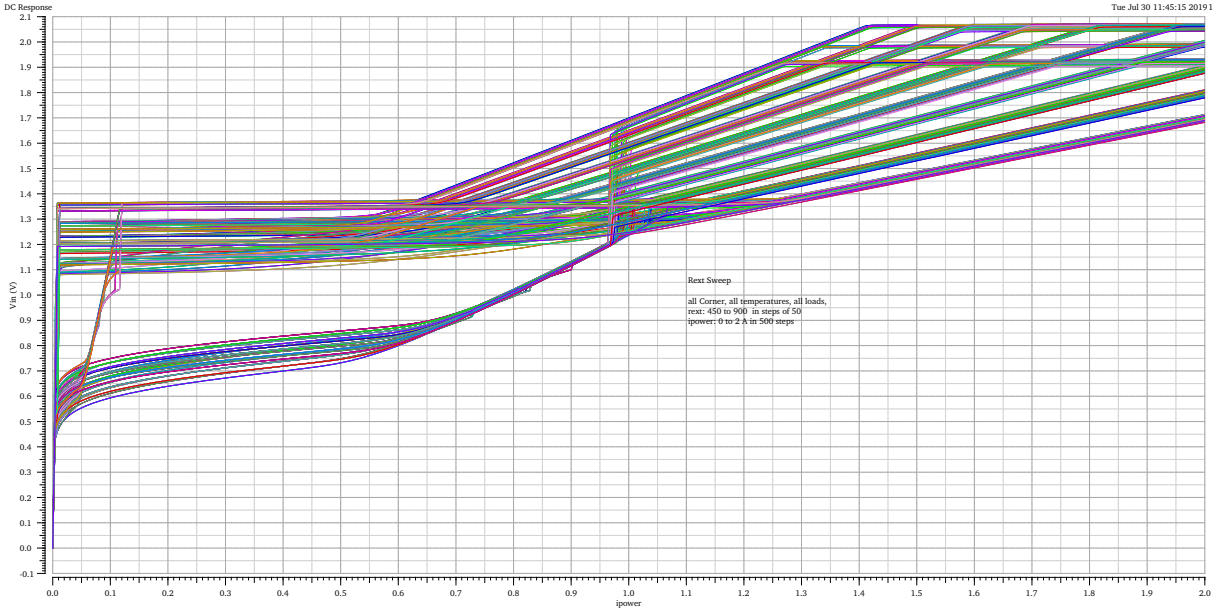

Figure 4.40: Sweep of ipower from 0 A to 2 A and V_{in} for different Rext with enabled OVP

It can be observed that the input voltage levels saturate at around 1.9 V to 2.05 V, which proves the effectiveness of the overvoltage protection. Due to the overall temperature- and corner dependency, the threshold voltage varies slightly below and above the desired 2 V.

4.11 Power Cycles

The Power Cycle simulation is based on the ISO 16750-2:2010 Standard[10] and examines the reset behaviour in the case of an input signal drop. A load profile with an input current of 2 A and different rise times was generated and implemented with an ipwlf-source. The load profiles correspond to the scheme shown in the figure 41[11].

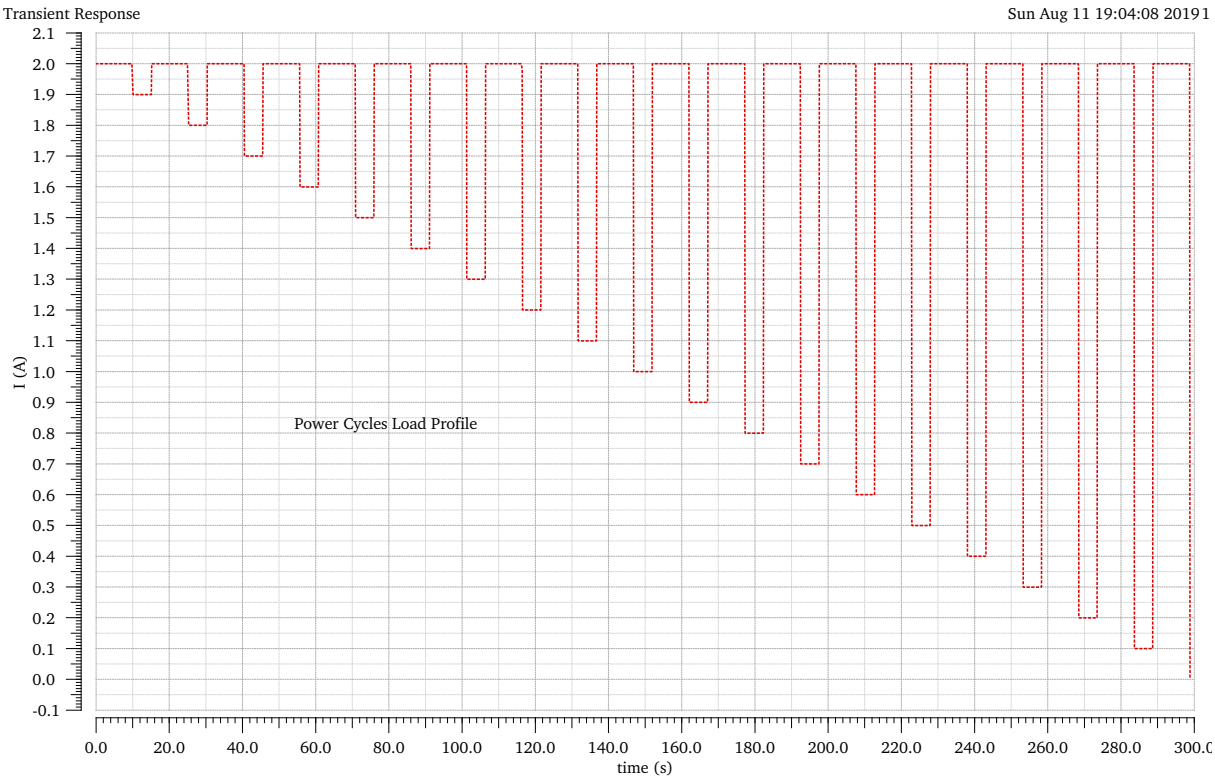

Figure 4.41: Load Profile with ipwlf-source according to ISO 16750-2:2010

First, the supply current is reduced by 5% to $0.95 \cdot IinMax$ and held for 5 s. After that the maximum value is increased again and kept for 10 s. Then it is decreased by another 5% until a value of 0 A is reached. A transient simulation is executed with the following parameters.

- Input current: 2 A to 0 A
- rload: 1.2 GΩ, 240 Ω, 12 Ω, 1.2 Ω
- Temperatures: −40 °C, −20 °C, 27 °C, 60 °C
- Process variations: ff, ss, fs, sf, tt

The results in general are satisfying, as there are no persistent oscillations in any signal. Voltage peaks are occurring occasionally, especially for ss- and fs-corners. When the input current is below 1 A, the voltages V_{in}, V_{out} and V_{ofs} follow the shape of the load profile current for corners with rload = 1.2 Ω. This is an effect of a too large load current for the correlating input current of $\leq$ 1 A. For input current drops close to 0 A temporary oscillation can be observed, resulting in the shutdown of the regulator when 0 A is reached.

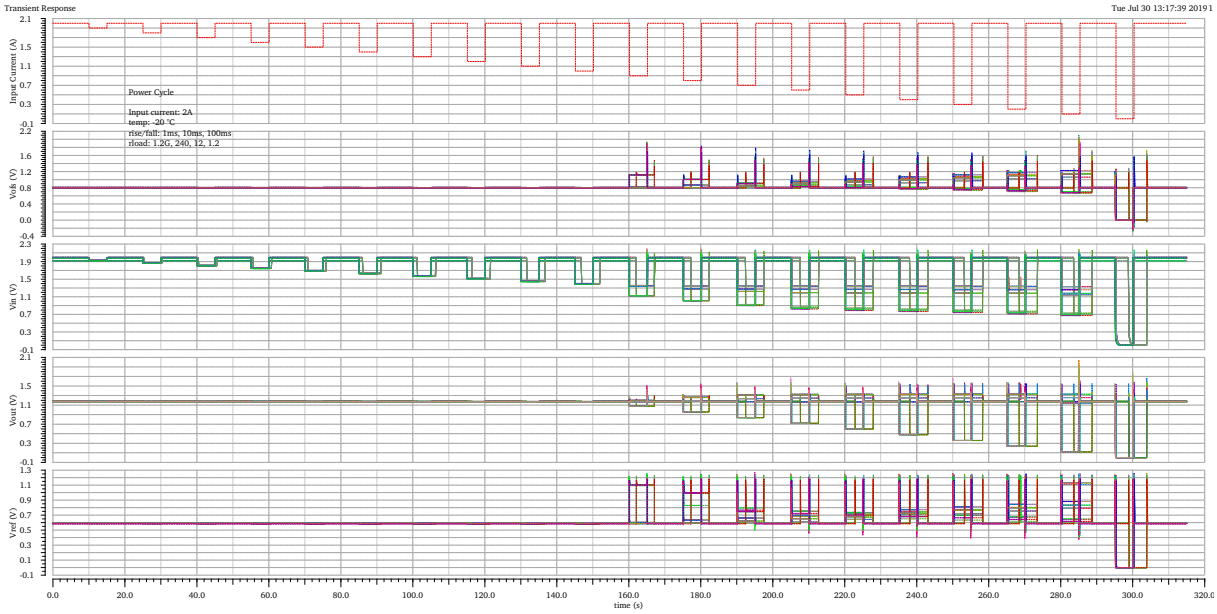

Figure 4.42: Power Cycles for −20 °C

trise[ms]	**Vin[V]**	**Vout[V]**	**Vref[V]**	**Vofs[V]**
1	2.2 (ss_11)	2.04 (ss_10)	1.27 (fs_11)	2.1 (ss_10)
10	2.17 (ss_7)	1.61 (ss_6)	1.26 (ss_7)	1.93 (fs_6)
100	2.16 (ss_3)	1.67 (fs_2)	1.24 (fs_1)	1.73 (fs_2)

Table 12: Peak values for Power Cycles at −20 °C and all process corners

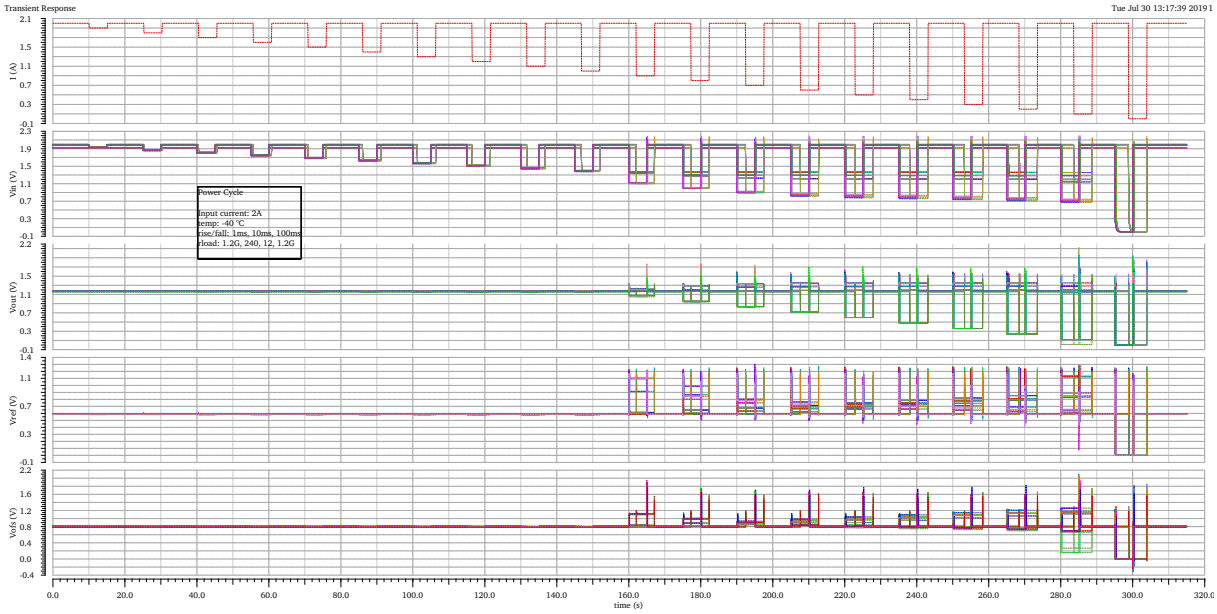

Figure 4.43: Power Cycles for −40 °C

trise[ms]	**Vin[V]**	**Vout[V]**	**Vref[V]**	**Vofs[V]**
1	2.2 (ss_10)	2.12 (ss_10)	1.29 (ss_10)	2.1 (ss_10)
10	2.2 (ss_7)	1.68 (ss_6)	1.15 (ss_7)	1.95 (fs_6)
100	2.18 (ss_3)	1.86 (fs_2)	1.26 (ss_2)	1.86 (fs_2)

Table 13: Peak values for Power Cycles at −40 °C and all process corners

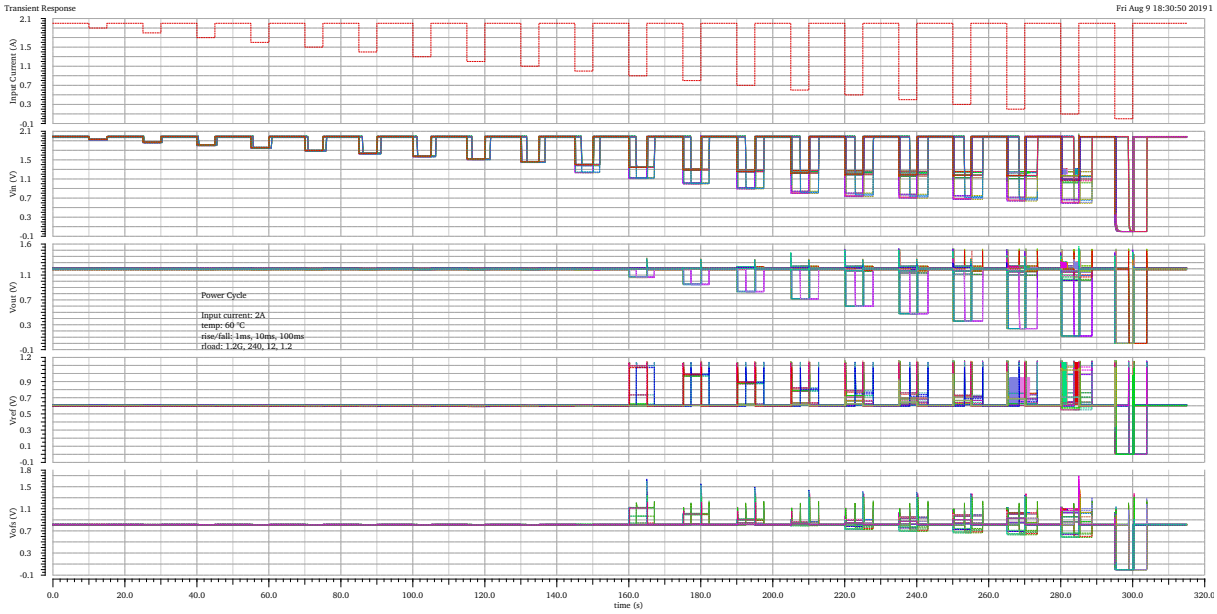

Figure 4.44: Power Cycles for 60 °C

trise[ms]	Vin[V]	Vout[V]	Vref[V]	Vofs[V]
1	2.09 (ff_10)	1.56 (fs_10)	1.16 (fs_11)	1.7 (fs_10)
10	2 (no peak)	1.51 (fs_5)	1.16 (fs_11)	1.44 (fs_6)
100	2 (no peak)	1.52 (fs_0)	1.15 (fs_9)	1.3 (fs_2)

Table 14: Peak values for Power Cycles at 60 °C and all process corners

4.12 Discontinuities

This test method is, like the Power Cycles in section 4.11, taken from the ISO 16750-2:2010 and simulates a circuit-break scenario, e.g when a fuse is triggered. This will lead to a temporary interruption in the power supply and, as a consequence, a drop of the input current. The rise and fall times should not exceed 10 ms and the supply signal drops by 62.5% and returns to the initial value after 100 ms[11]. Figure 4.45 shows the load profile, generate by the ipwlf-source.

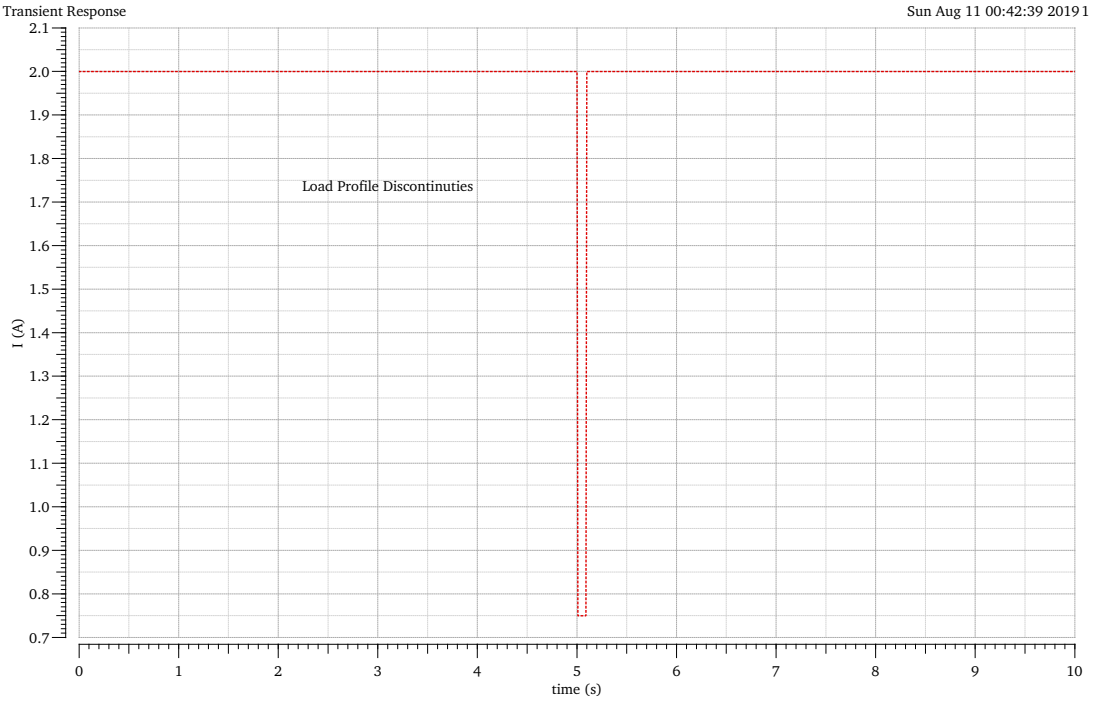

Figure 4.45: Load profile according to the ISO 16750-2:2010 Standard

The transient simulation is run with the following parameters.

- Input current: 1 A to 2 A
- rload: 1.2 GΩ, 240 Ω, 12 Ω, 1.2 Ω
- rise/fall-time: 1 ms, 10 ms, 100 ms
- Temperatures: −40 °C, −20 °C, 27 °C, 60 °C
- Process variations: ff, ss, fs, sf, tt

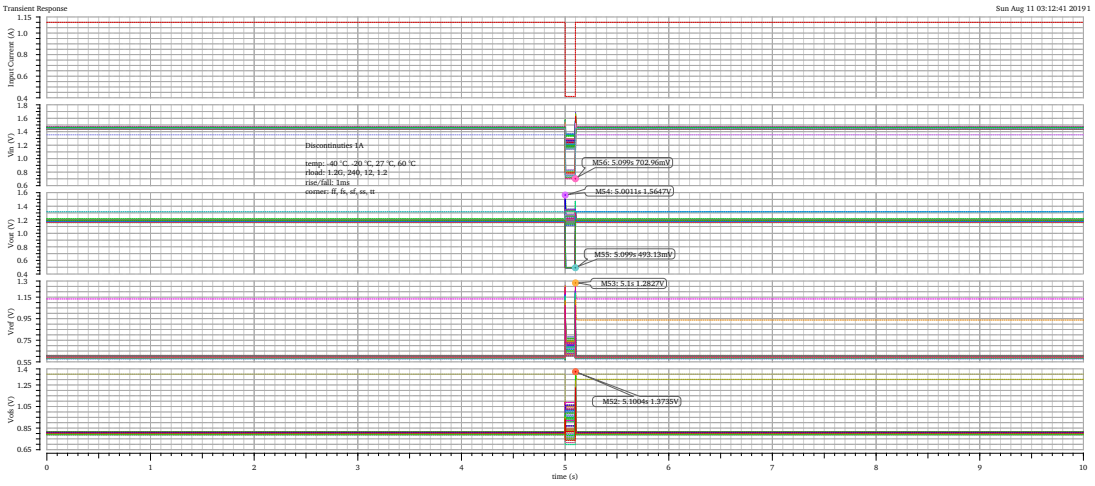

Figure 4.46: Results for rise/fall-time 1 ms for itpower = 1 A, all temps, loads and corners

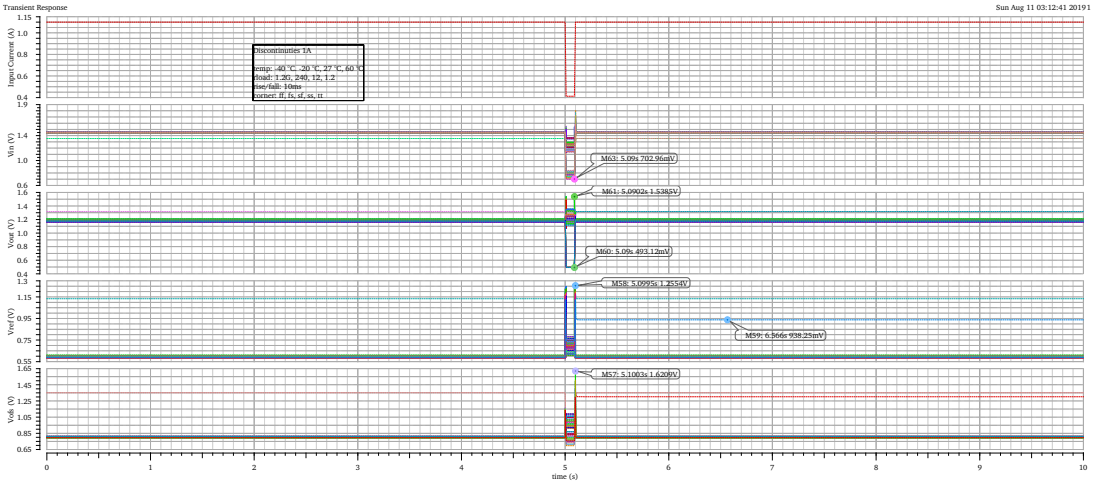

Figure 4.47: Results for rise/fall-time 10 ms for itpower = 1 A, all temps, loads and corners

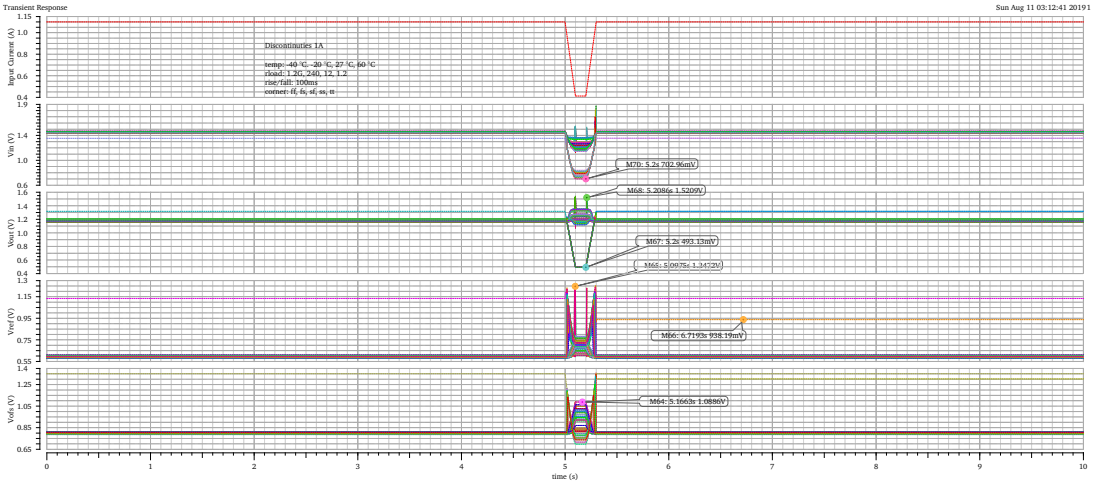

Figure 4.48: Results for rise/fall-time 100 ms for itpower = 1 A, all temps, loads and corners

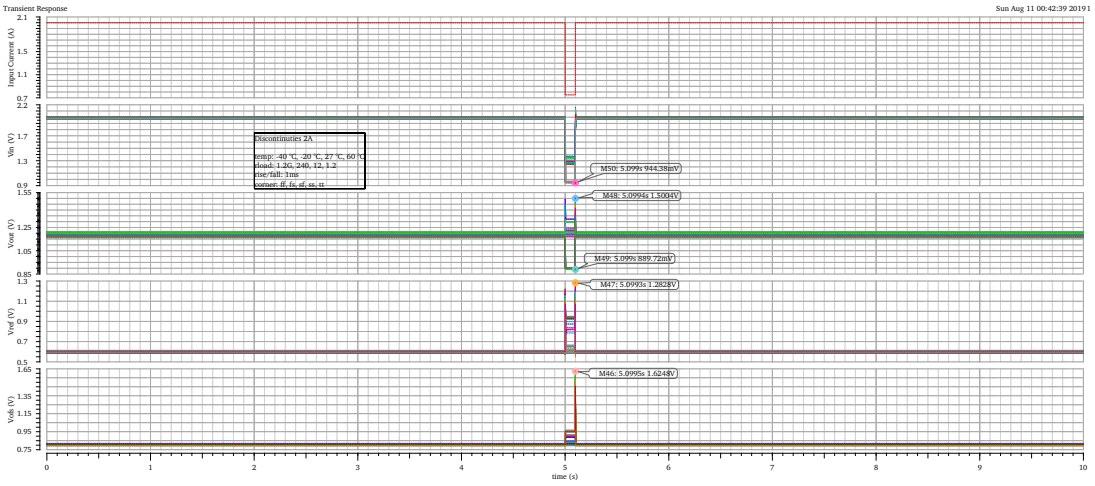

Figure 4.49: Results for rise/fall-time 1 ms for itpower = 2 A, all temps, loads and corners

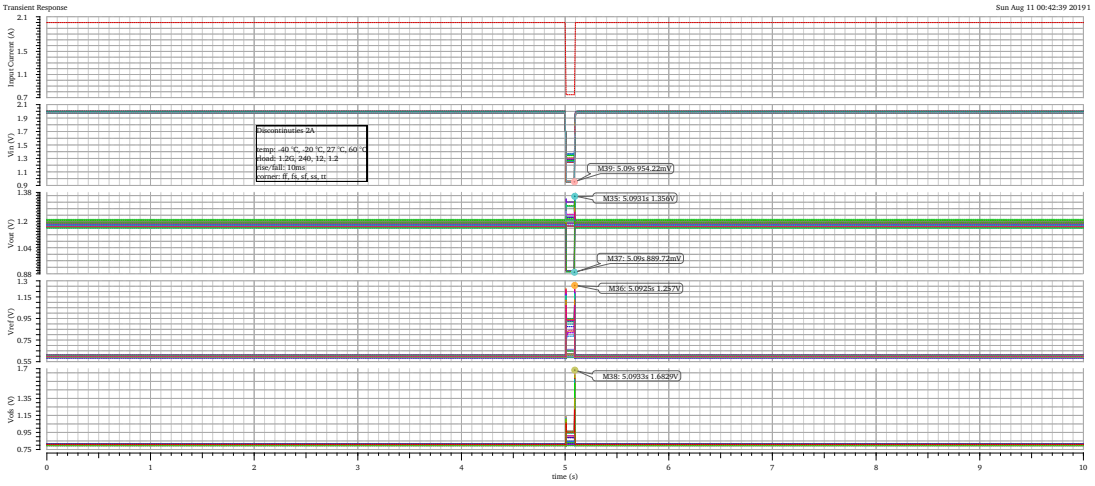

Figure 4.50: Results for rise/fall-time 10 ms for itpower = 2 A, all temps, loads and corners

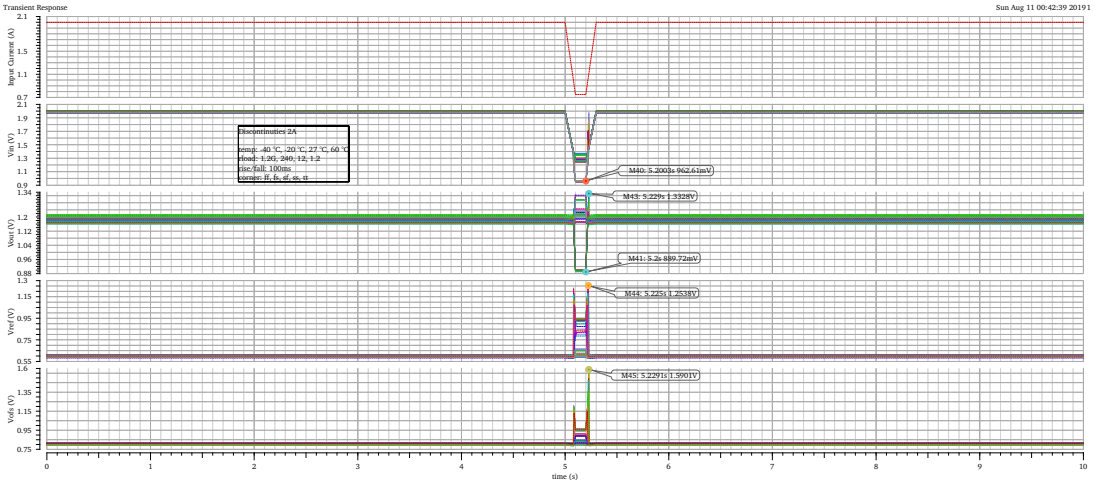

Figure 4.51: Results for rise/fall-time 100 ms for itpower = 2 A, all temps, loads and corners

It can be seen that all tests passed without the appearance of oscillations. Around the point of interruption, the input voltage drops to around 700 mV for the 1 A-load profile and to approximately 950 mV for 2 A. This results in a temporary breakdown of V_{out} and short peaks in V_{ref} and V_{ofs}. After the interruption of the supply current, all voltages return to their specified values without noticeable problems. Low-temperature corner tend to generate the highest peaks. Furthermore, the combination of an input current of 1 A and a load resistance of 1.2 Ω can, likewise to other simulations, cause abnormal behavior of the regulators voltages.

4.13 Monte-Carlo Simulation

The Monte-Carlo Simulation is a stochastic method based on random experiments and the law of large numbers. It can be used for problems, which are not solvable with an analytical approach or to emulate a random variation of specific parameters. The circuit is examined with respect to the influence of process- and mismatch variations. While process covers the corner variation between chips and especially between different wafers, mismatch considers variations between devices integrated on the same chip, which are located close to each other. Therefore parameters like the W and L of adjacent transistors are taken into account. The model files mc_lib (process) and mismatch_lib (mismatch) contain the necessary information to simulate statistical behavior and are provided directly from TSMC. Process and mismatch variations are both tested separately. Two tests have been defined: variations of the DC operating points for V_{out}, V_{in}, V_{ref} and V_{ofs} as well as the offset voltages at the amplifier inputs (A1 - A4) are considered. Secondly the slope of the input voltage and the offset voltage are examined with a DC sweep and are calculated as described in section 4.9. The DC operating points are simulated with an input current of 1.05 A and 2 A. For the slope and the offset, a DC sweep of the input current from 0 A to 2 A is set. The additional varying parameters are listed below.

- Statistical variations: process and mismatch
- rload: 1.2 GΩ, 240 Ω, 12 Ω, 1.2 Ω
- Temperatures: −40 °C, −20 °C, 27 °C, 60 °C
- External Resistor: 600Ω
- Simulation specs DCVoltage: V_{in} (1.4 V to 2 V), V_{out} (1.15 V to 1.25 V), V_{ref} (580 mV to 620 mV), V_{ofs} (780 mV to 820 mV)
- Simulation specs Rslope: $Rslope$ (580 Ω to 620 Ω), $Vofs\_Calc$ (780 mV) to 820 mV)

Table 15 summarizes all the results of the Monte-Carlo simulation by pointing out minimal, maximal and mean values for each examined output and furthermore including the standard deviation[11].

Test	Name	Yield	Min	Max	Mean	Std Dev	Errors
DCVoltage_Process							
	VDC_Vin	86.18	1.293E+0	2.026E+0	1.70E+0	284.37E-3	2
	VDC_Vout	95.35	1.117E+0	1.274E+0	1.201E+0	24.19E-3	2
	VDC_Vref	98.5	554.40E-3	652.70E-3	604.40E-3	10.68E-3	3
	VDC_Vofs	77.74	748.80E-3	1.294E-3	811.20E-3	56.52E-3	2
	Ofs_Amp_A1	x	-331.70E-3	-166.0E-6	-237.57E-6	7.41E-6	6
	Ofs_Amp_A2	x	-5.155E-6	4.224E-3	273.0E-6	629.1E-6	2
	Ofs_Amp_A3	x	-85.93E-3	-20.2E-6	-1.24E-3	305.0E-6	5
	Ofs_Amp_A4	x	-747.10E-6	9.455E-3	-402.30E-6	2.764E-6	2
DCVoltage_Mismatch							
	VDC_Vin	82.06	1.283E+0	2.051E+0	1.704E+0	62.8E-3	0
	VDC_Vout	87.86	1.098E+0	1.287E+0	1.196E+0	61.22E-3	0
	VDC_Vref	95.20	309.60E-3	777.20E-3	602.10E-3	31.02E-3	0
	VDC_Vofs	66.8	645.70E-3	1.08E+0	803.5E-3	25.17E-3	0
	Ofs_Amp_A1	x	-148.3E-3	6.954E-3	-374E-6	3.61E-3	0
	Ofs_Amp_A2	x	-2.24E-3	4.55E-3	263.60E-6	635.63E-6	
	Ofs_Amp_A3	x	-86.31E-3	2.88E-3	-1.457E-3	3.34E-3	0
	Ofs_Amp_A4	x	-2.74E-3	915.7E-6	-469.40E-6	567.89E-6	0
Rslope_Process							
	Rslope	78	580.40E-3	753.40E-3	592.80E-3	9.57E-3	0
	Vofs_Calc	77.18	507.90E-3	853.4E-3	801.70E-3	22.49E-3	0
	Rslope_min	x	564.20E-3	595.1E-3	585.80E-3	2.45E-3	2
	Rslope_max	x	585.80E-3	819.90E-3	596.50E-3	2.94E-3	2
	Rslope_average	x	580.50E-3	598.50E-3	591.90E-3	9.86E-3	2
Rslope_Mismatch							
	Rslope	71.25	581.50E-3	779.20E-3	593.70E-3	14.94E-3	0
	Vofs_Calc	68.40	487.80E-3	860.00E-3	800.20E-3	31.75E-3	0
	Rslope_min	x	566.10E-3	597.80E-3	584.95E-3	2.46E-3	4
	Rslope_max	x	584.60E-3	607.30E-3	593.42E-3	2.75E-3	4
	Rslope_average	x	581.50E-3	602.80E-3	591.30E-3	2.32E-3	4

Table 15: Results for the Monte-Carlo analysis of DC-Voltage and Rslope

Figures 4.52 to 4.62 visualize the Gaussian distributions of the DCVoltage- and the RSlope test, seperated in process- and mismatch variations.

DCVoltages Process

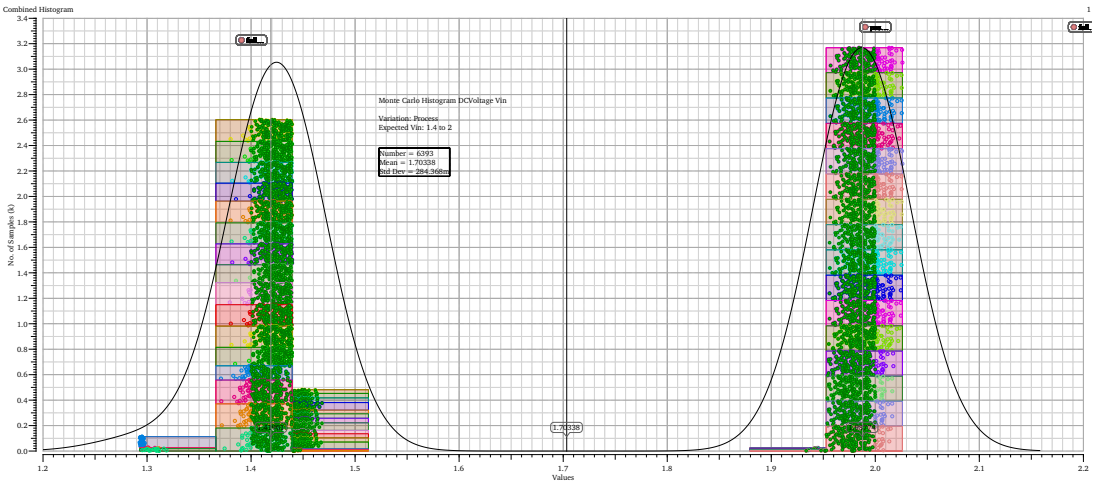

Figure 4.52: Histogram for all Monte-Carlo runs with process variation of V_{in}

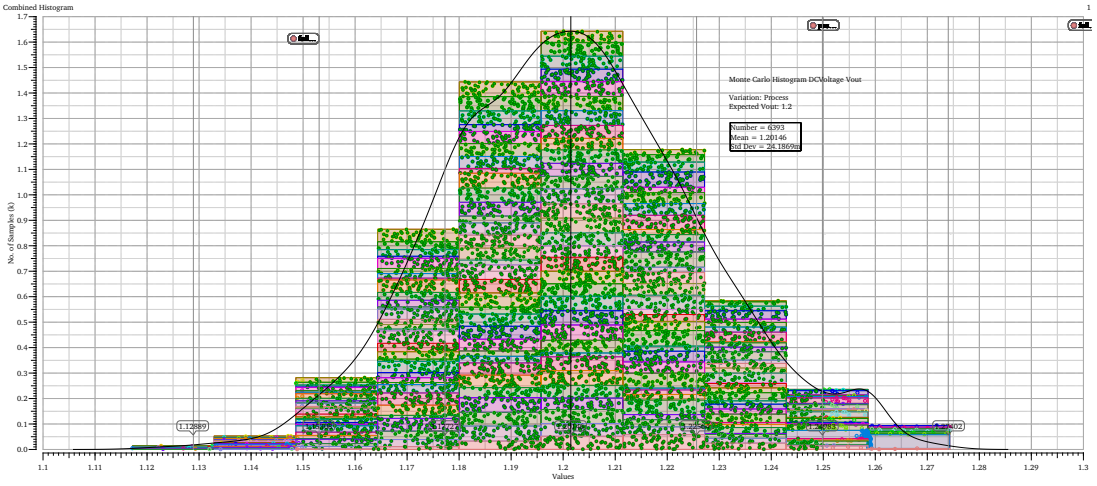

Figure 4.53: Histogram for all Monte-Carlo runs with process variation of V_{out}

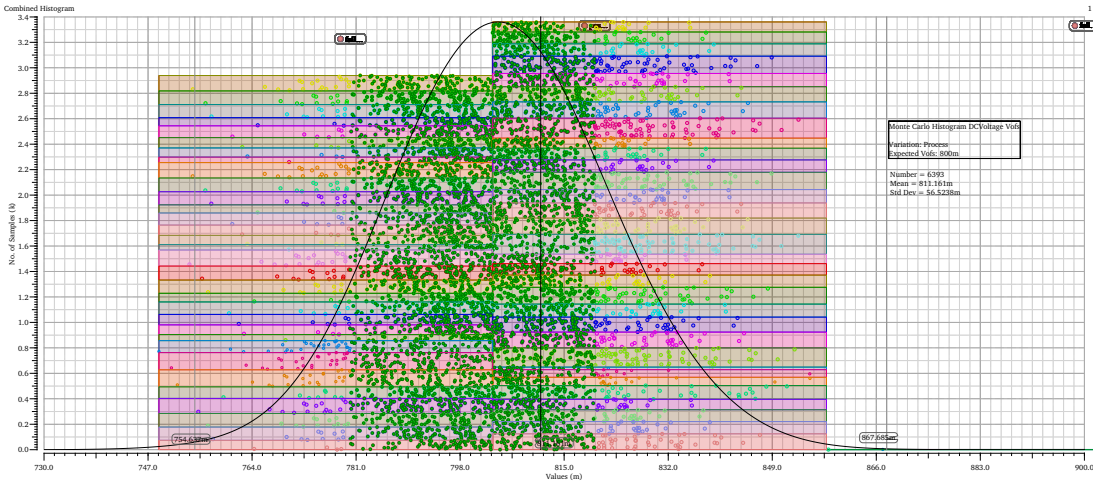

Figure 4.54: Histogram for all Monte-Carlo runs with process variation of V_{ofs}

DCVoltages Mismatch

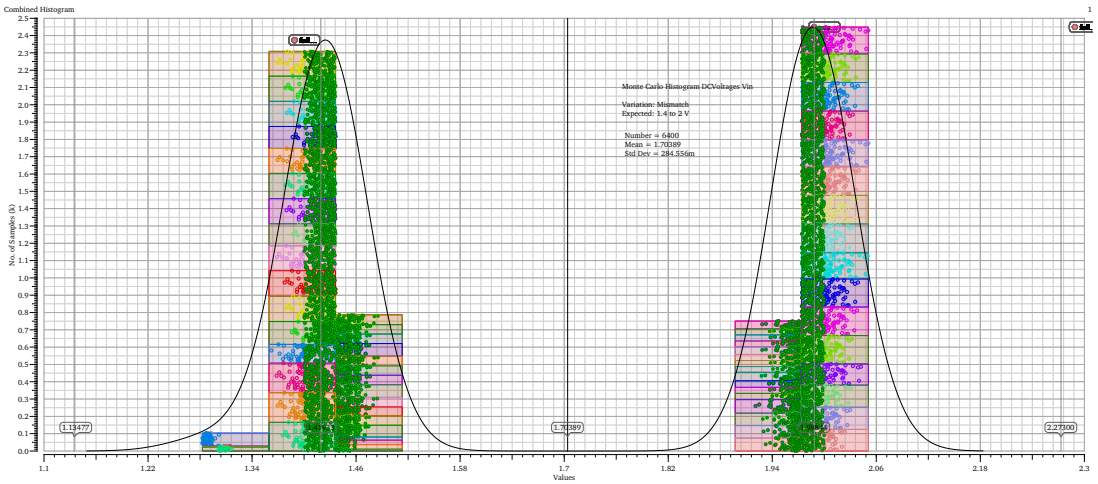

Figure 4.55: Histogram for all Monte-Carlo runs with mismatch variation of V_{in}

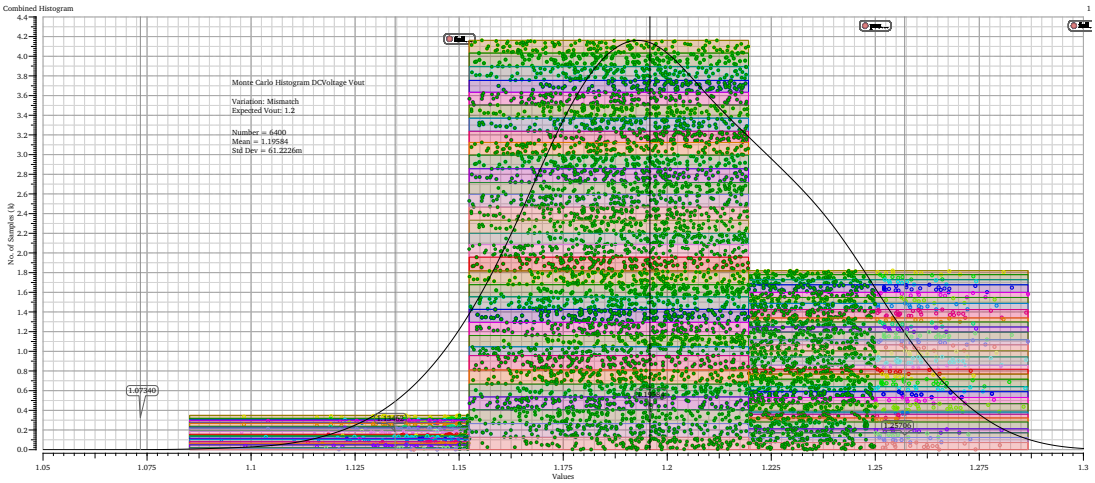

Figure 4.56: Histogram for all Monte-Carlo runs with mismatch variation of V_{out}

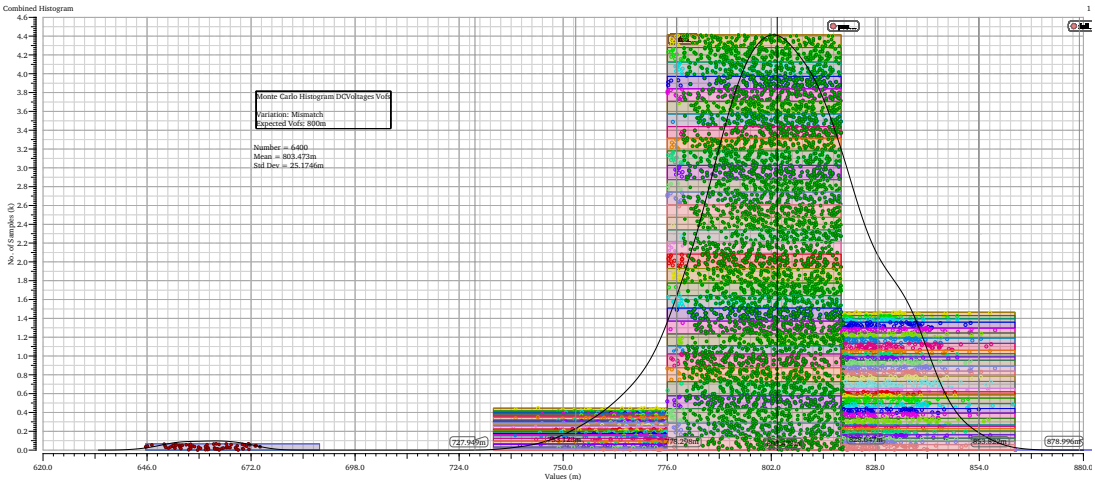

Figure 4.57: Histogram for all Monte-Carlo runs with mismatch variation of V_{ofs}

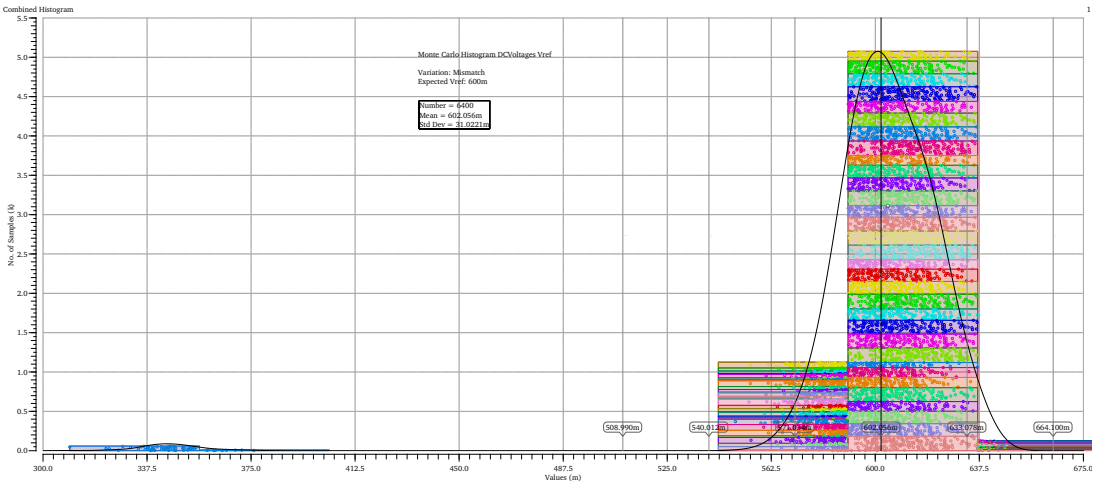

Figure 4.58: Histogram for all Monte-Carlo runs with mismatch variation of V_{ref}

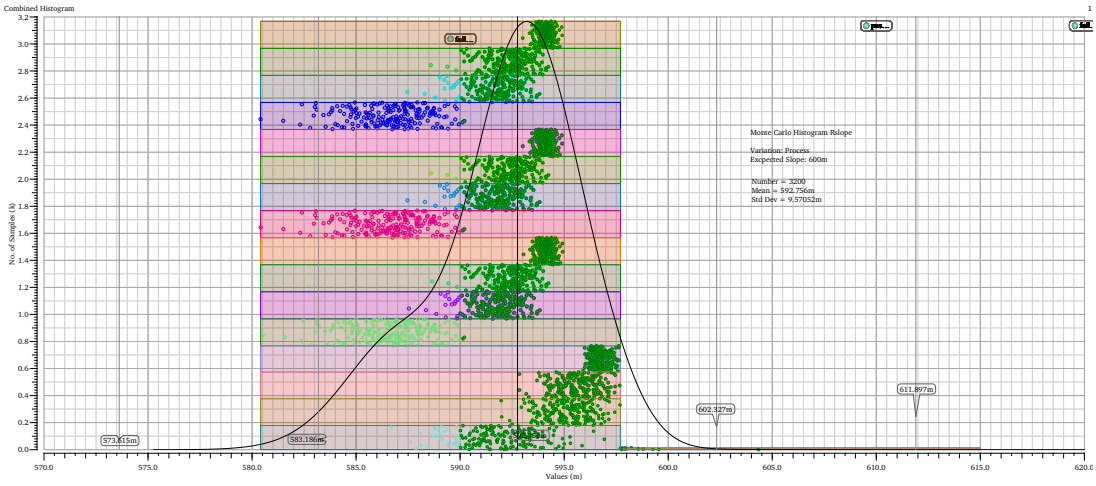

Figure 4.59: Histogram for all Monte-Christo runs with process variation of the Rslope-test

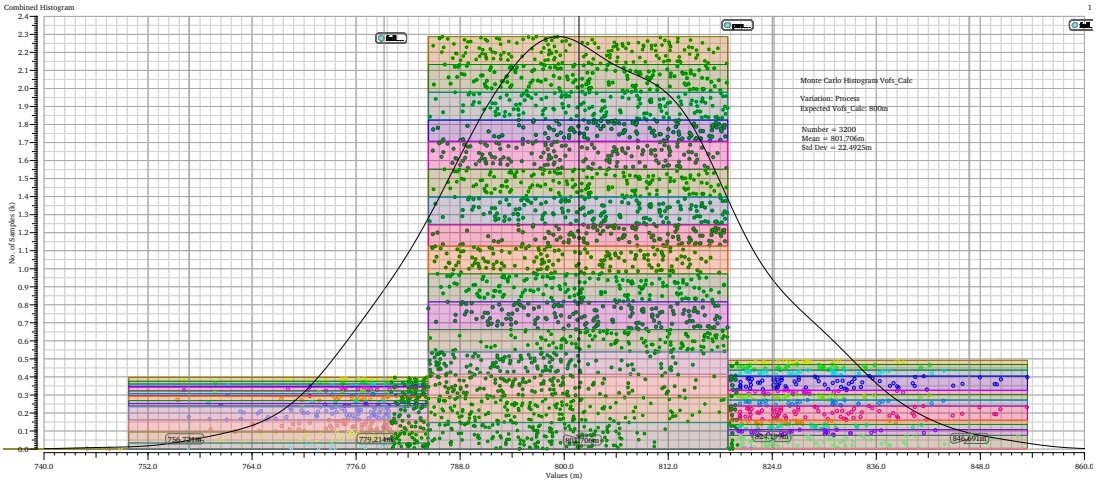

Figure 4.60: Histogram for all Monte-Carlo runs with process variation of the calculated V_{ofs}

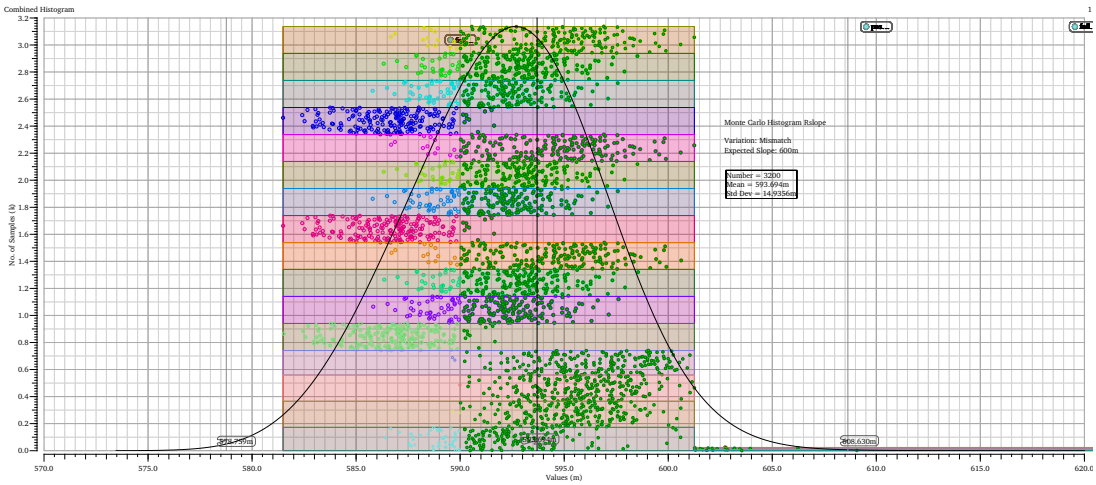

Figure 4.61: Histogram for all Monte-Carlo runs with mismatch variation of the Rslope-test

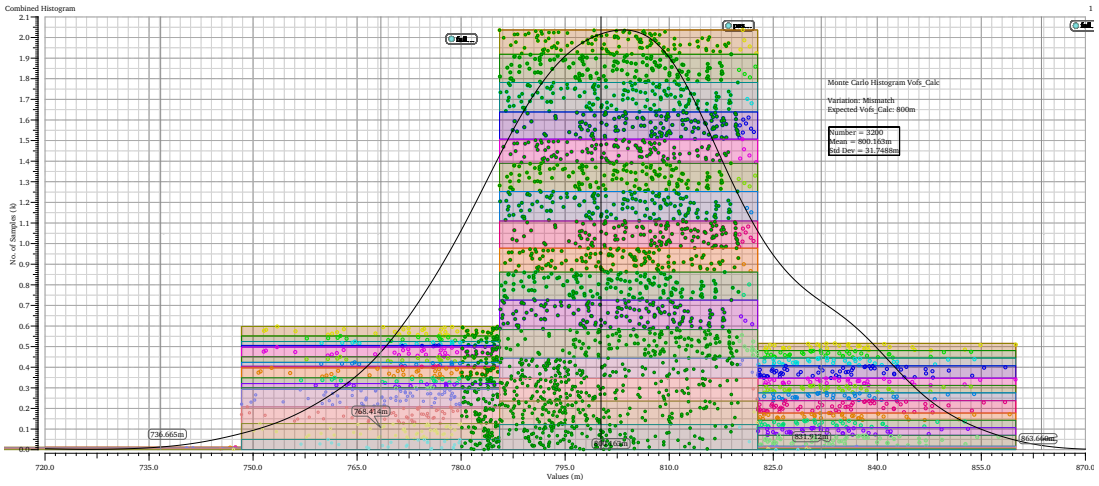

Figure 4.62: Histogram for all Monte-Carlo runs with mismatch variation of the calculated V_{ofs}

DCVoltages Mismatch Offset Amplifiers A1-4

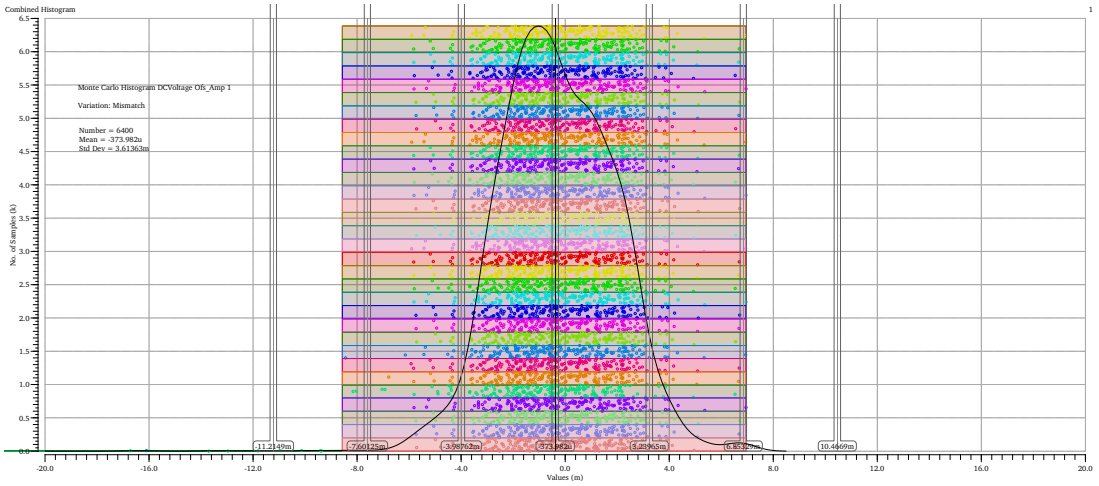

Figure 4.63: Histogram for all Monte-Carlo runs with mismatch variation of OfsAmp A1

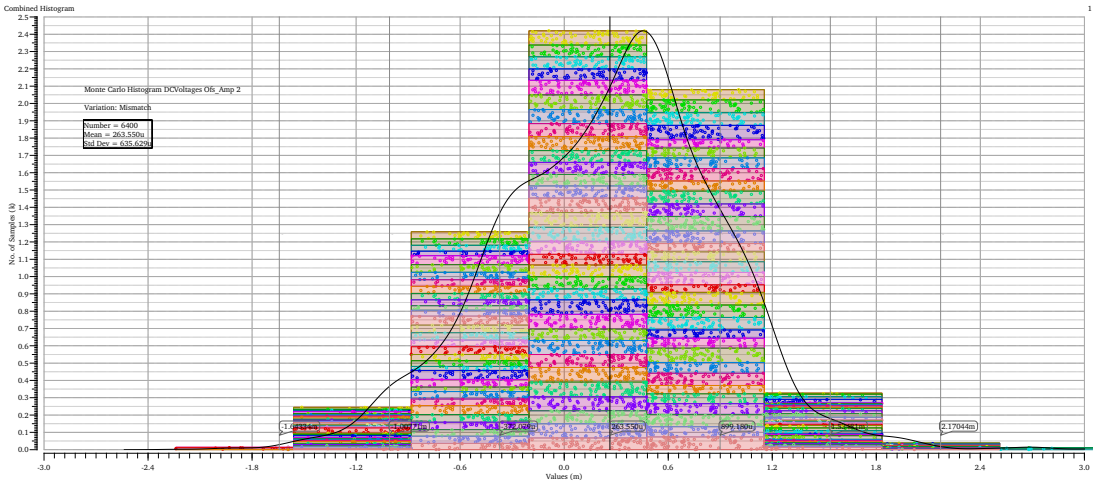

Figure 4.64: Histogram for all Monte-Carlo runs with mismatch variation of OfsAmp A2

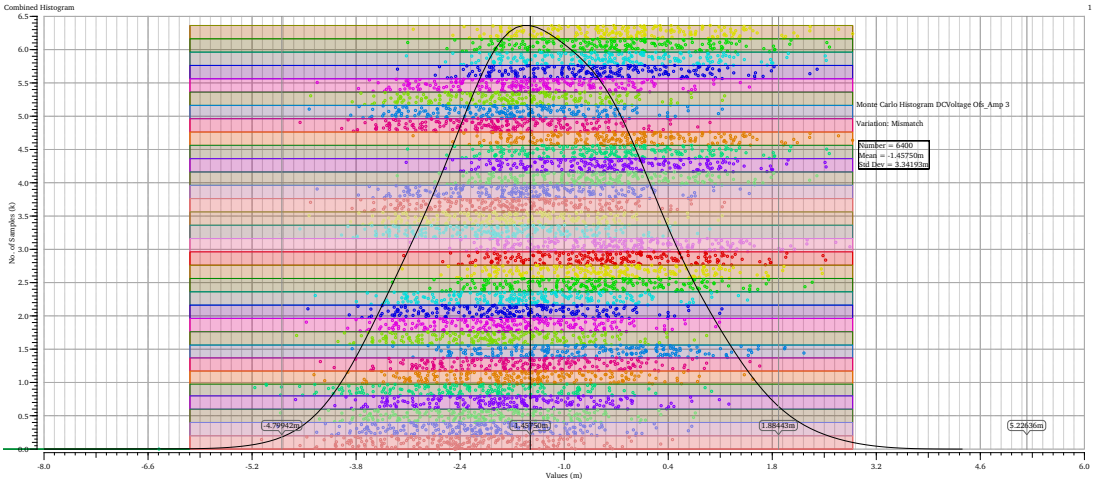

Figure 4.65: Histogram for all Monte-Carlo runs with mismatch variation of OfsAmp A3

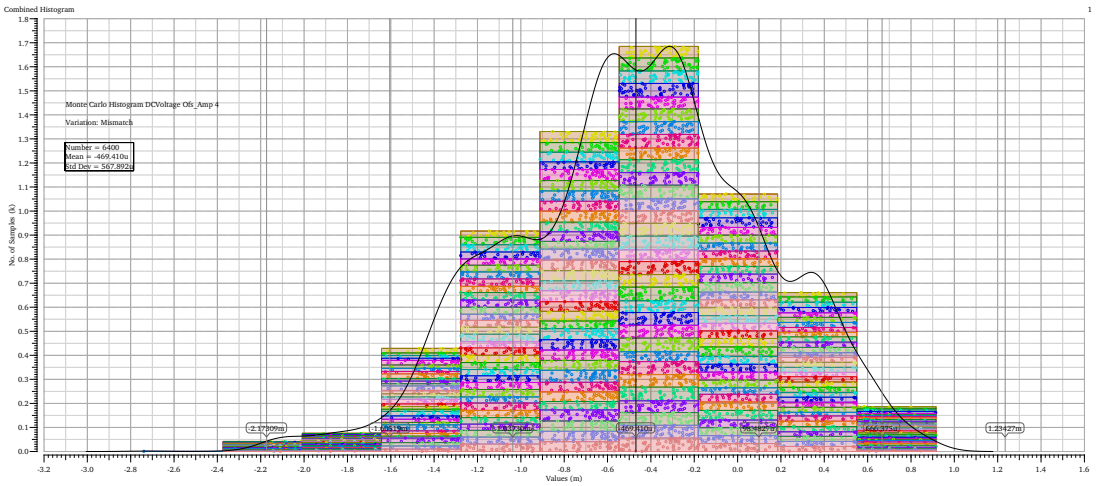

Figure 4.66: Histogram for all Monte-Carlo runs with mismatch variation of OfsAmp A4

The results of the Monte-Carlo analysis provide an overview of the regulators voltage behavior when parameters are changed randomly. This contains variations in process and wafer characteristics, like doping density, reproduced by the process model data and device mismatches, covered with the mismatch data. As provided in table 15 and figures 4.52 to 4.62 all voltages are mostly within their specifications, with outliers in some Monte-Carlo iterations. In a general view, expressed by the standard mean values, the results are satisfying for all regarded voltages.

5 Conclusion

In this résumé, individual test results are not reflected in details as they are adequately discussed in their particular sections. In general, the verification of the SLDO test chip was a complex and demanding task. Due to the enhanced complexity of the chip in comparison to earlier iterations, a range of particular changes to the Cadence test bench has been made. Although previous test chips have been verified with a similar approach, it was not possible to outright adopt an existing test bench. Due to new specifications, convergence issues as a result of an increased circuit complexity and other reasons, many new features and enhancements were implemented to create an applicable test bench with the possibility to deliver coherent verification results. Nevertheless, it was especially the work of my fellow student and friend Mr. Jeremias Kampkötter, which made my work on this thesis so much easier. With the verification of the RD53A test chip A as part of his second master project work, he committed a foundation to build up on, even if a large amount of adaptions were required to fit this base into the test chip C verification. For this, i want to commit my particular thanks.

One of the major difficulties during the verification was the enormous amount of simulation errors due to convergence problems across all tests and analysis types. This went up to an extent where it was not possible to achieve reasonable results for a bigger part of the planned tests. In consultation with Prof. Dr. Karagounis, many approaches to engage this circumstance were tested, including contacting the Cadence support. After a phase with little progress, the use of transient nodeset files was defined as the most viable option. Although this method did indeed improve the convergence issue, it comes with a major downside: Every process corner and temperature requires an individual nodeset file, adding up in 20 separate files. In addition to that, Cadence does not provide any straight way to include these files automatically into the corner setup. As a consequence, all temperatures and process variations have to be set up separately. This is the reason, why the test bench for test chip C has a tremendous amount of different corners and a very blown up ADE-XL state, resulting in high complexity especially for uninvolved users. Furthermore, this method forces a compromise when it comes to Monte-Carlo simulations, because it is not possible to configure separate process corners for these tests, as their occurrences in Monte-Carlo are random. This concerns the trimming setting for the reference current, as it is process corner dependent. By using the setting for the typical corner, a middle ground was chosen for this scenario. However, within the time scope of this thesis it was the best approach to implement.

Apart from the above-mentioned limitations and hurdles, the stability analysis was the only simulation generating implausible results, which could not be resolved up to the point where the work on this thesis draws to an end. Deeper troubleshooting on the schematic/circuit-side is required in this case and as a consequence - as these actions are not part of this thesis - the stability analysis is - for now - excluded from this documentation.

To encapsulate my experiences gained during the work on this project, I can outline that it was a great opportunity to contribute in a development process of a microelectronic circuit, lead by the prestigious ATLAS collaboration. The significance of simulation-based verification as part of a development process must not be underestimated. The intensive work with the Cadence Virtuoso EDA Software was a beneficial side effect from which I personally will profit as an engineer.

Last but not least, I would like to thank Prof. Dr. Michael Karagounis for offering me the opportunity to work as a part of the ATLAS collaboration on a project that really matters, for his continuous support and his entertaining way to motivate students.

Florian Winkler

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A Appendix

A.1 CD

Hiermit versichere ich an Eides statt, dass die von mir vorgelegte Prüfungsleistung selbstständig und ohne unzulässige fremde Hilfe erstellt worden ist. Alle verwendeten Quellen sind in der Arbeit so aufgeführt, dass Art und Umfang der Verwendung nachvollziehbar sind.

Dortmund, den 23. August 2019 .....

Unterschrift des Studierenden