Fachhochschule
Dortmund
University of Applied Sciences and Arts

Shunt-LDO Regulator

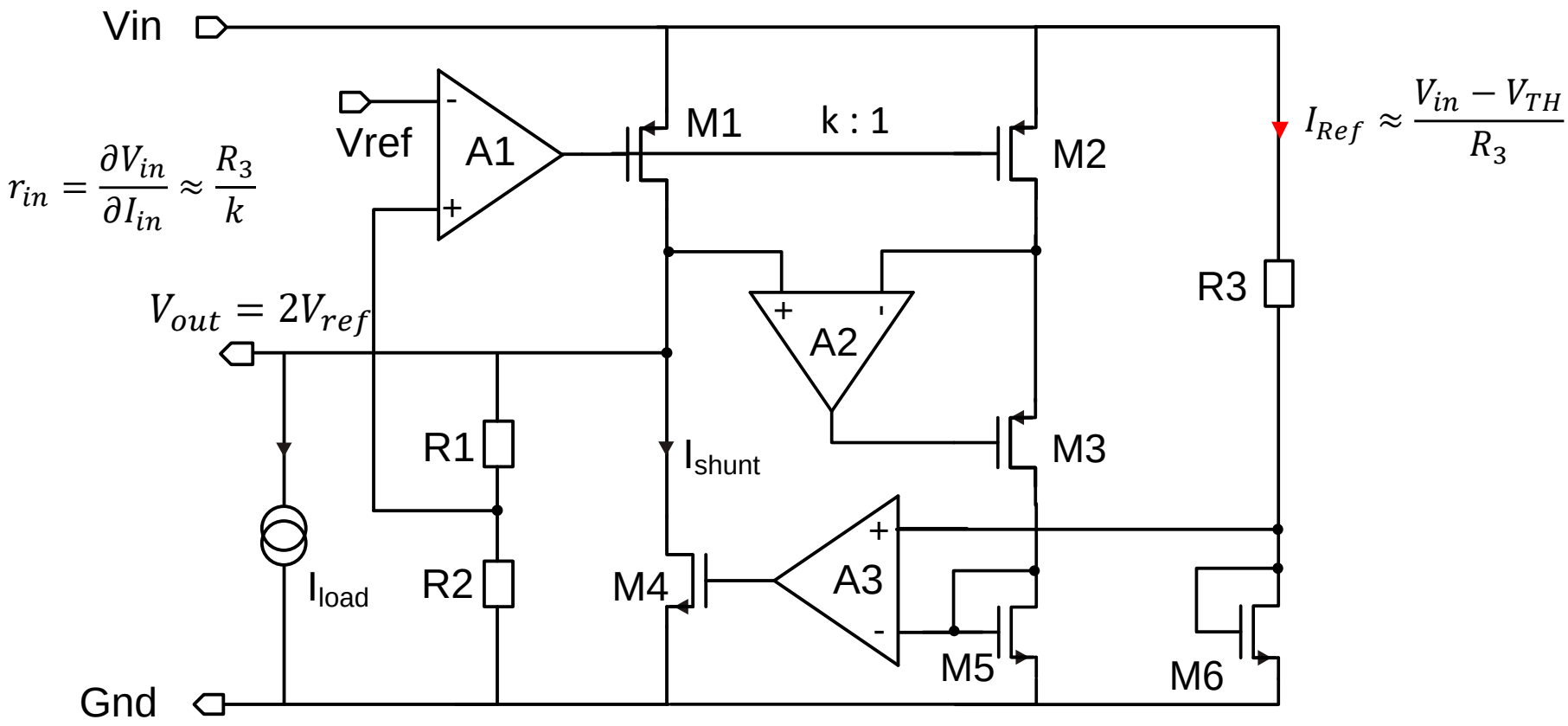
Evolution of the SLDO Regulator

08-September-2022

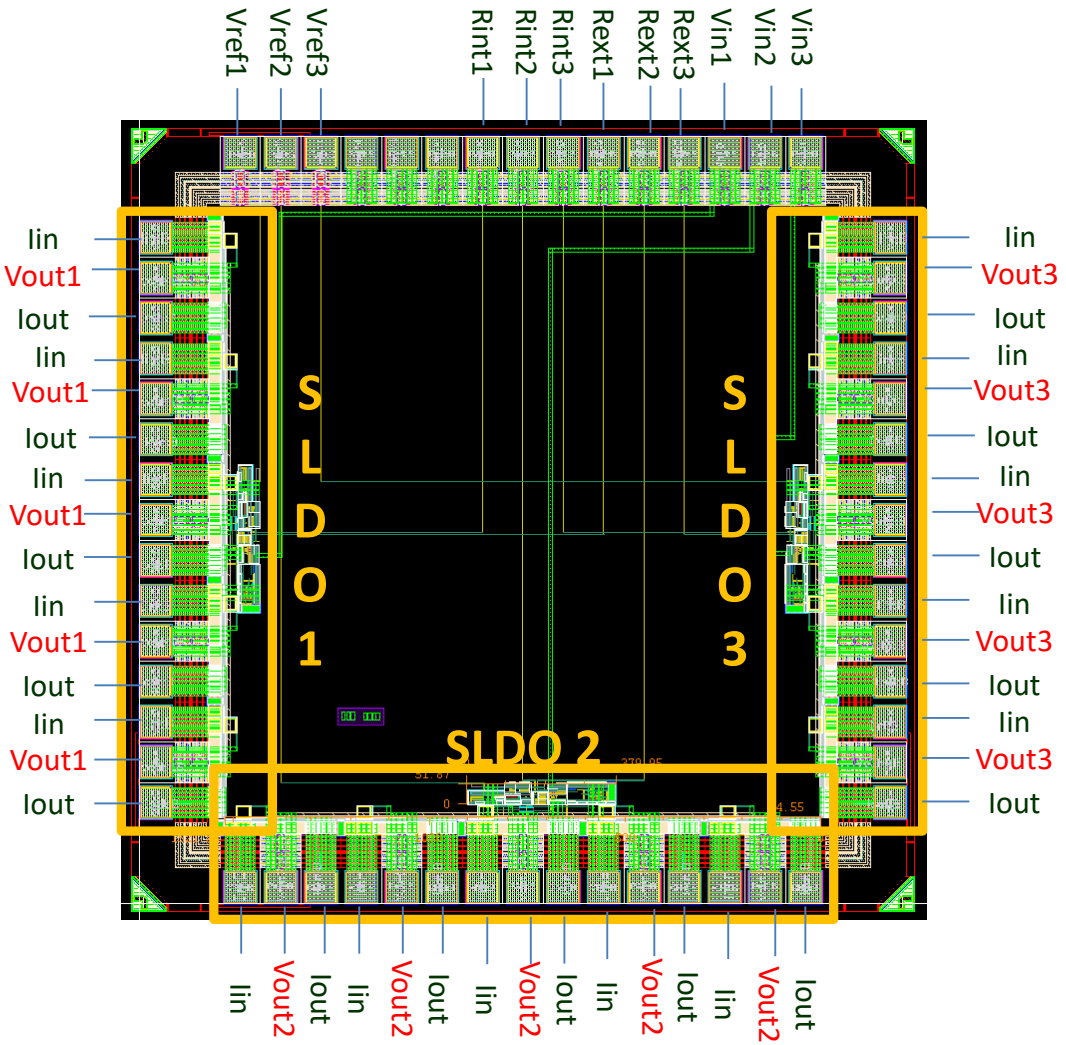
Michael Karagounis

Design Proposal PISA 2015

- SLDO design a la “FE-I4” ported from 130nm to 65nm
- Maximum load current of 500mA
- Maximum input voltage of 2V



Submitted Prototype February 19th 2016



Regulator – Type

Nominal Current 0.5 A

No Offset Voltage Calibration

Testchip - Content

3 regulator

Biasing Circuits

No Bandgap

Testchip – Size

2 mm x 2 mm

Pad – Count

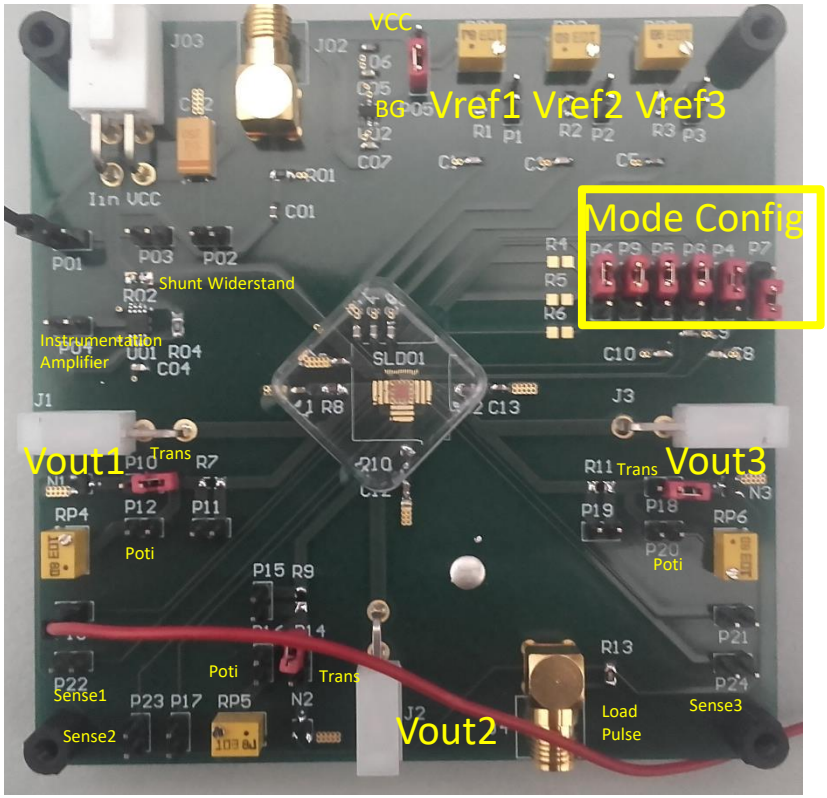
4 x 16 with 100 µm pitch

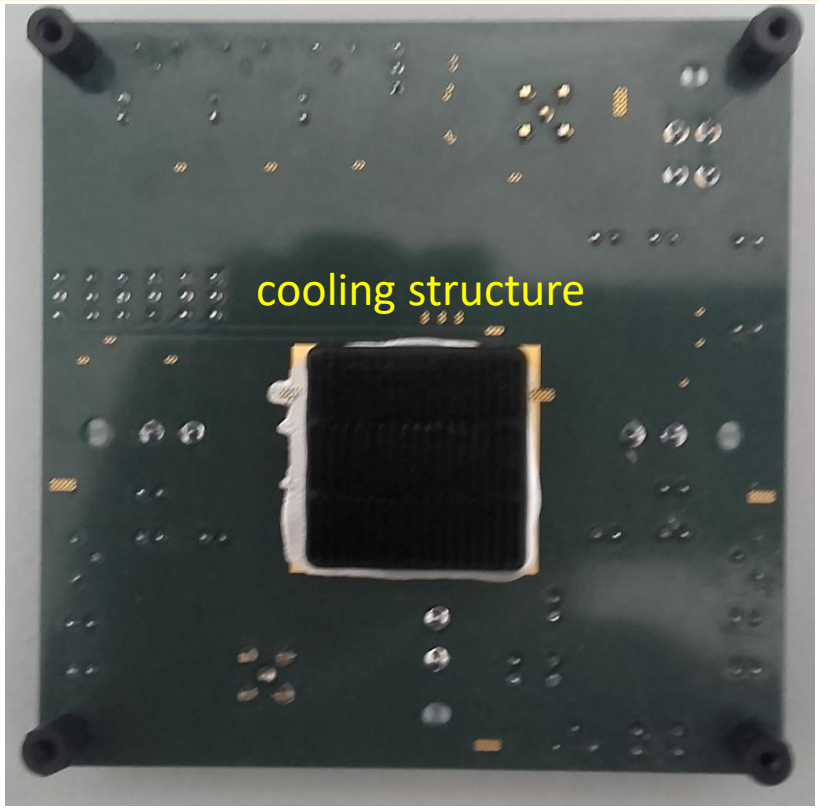
Area per Regulator:

45 µm x 1500 µm

50 µm x 380 µm

Test PCB





Supply Mode Jumper Configuration

P7: Regulator 1: (Top Voltage) / (Bottom Current) Supply Mode

P8: Regulator 2: (Top Voltage) / (Bottom Current) Supply Mode

P9: Regulator 3: (Top Voltage) / (Bottom Current) Supply Mode

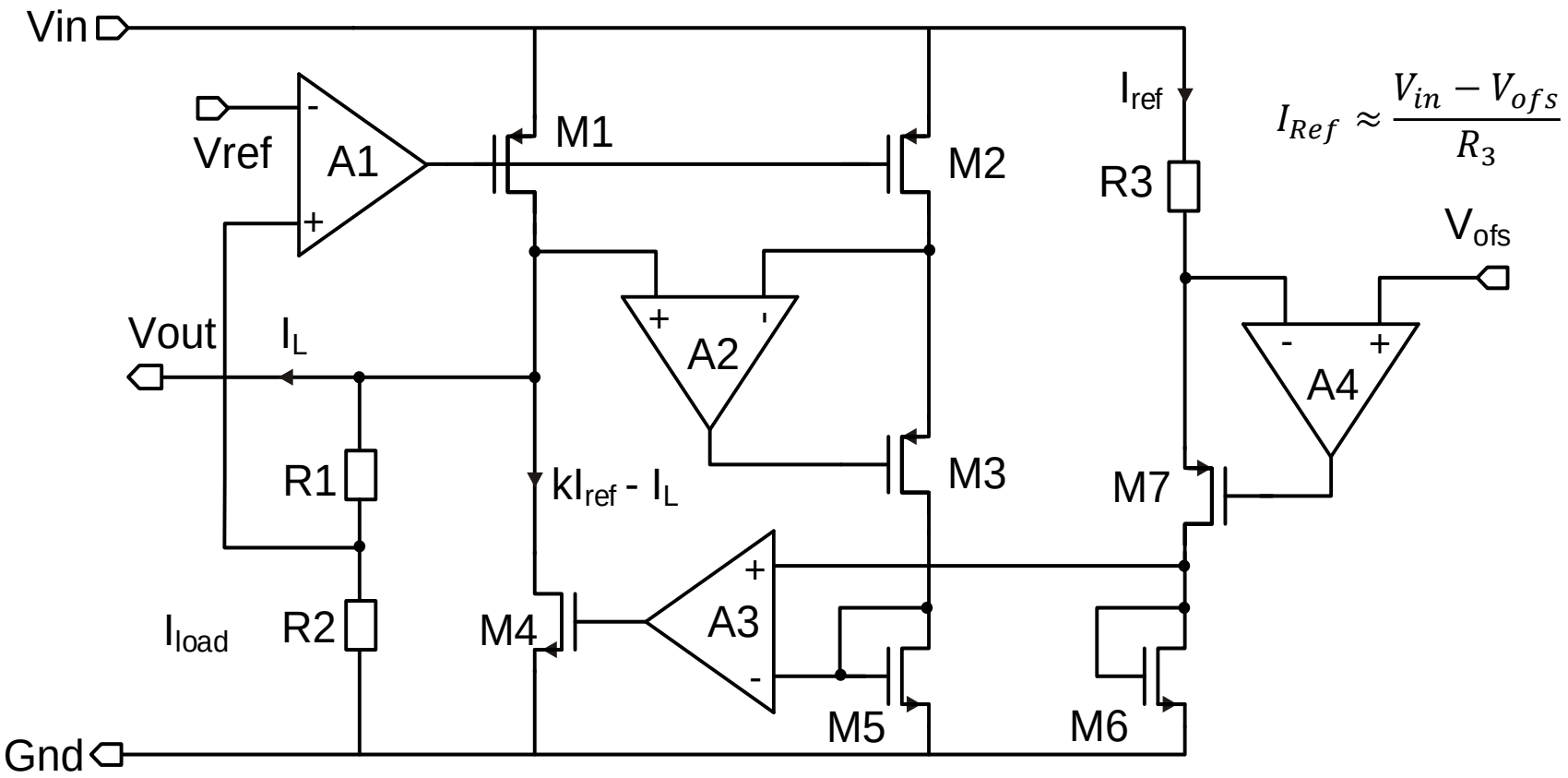
P4: Regulator 1: (Top Internal) / (Bottom External) Reference Resistor

P5: Regulator 2: (Top Internal) / (Bottom External) Reference Resistor

P6: Regulator 3: (Top Internal) / (Bottom External) Reference Resistor

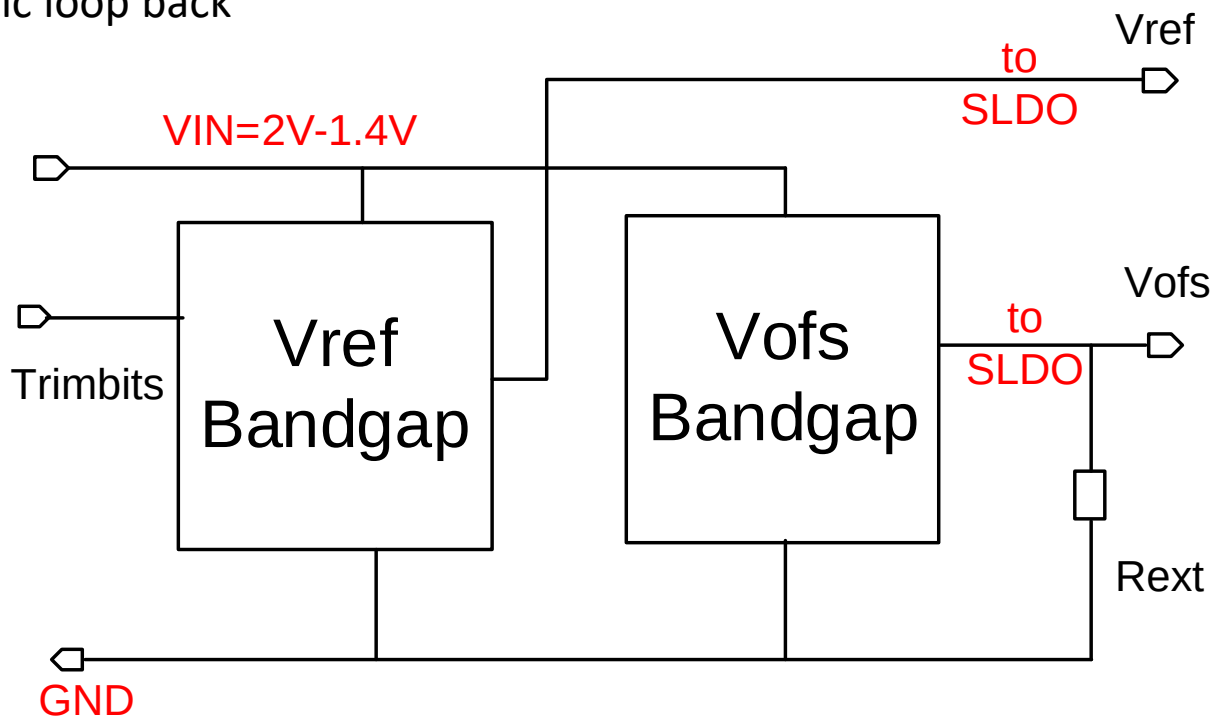
Introduction of Vofs

- Introduction of a defined and configurable Offset Voltage
- Maximum load current of 1A
- Maximum shunt current of 2A

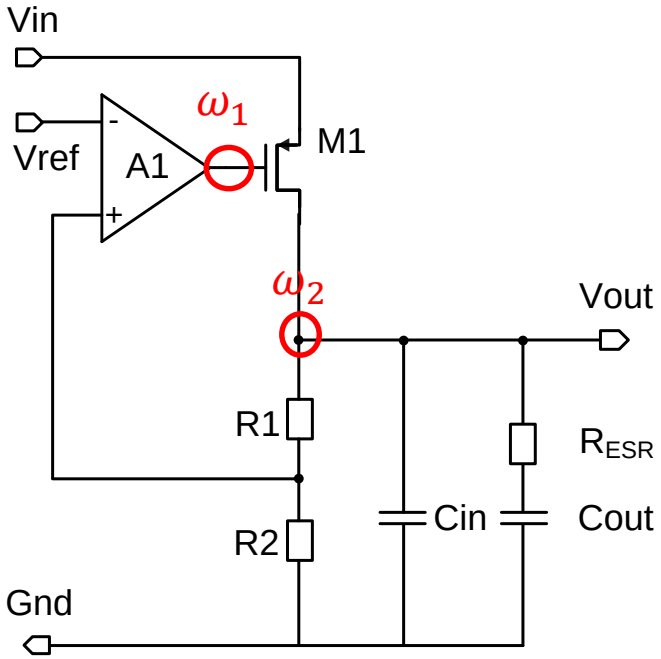


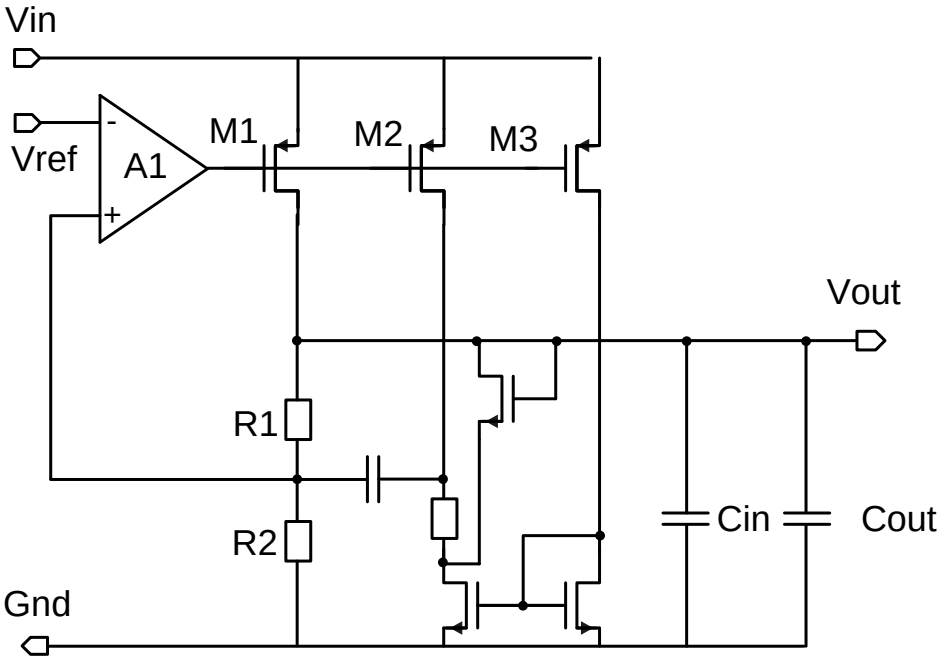
RD53A Bandgap Scheme

- 2 bandgap circuit per SLDO
  - Complex startup behavior
- Bandgaps directly powered by the input voltage
  - not ideal for good Line Regulation
  - problems with ovevoltages in trimming circuitry
- No levelshifters used for trimbits
  - Parasitic loop back



Low-ESR output capacitor compensation scheme





$$\omega_z = \frac{1}{R_{ESR} C_{out}}$$

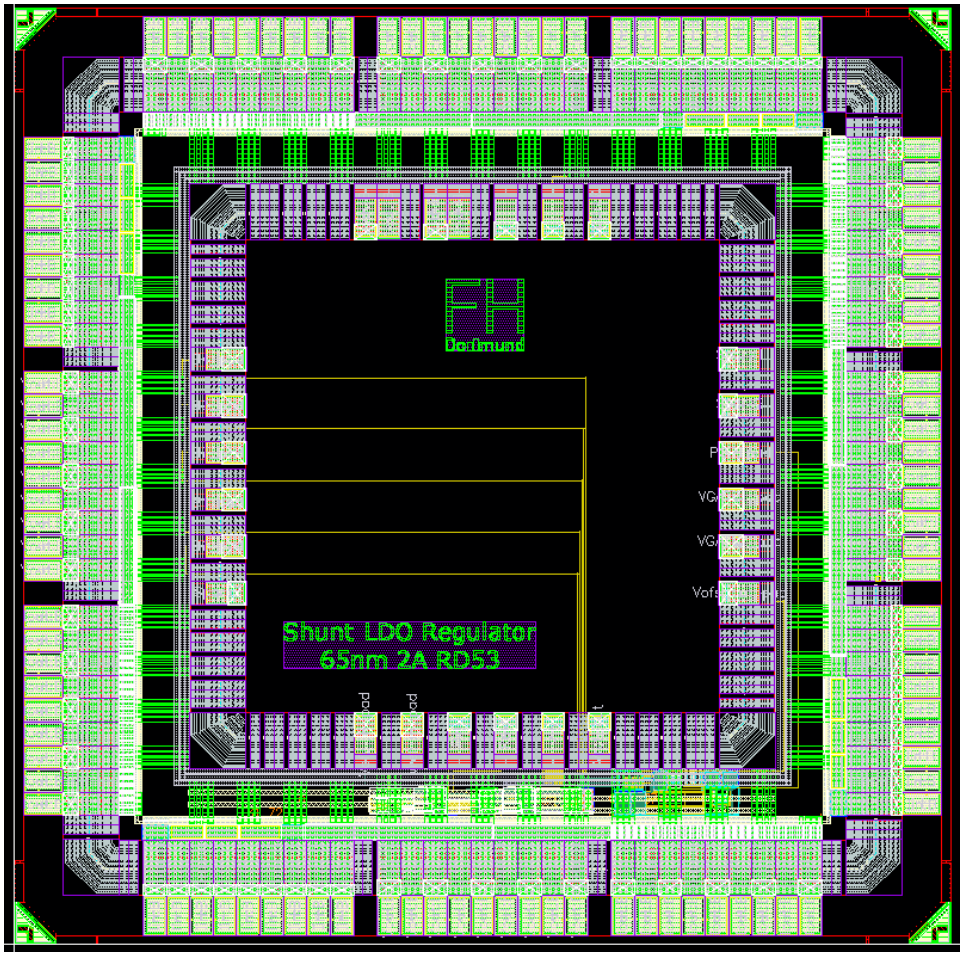
ω_z cancels pole ω_1

ω_2 pole at regulator is dominant

Fast voltage peak during load current change has stablizing effect

M. Bochenek, W. Dąbrowski, "Prototype linear voltage regulators for the ABC130 front-end chip for the ATLAS Inner Tracker Upgrade", *JINST*, vol. 8, pp. C01037, 2013

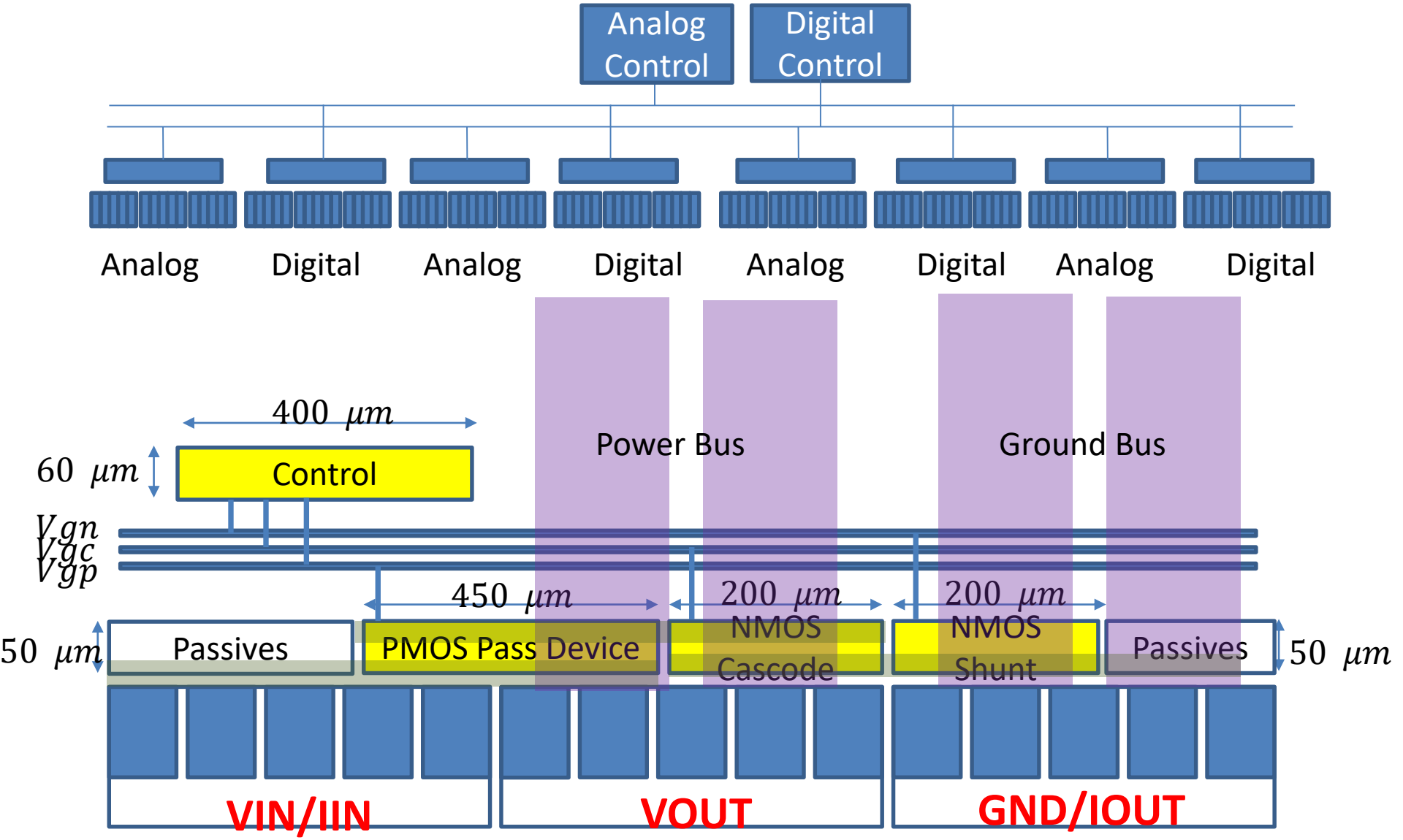
Submitted Prototype October 19th 2016



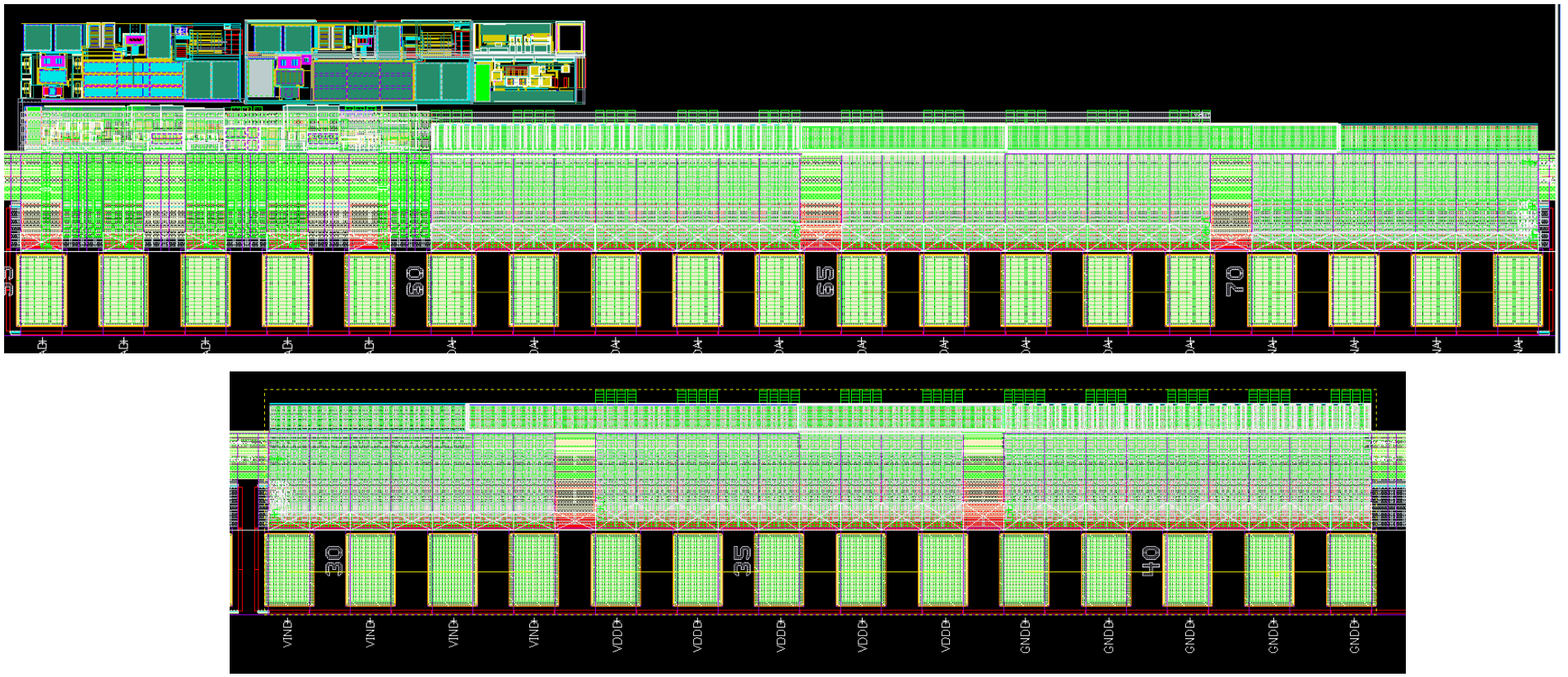
Regulator – Type
Nominal Current 1 A
Max Current 2 A
Offset Voltage Calibration

Testchip - Content
1 regulator
Biasing Circuits
Bandgap

Floorplan 2A Regulator for RD53A Chip



Layout for RD53A Chip April 2017

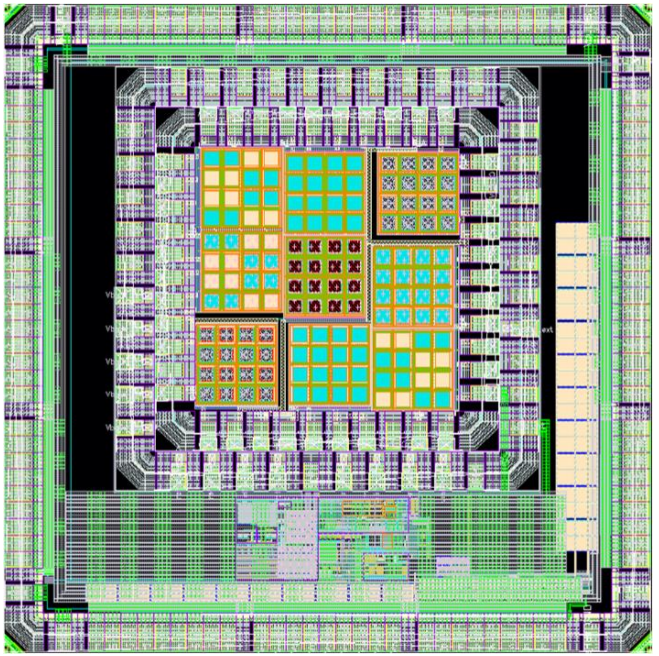


- Two layout cells per regulator
  - Master: power transistors plus control circuitry
  - Slave: power transistors

Monitoring Functionality

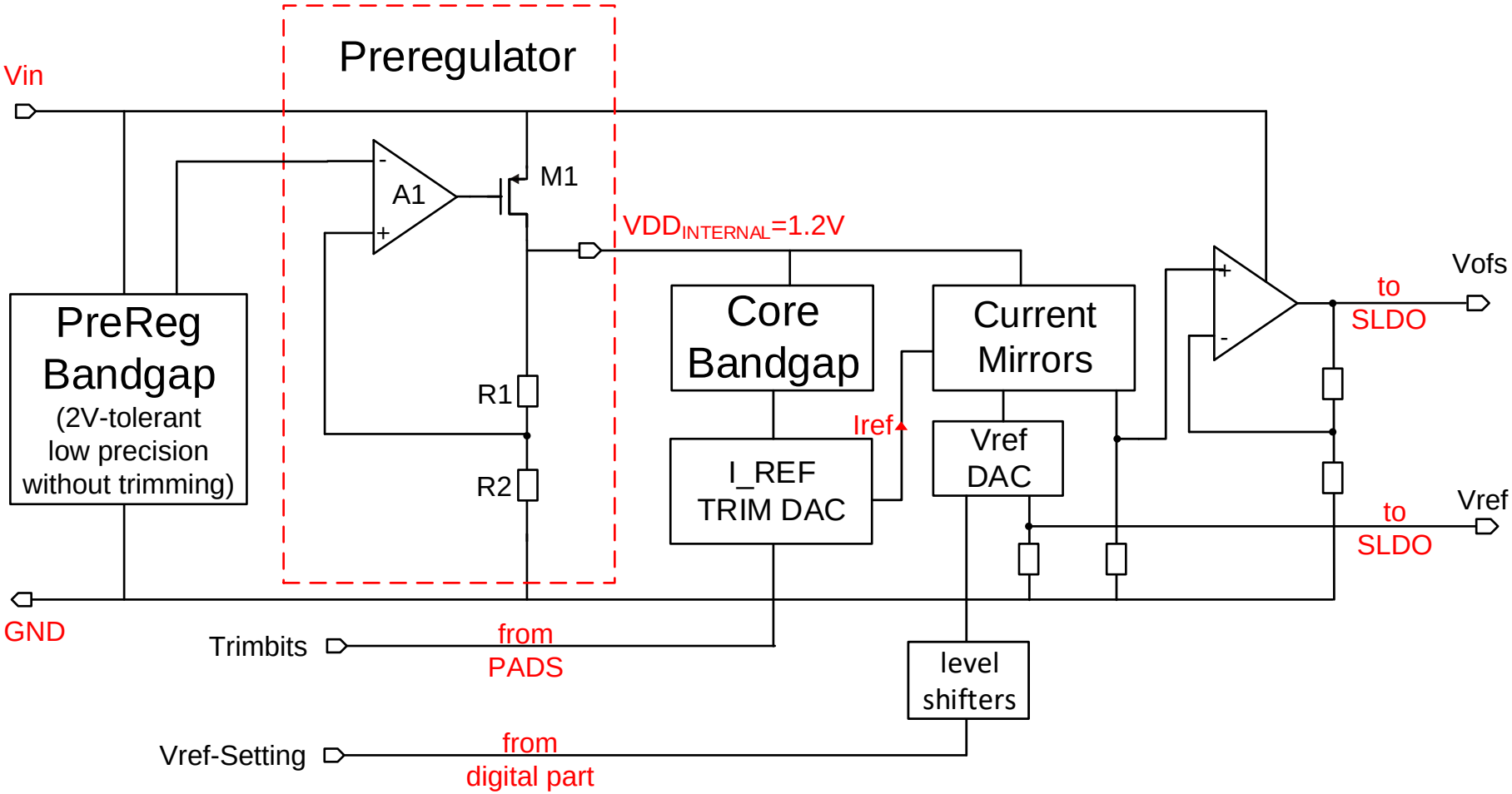
- 2 Shunt-LDO regulators (one analog, one digital) with 4 Power-Transistors each
  - **Input voltage**
    - There is actually only 1 input voltage both regulators have in common
  - **Output voltage**
    - 2 supply voltages → for each power domain 1 voltage
    - 8 voltages → for each Power-Transistor 1 voltage
  - **Supply current** (shunt+load) (0-200µA)
    - 2 currents→ for each power domain 1 current
    - 8 currents→ for each Power-Transistor 1 current
  - **Shunt current** (0-200µA)
    - 2 currents→ for each power domain 1 current
    - 8 currents→ for each Power-Transistor 1 current
  - **Reference Voltage**
    - 2 reference voltages → for each power domain 1 reference voltage
  - **Offset Voltages**
    - 2 reference voltages → for each power domain 1 reference voltage

RD53B_SLDO_Testchip_A
August 2018 Prototype

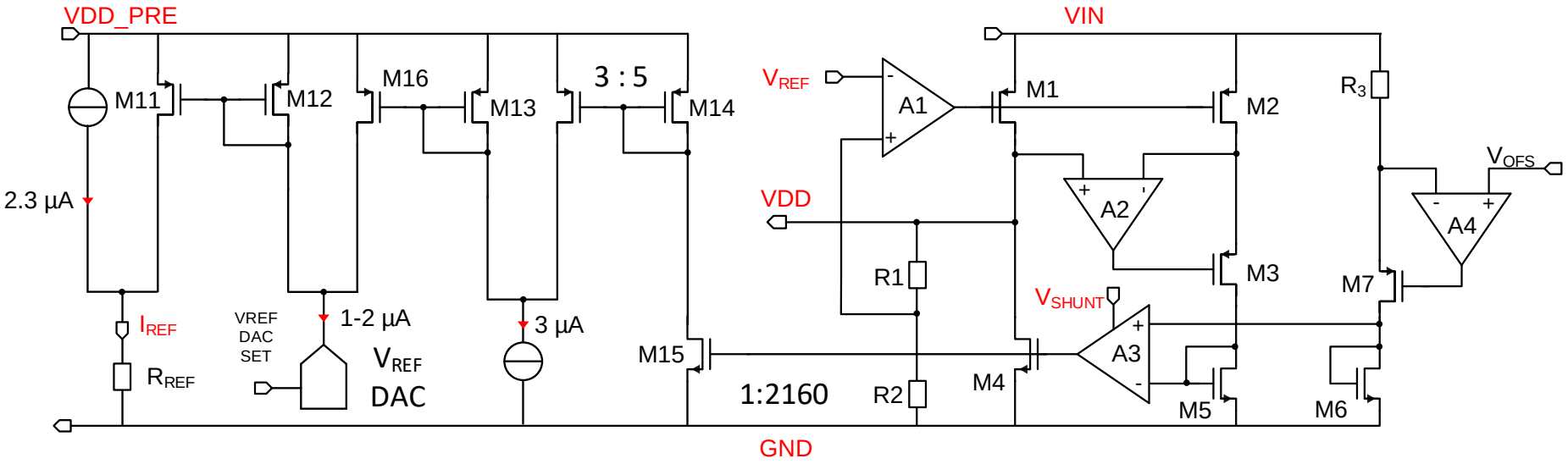


- New Features:
  - New Bandgap Scheme: 2V-bandgap, preregulator, core bandgap, iref generator
  - under-shunt current protection circuit
- Features not included:
  - startup circuit
  - external resistors in current reference generator
  - overvoltage protection
  - low power mode
- Special Notes:
  - internal resistor used for the current reference generator has been reported to be susceptible to radiation

New SLDO Biasing Scheme

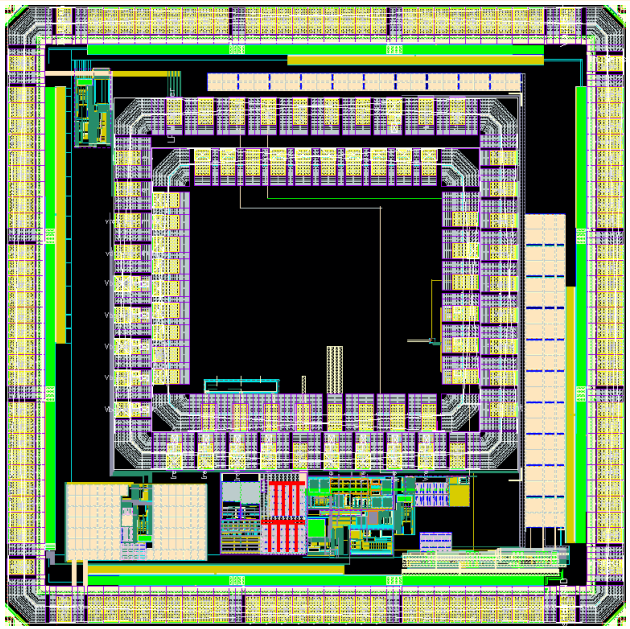


Under Shunt Protection



- overload current situation is considered as undershunt current scenario
  - high load current reduces shunt current
- In undershunt current case Vref is reduced
- minimum voltage defined by current source
  - Vmin=2.3µA x 150kOhm=350mV
- additional injected current (1-2µA) can be configured by DAC setting
- At shunt current lower < 11 mA addition current is disabled

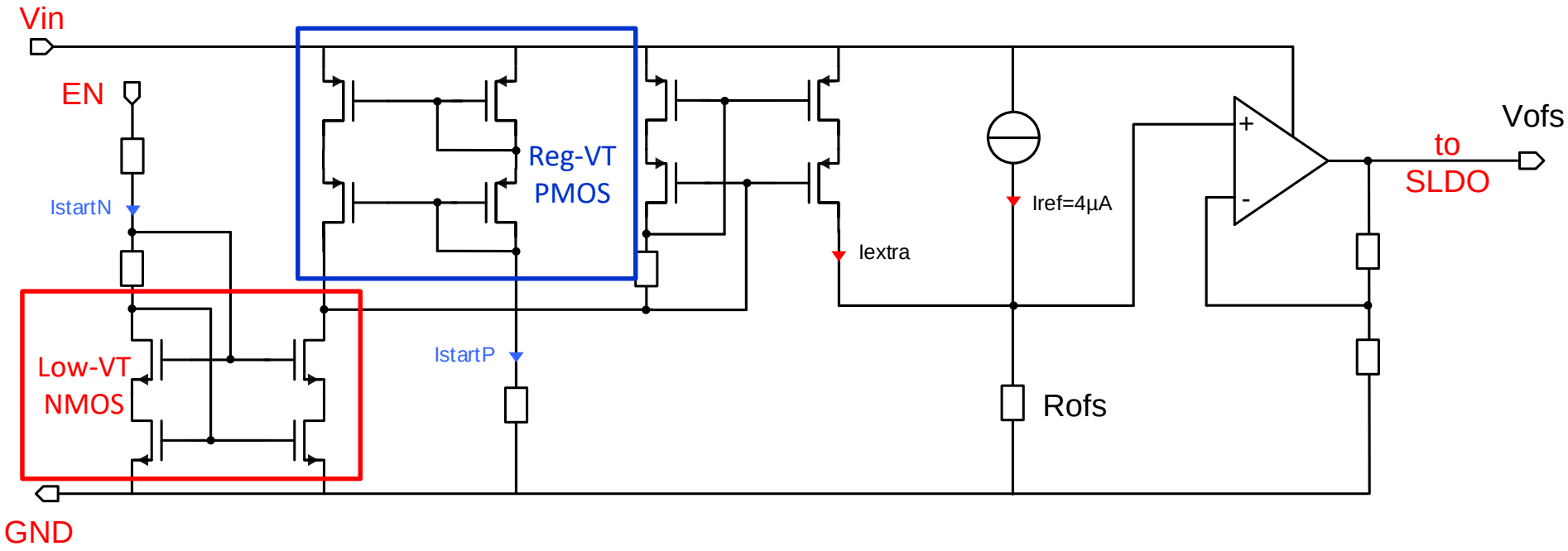
RD53B_SLDO_Testchip_B
November 2018 Prototype



- New Features
  - external resistor for reference current generator
  - startup circuit
  - switch for Rofs to choose between two Vofs values
  - AC coupled control signal for enabling low power mode
  - Alvaro control circuit for enabling low power mode
  - overvoltage protection circuit

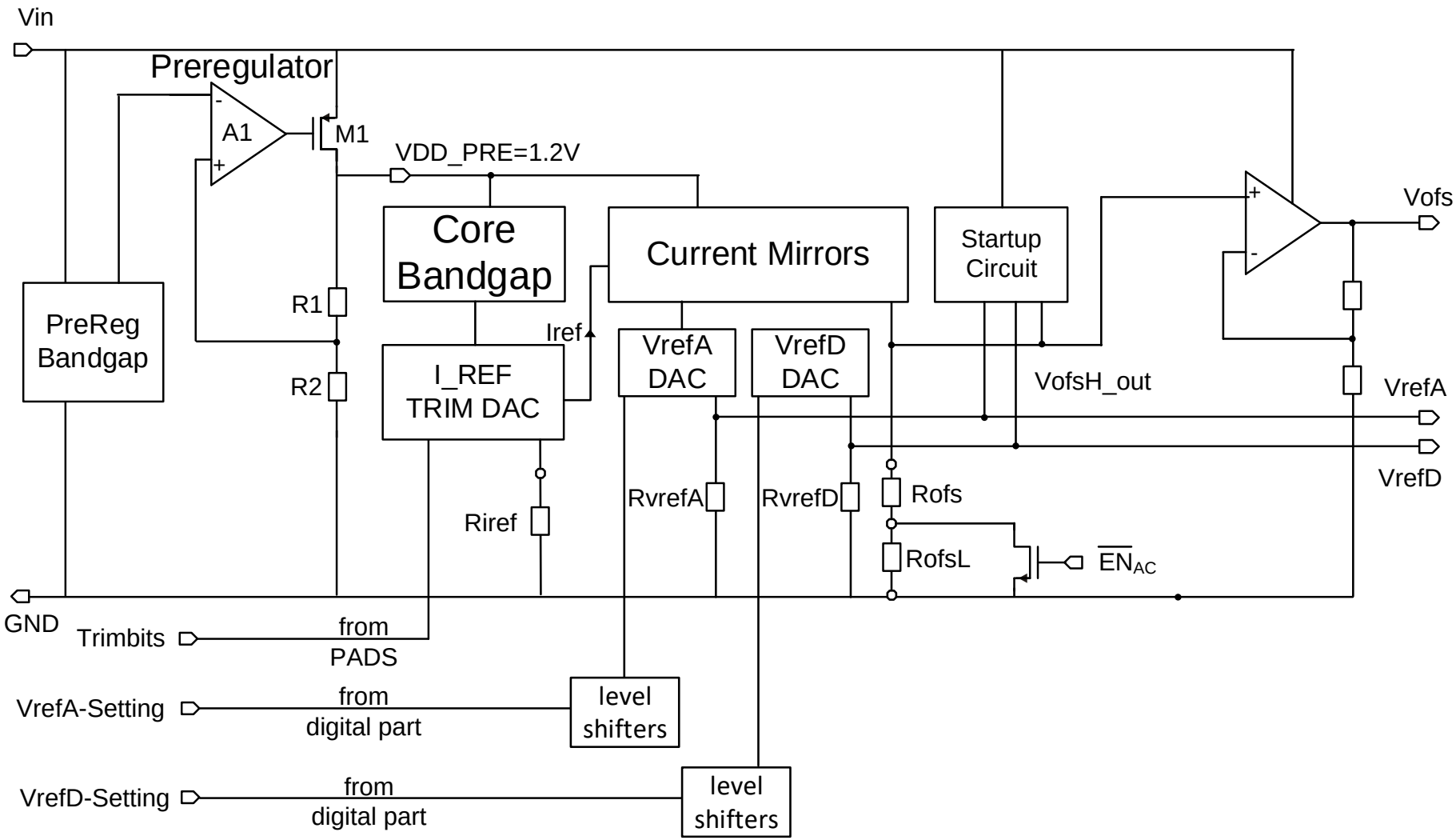
- Special Notes:
  - bandgaps have been reported to generate smaller than expected output voltages
  - startup circuit might be oscillating in some corners
  - Best test chip in terms of integrated features and performance

Vofs Startup Circuit

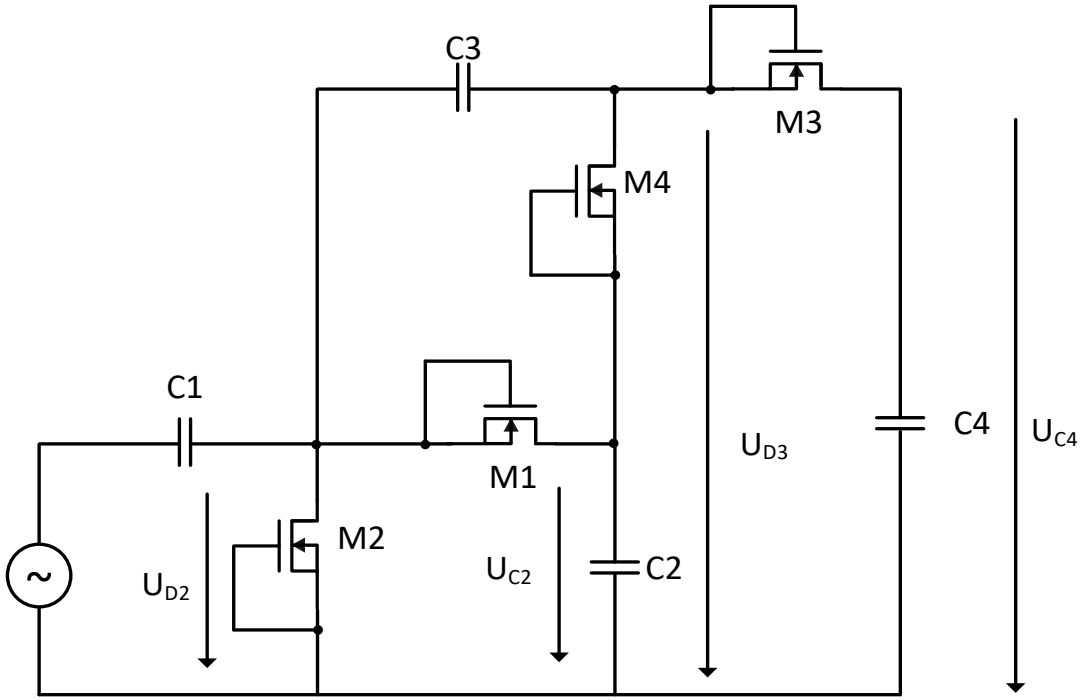


- wide-swing cascode current mirror with low-vt NMOS transistors draw current first
- standard cascode current mirror wit reg-vt PMOS transistors drain current later
  - difference between current is injected to R_{ofs}

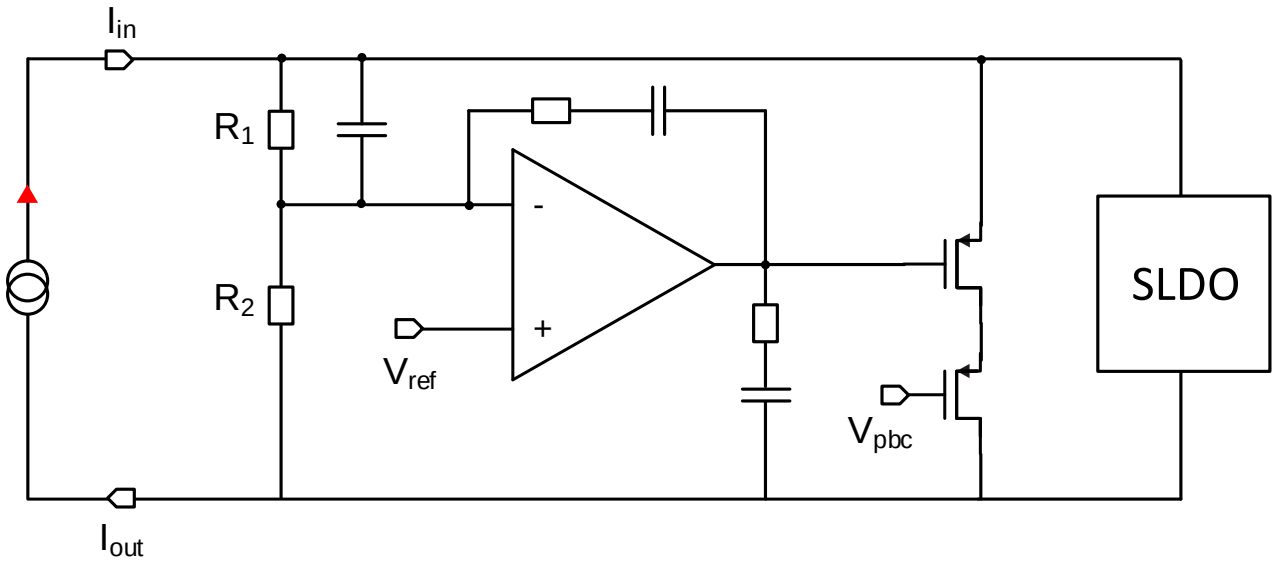
Bandgap Scheme with Configurable Vofs



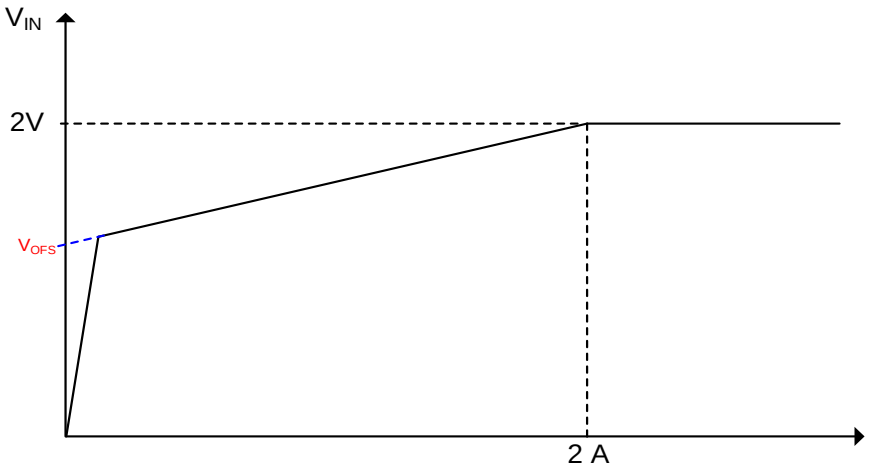
Voltage Doubling with Single External Capacitance



Overvoltage Protection Voltage Clamp



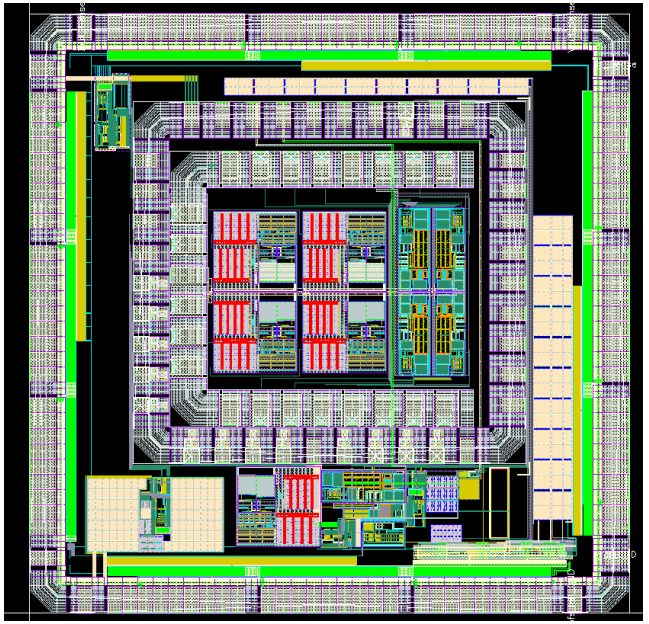
- voltage clamp implemented as shunt regualtor
- Operated in parallel to SLDO
- takes all excess current in case Vin =>2v



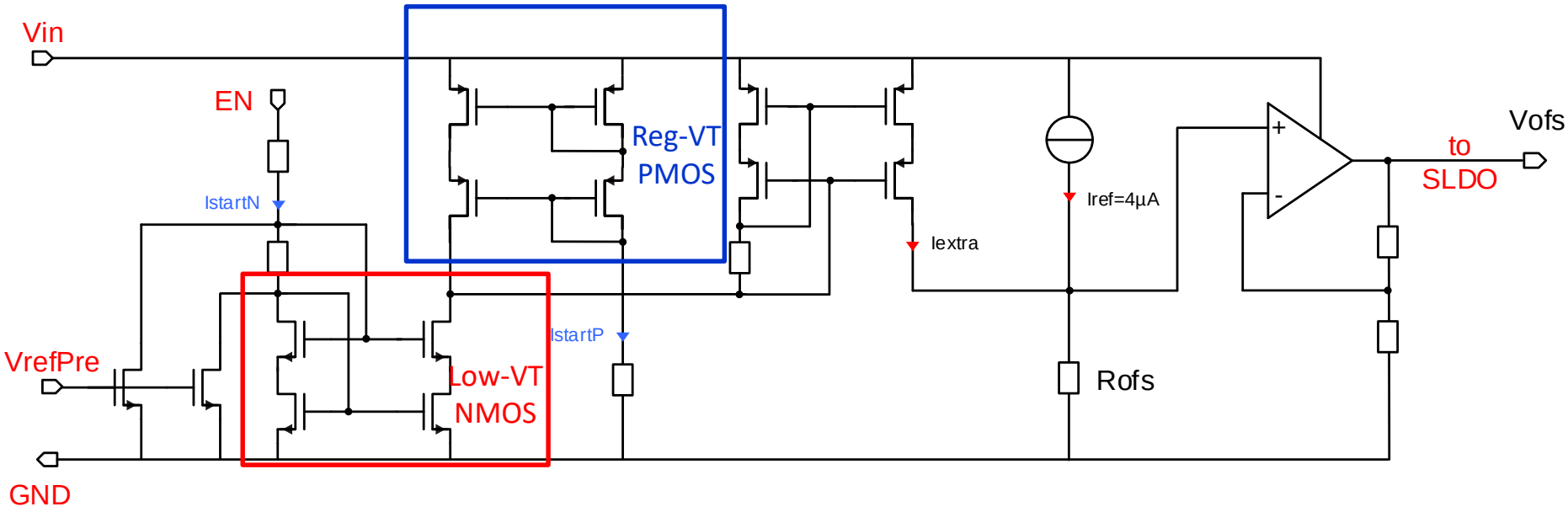
RD53B_SLDO_Testchip_C
Februar 2019 Prototype

- New Features:
  - „Improved“ startup circuit
  - modified preregulator with external capacitor
- Special Notes:
  - preregulator requires external capacitor

- Has a leaky capacitor connected to Vofs
  - strong temperature dependence of Vofs

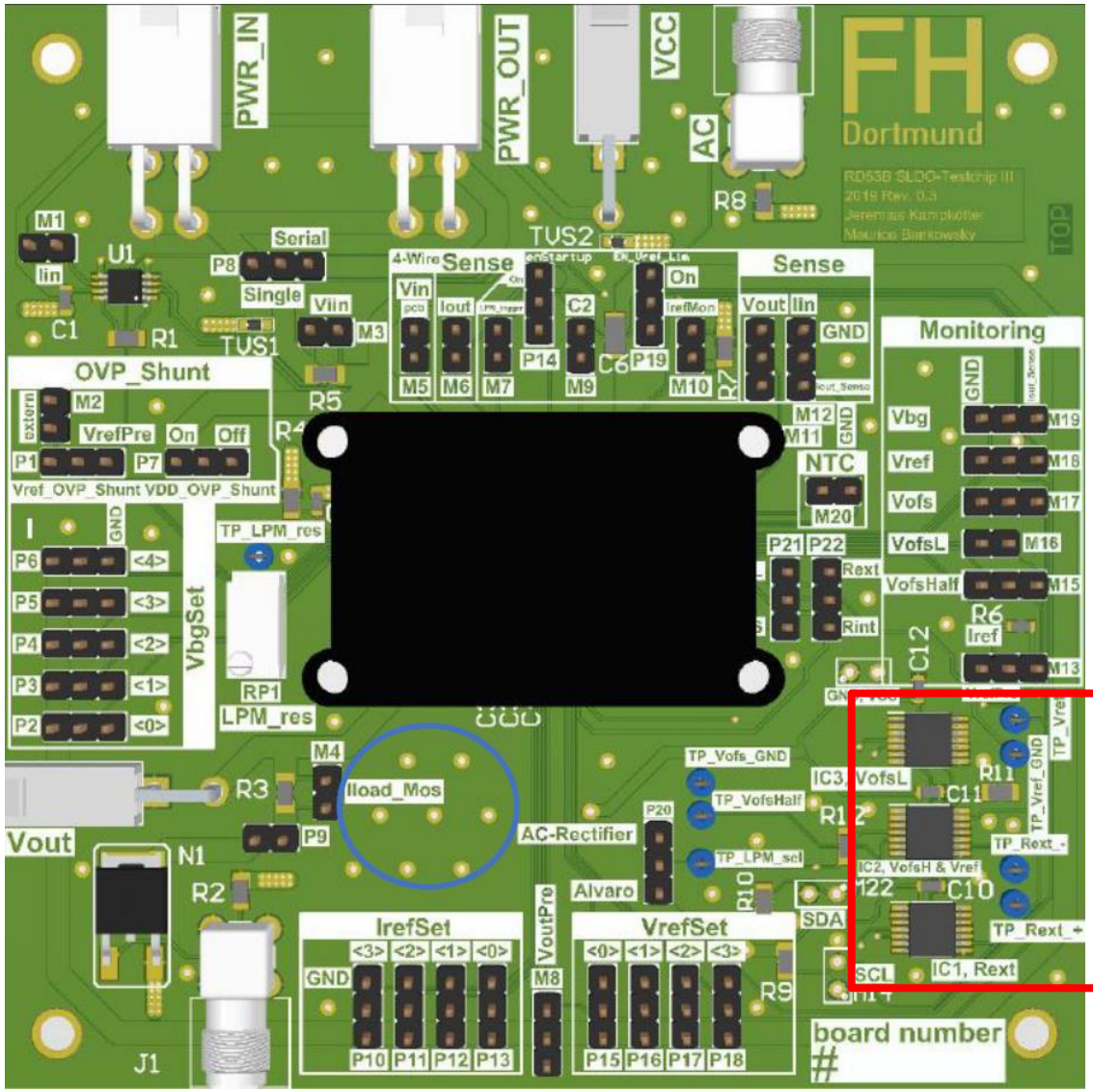


Startup Circuit



- wide-swing cascode current mirror with low-vt NMOS transistors draw current first
- standard cascode current mirror wit reg-vt PMOS transistrs drain current later
  - difference between current is injected to R_{ofs}
- startup-operation is interrupted as soon as pregulator bandgap switched-on

Testboard for SLDO Testchip Characterization

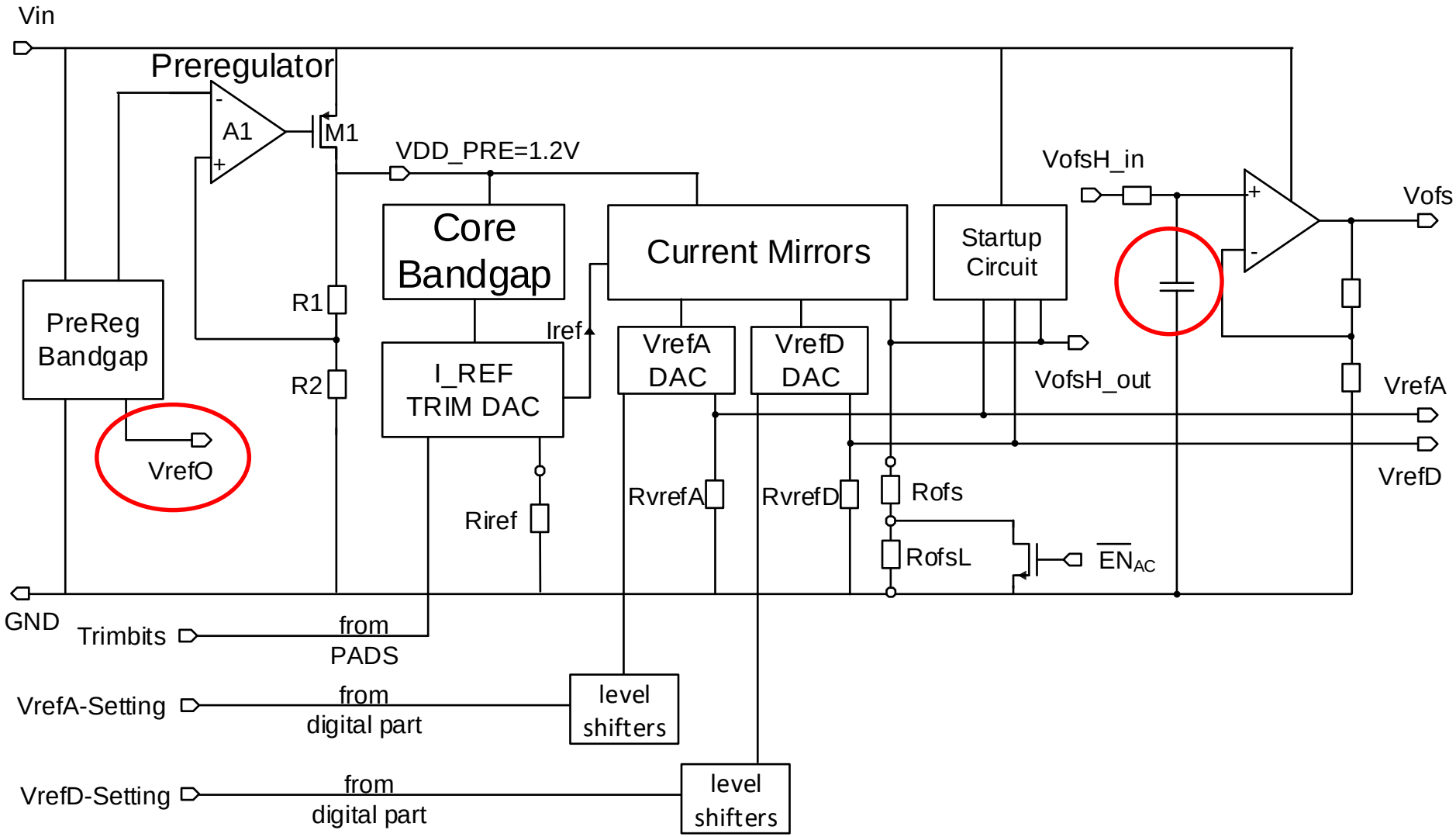


conventional potentiometer
replaced by digital potentiometer
controlled by I2C interface

RD53B Modifications ITKPIX 1 March 2022

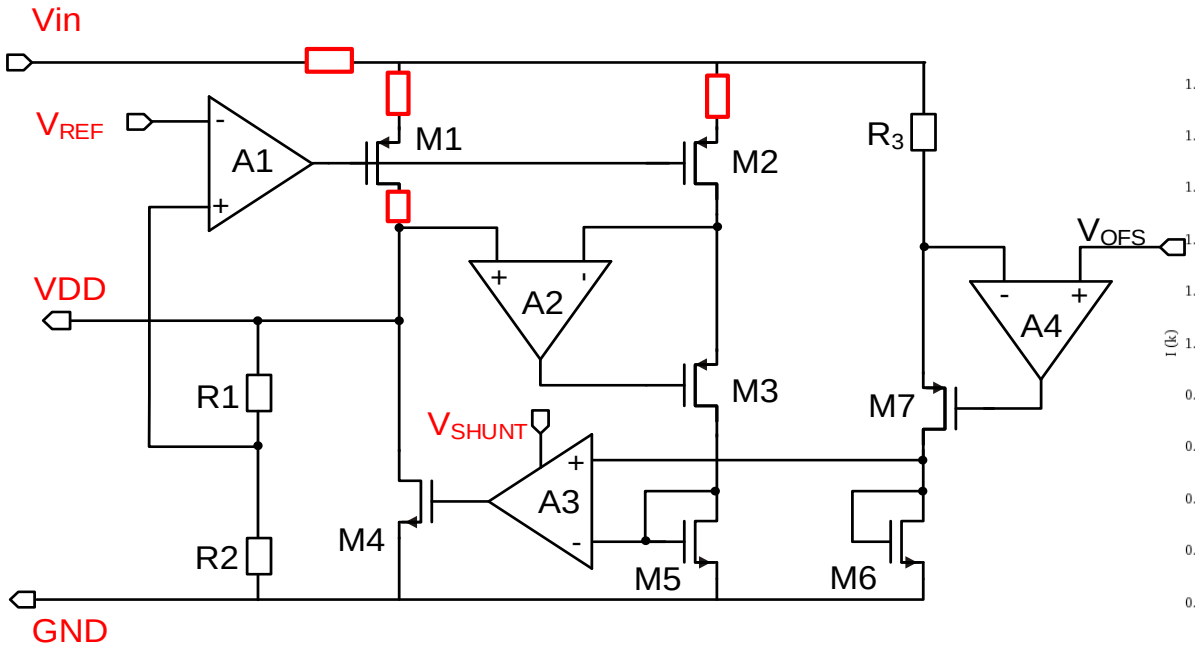
- Switch-Off OVP feature
  - Introduction of a replica of VrefPre (VrefO) for use with OVP as reference
- Shared Vofs feature
- Improvement of k-factor matching by layout modifcation in the pass transistor layout
- Startup circuit overvoltage migitation
- biasing circuit asymmetry between digital/analog SLDO lead to asymmetry startup behavior
  - OVP cascode power transistor got its own biasing circuit

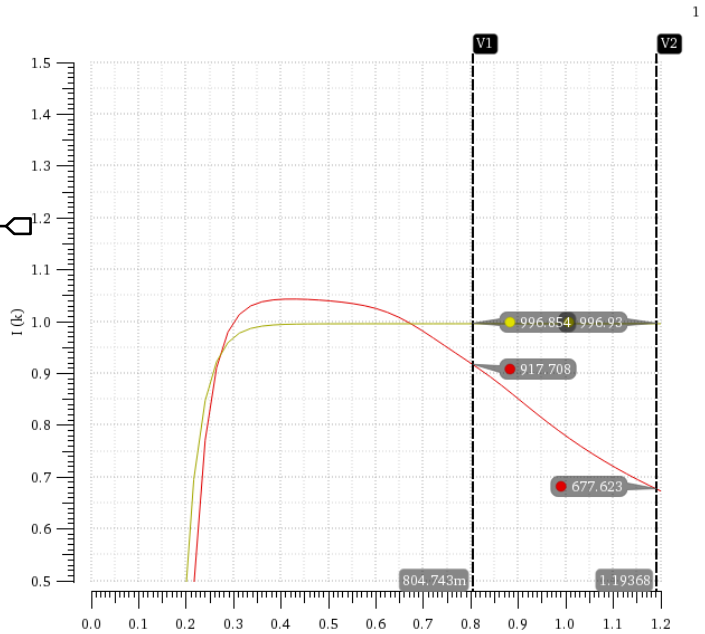
RD53B Bandgap Scheme



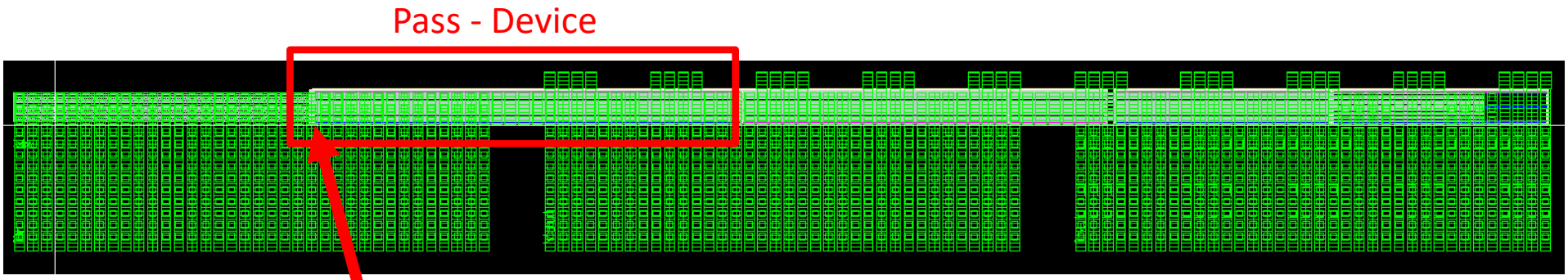
RD53B Modifications to Core Regulator Design

- new layout of the power transistors to reduce influence of parasitic resistors
  - measured input impedance (Vin slope) was larger than expected
  - parasitic resistors influenced M1/M2 current mirror ratio

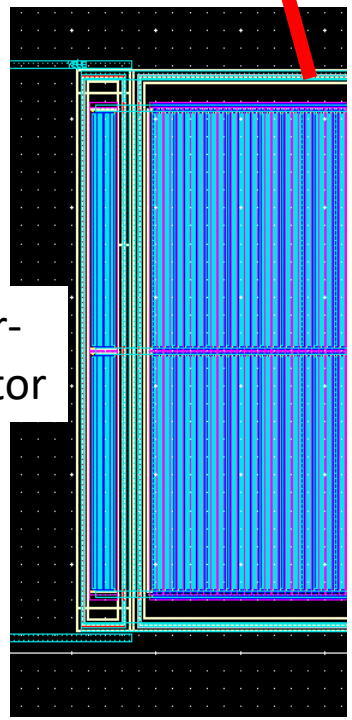




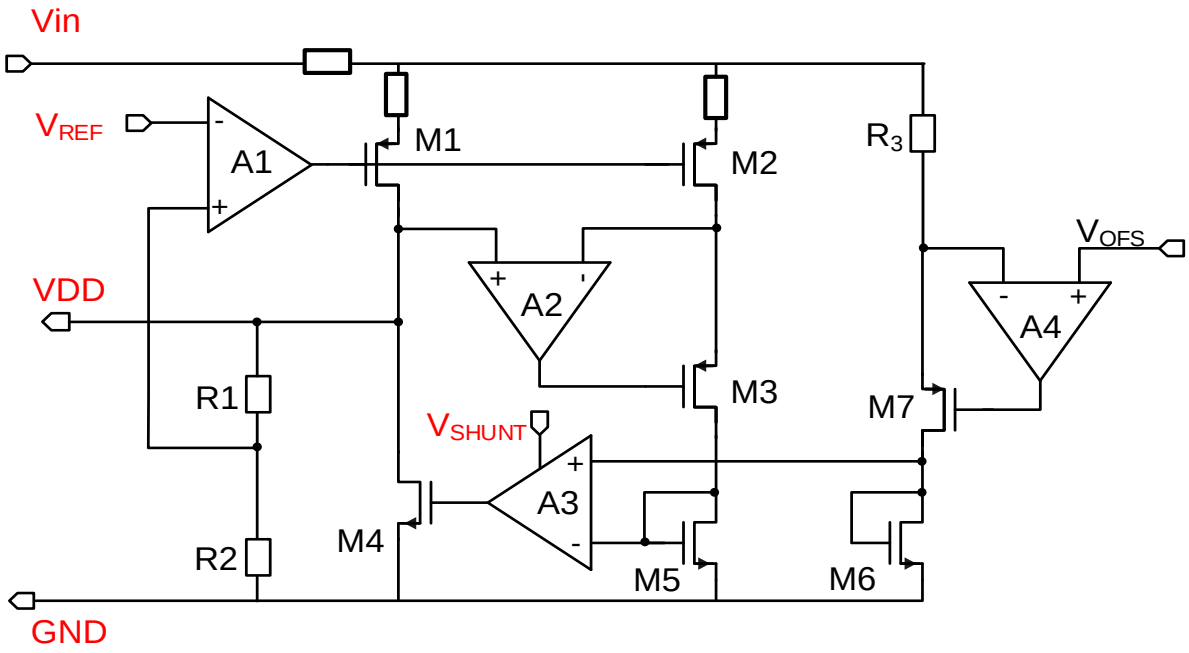
Layout of Power Transistor



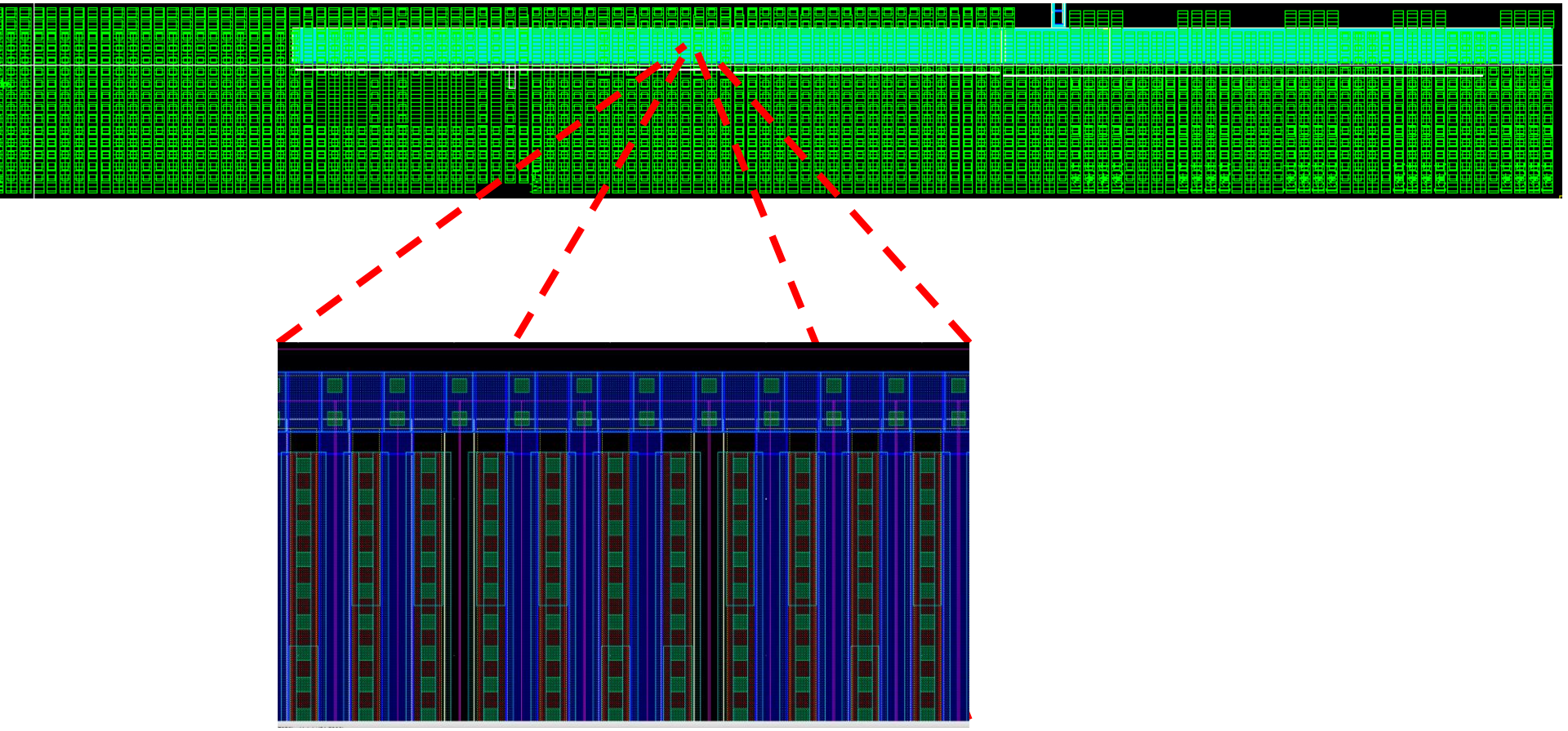
Mirror-Transistor



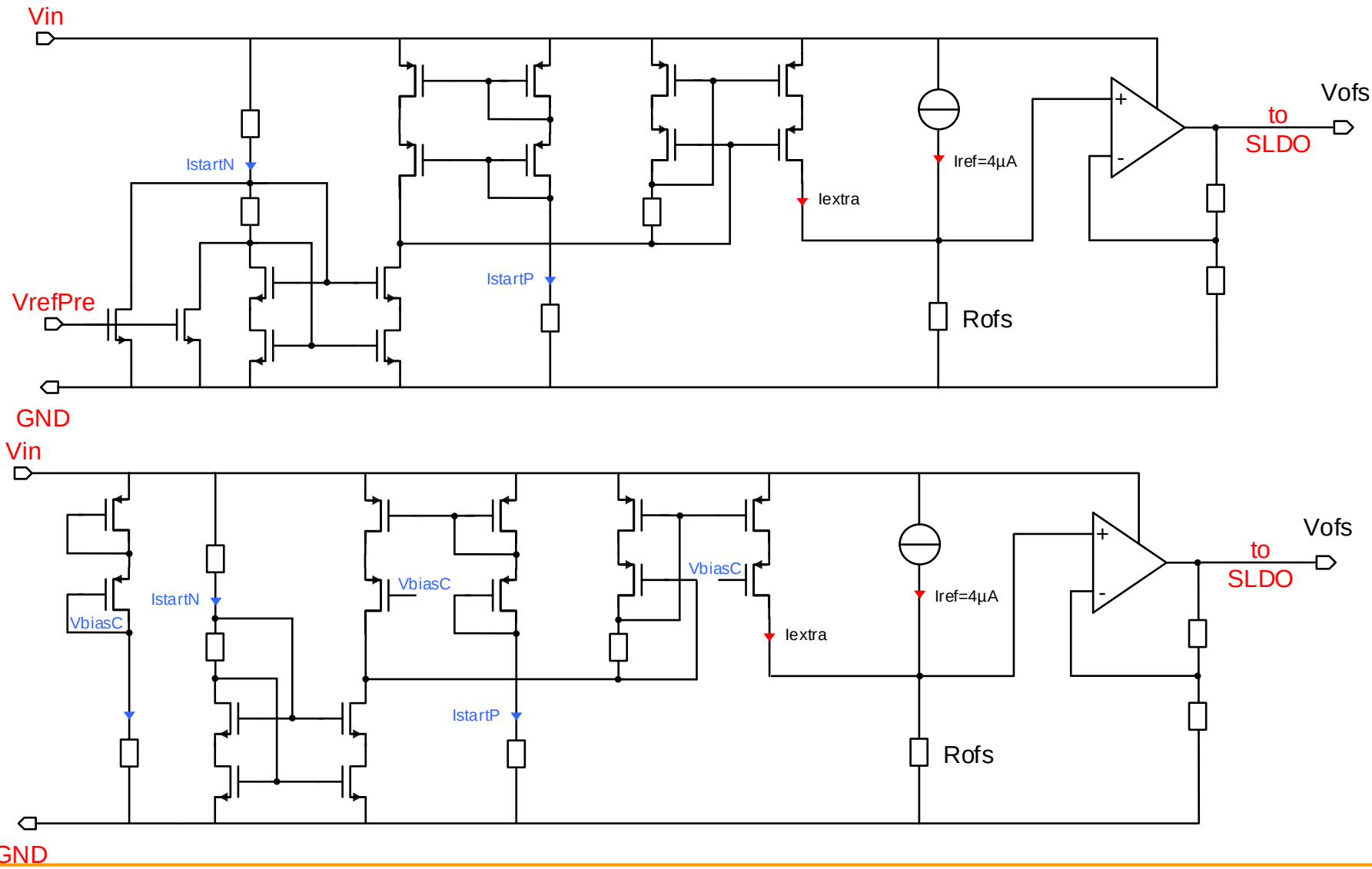
Pass-Device



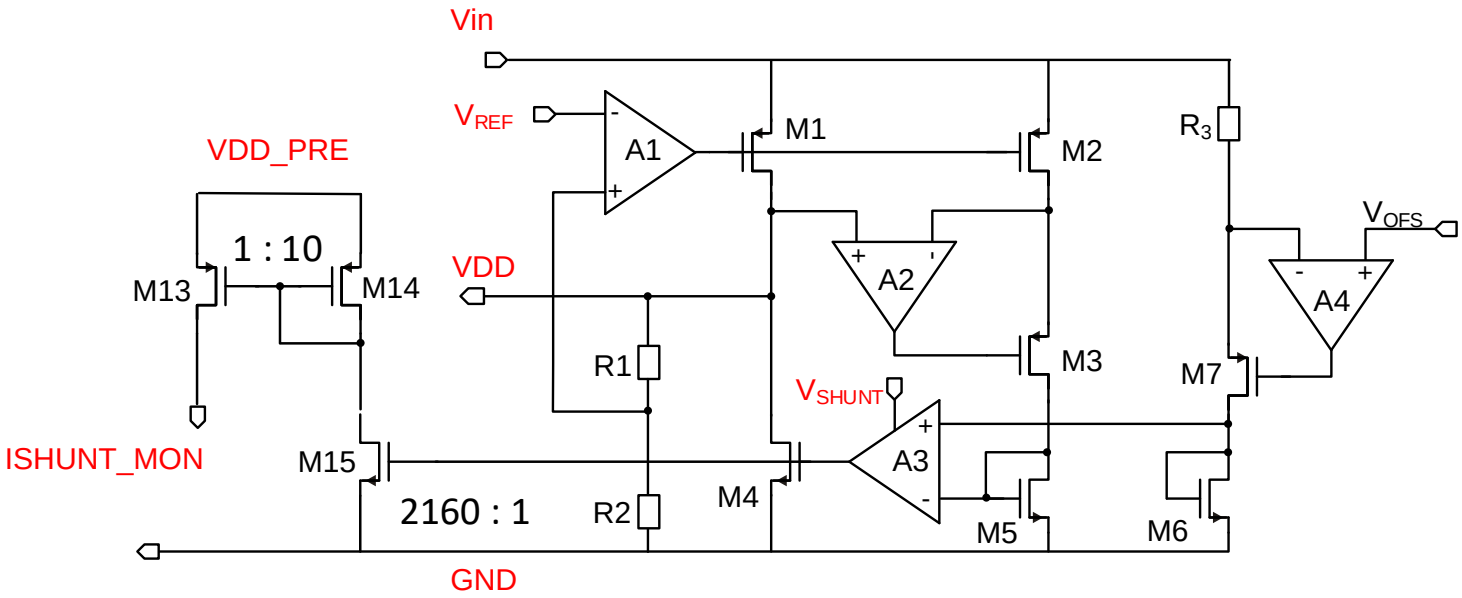
Layout Topology

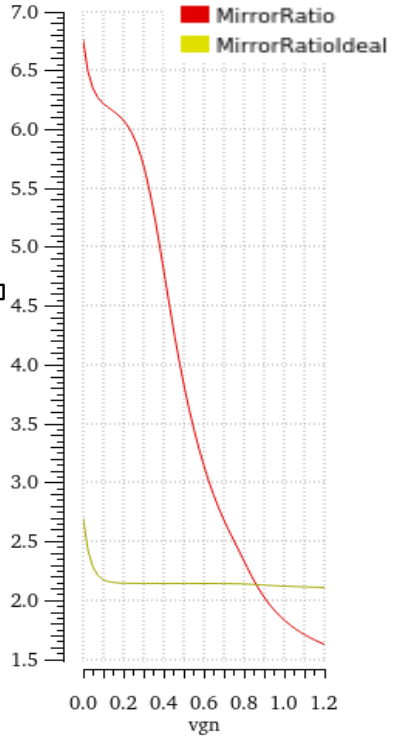


Modifications to Startup-Circuit



Shunt Current Monitoring Circuit



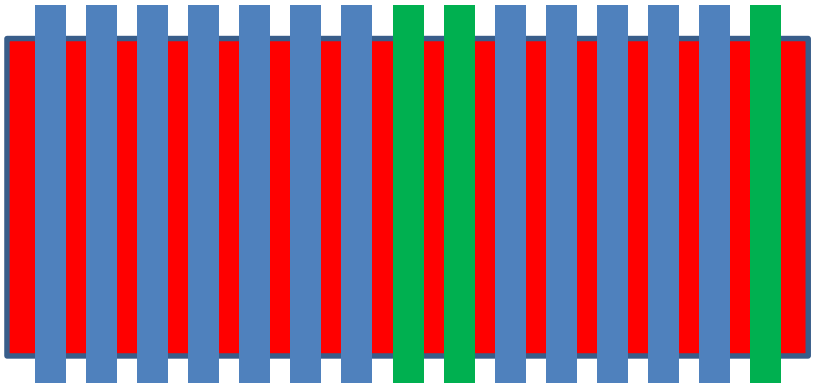


- A fraction of the shunt current is mirrored in a two-step current mirror configuration
- Strong dependence of current mirror ratio on operating point
  - in measurement and post layout simulation
  - not caused by parasitic resistances
  - STI stress identified as root cause

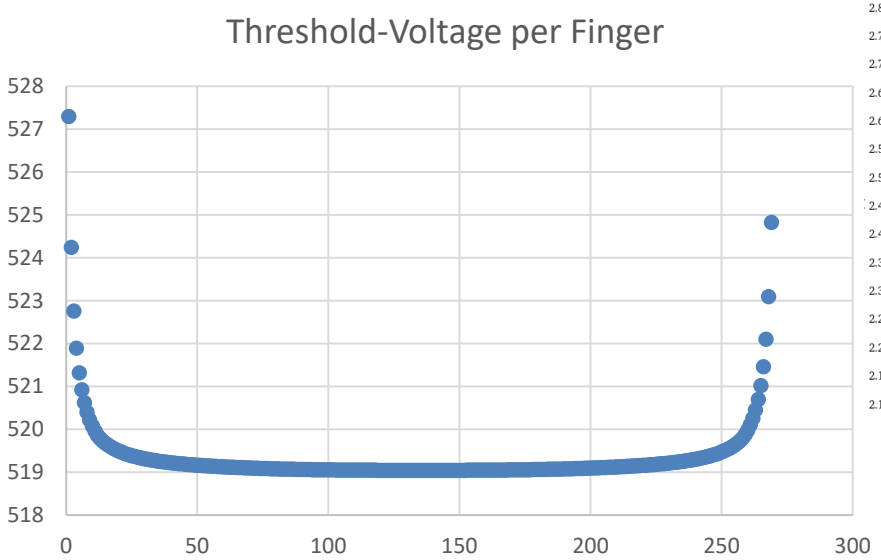
RD53B Modification for CROC May 2021

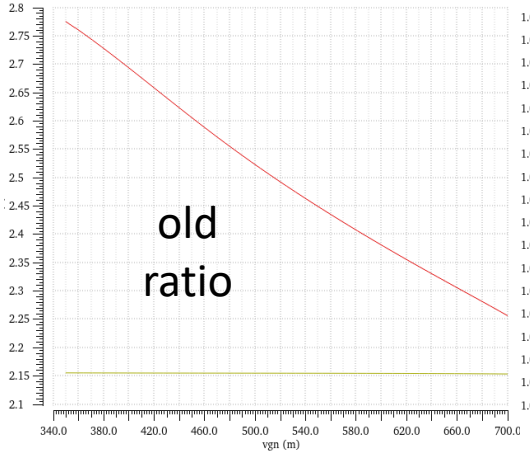
- Improve of shunt current sensing accuracy

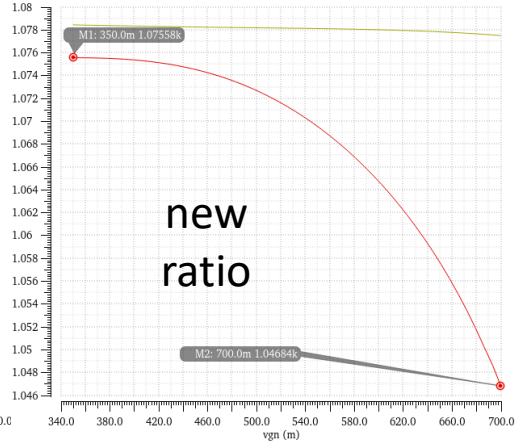
STI stress effect on power transistor



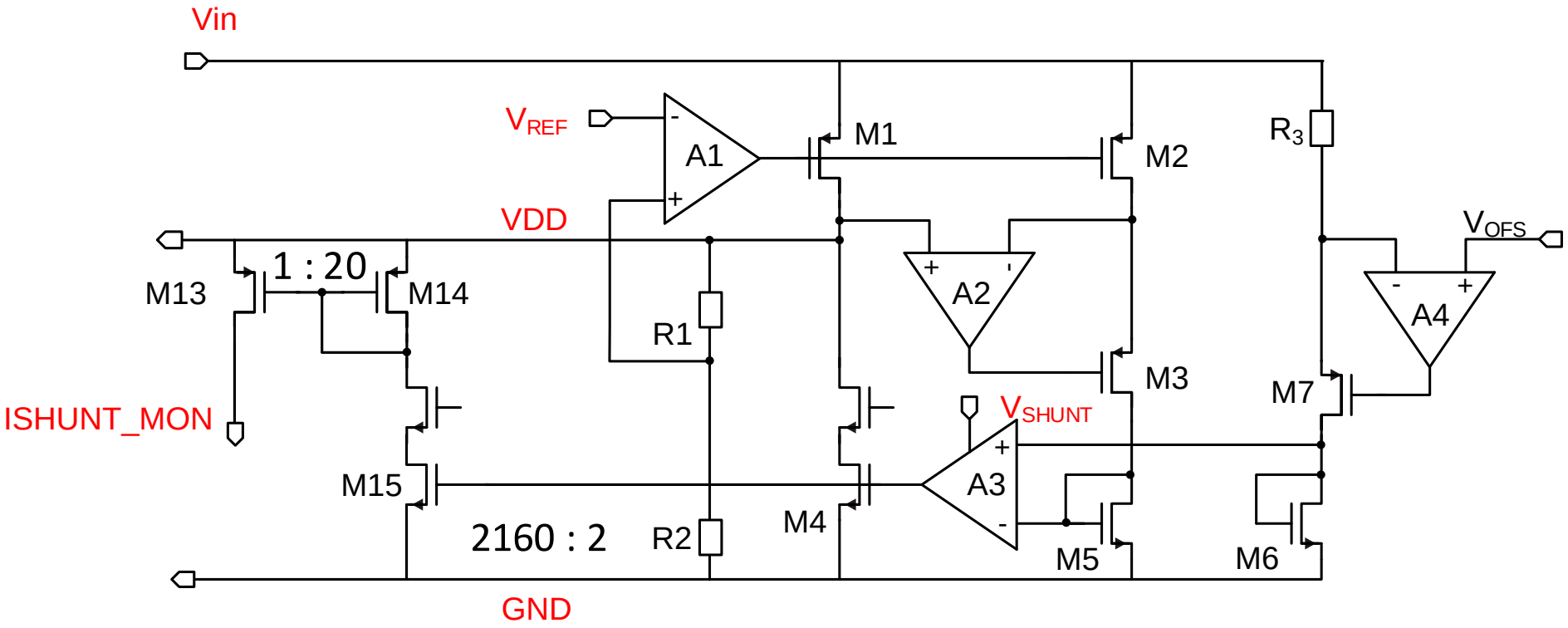
- Threshold of power transistor fingers depend on distance to the STI
- Shunt sense finger was put at the right edge
- Solution: 2 finger were put in the middle of the power transistor
- Additional dummies were add to the edges





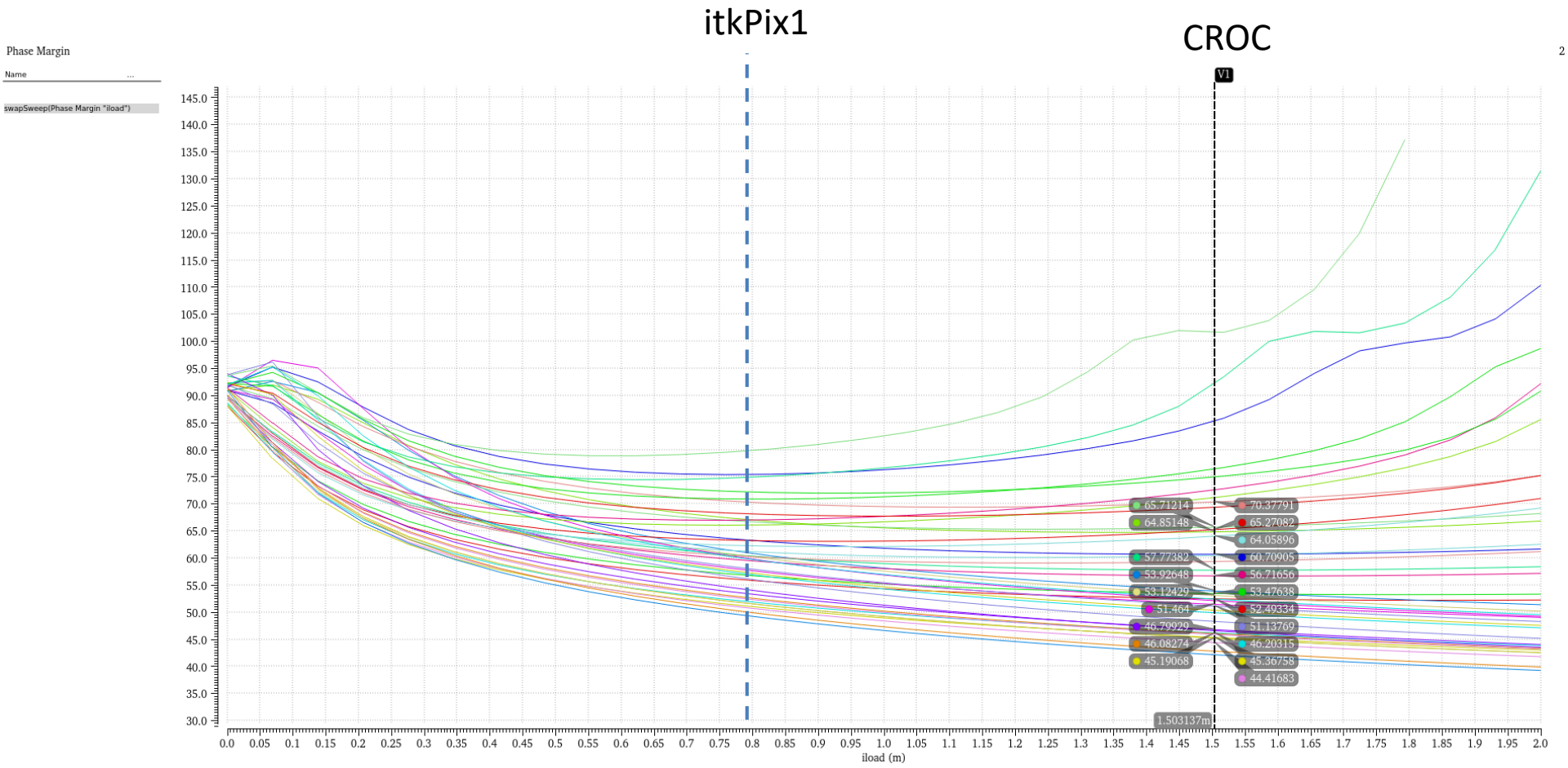


Drain Potential of the Cascode in the Shunt Sense Mirror



drain potential of cascode tranistor in shunt sense curent mirror varies
drain potenial of cascode transistor in the shunt path stays constant

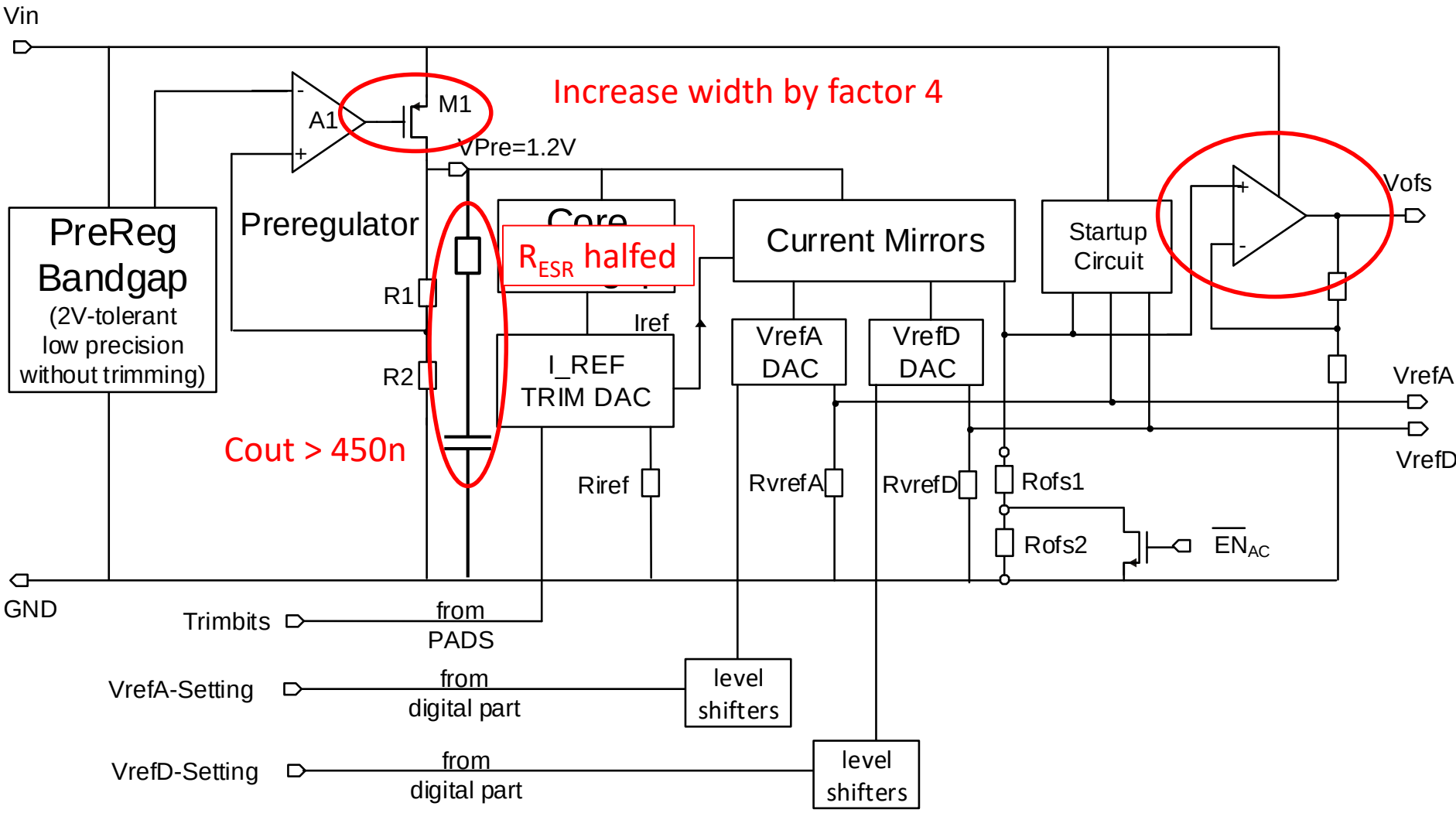
Pregulator Stability Affected by Additional load caused by undershunt current protection



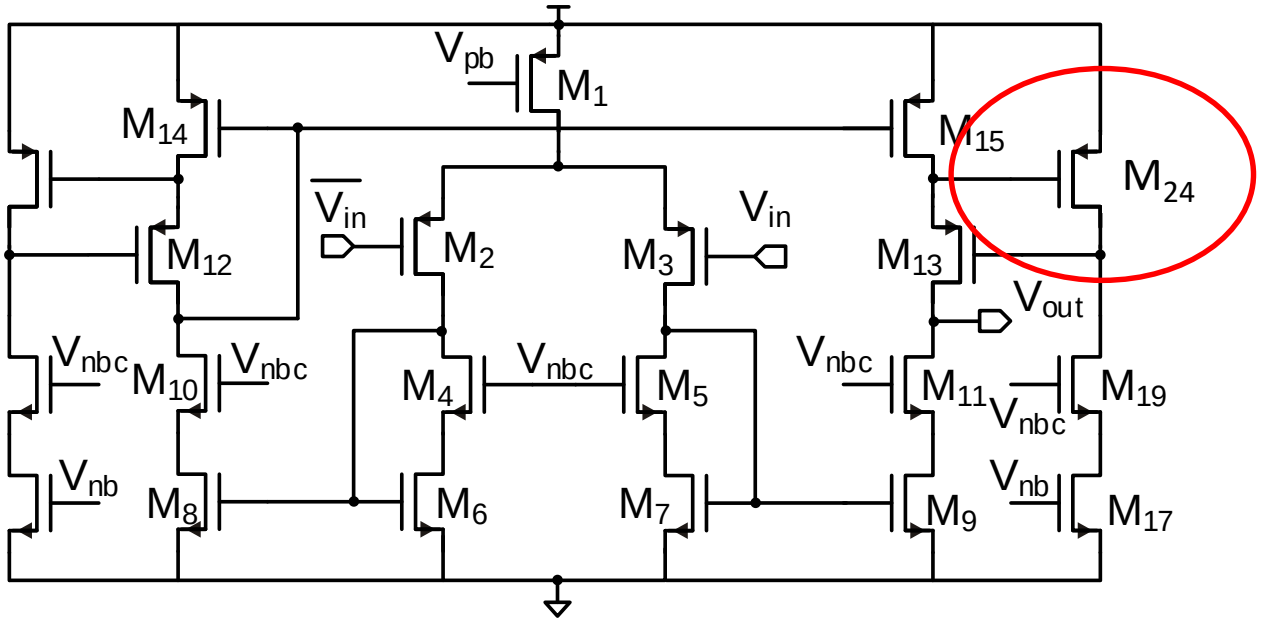
RD53C Modifications

- Redesign of the Preregulator to provide higher load current
- Migitatation of overvoltage in Vofs generation circuit for high Vofs
- Top level metal layout symmetry

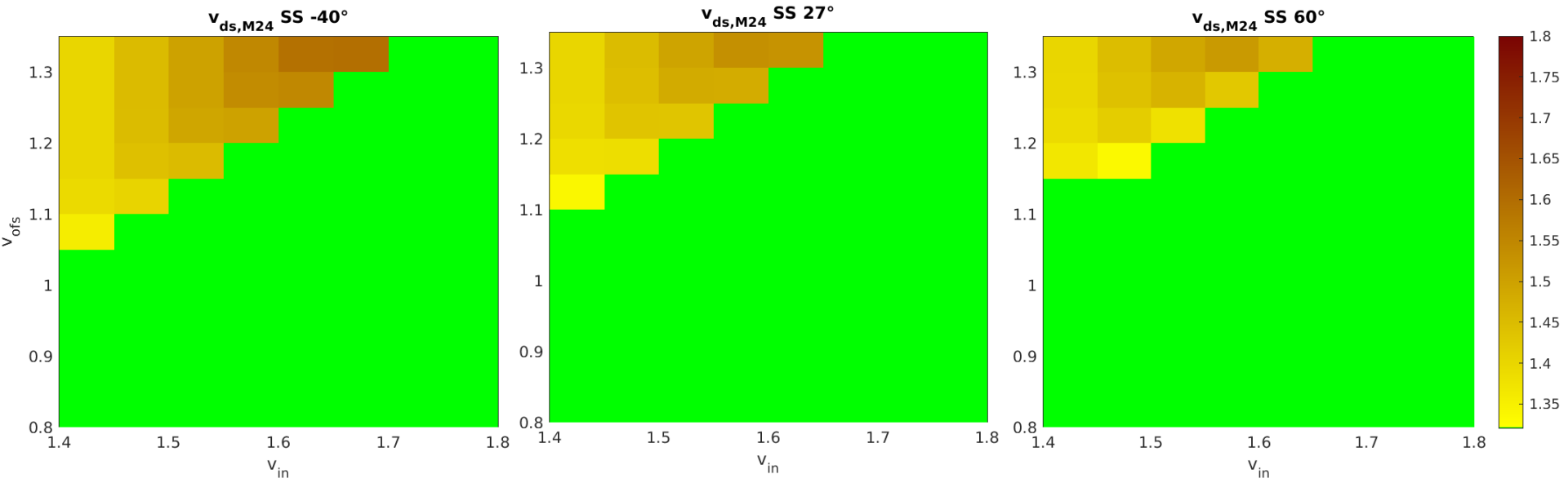
Preregulator Stabilization



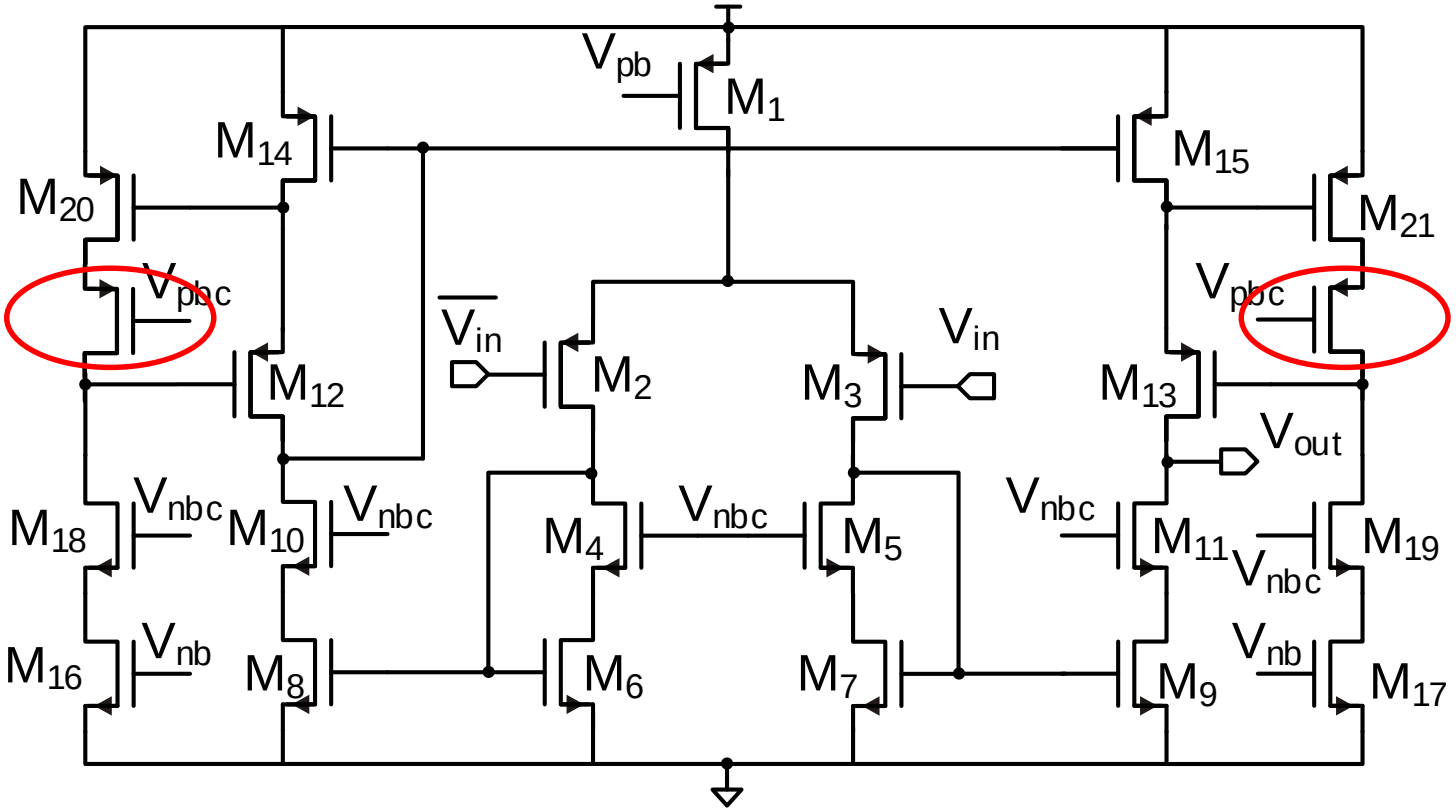
Vofs Amplifier Circuit



M24 V_{DS} Slow Corner



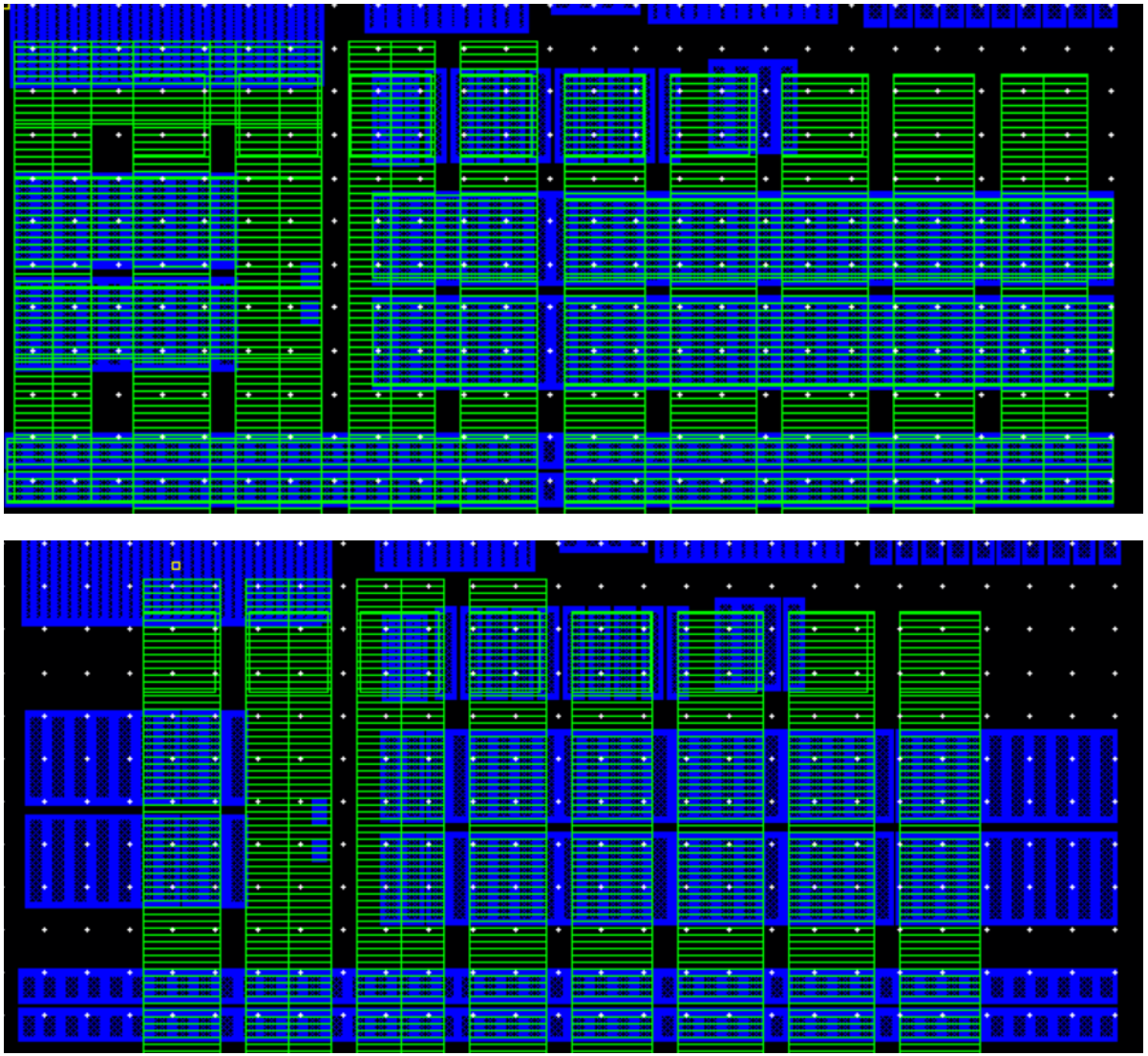
Design Improvement



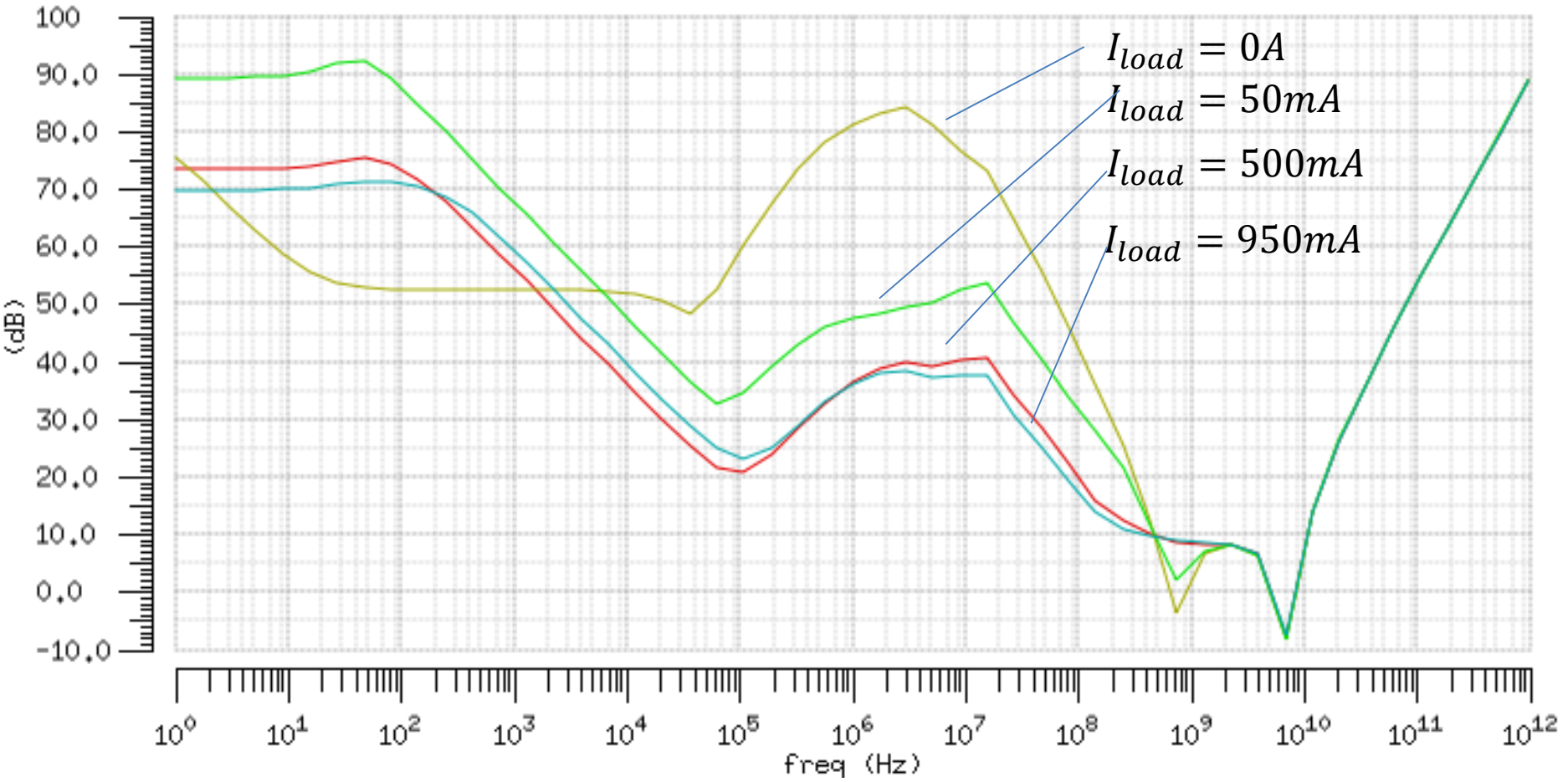
Simulation Result with Added Cascode Transistor

vin	iRefSet	Rofs	Vofs	temperature	toplevel.scs	Pass/Fail	VdsM24	VgsM24	VgdM24	VdsM4	VgsM4	VgdM4
1.55	9	33.75K	1.35	60	ff_lib	near	424.4m	167.2m	257.3m	3.255m	1.365	1.362
1.5	9	33.75K	1.35	60	ff_lib	near	459.9m	130.9m	329m	3.068m	1.362	1.359
1.55	5	33.75K	1.35	60	sf_lib	near	432.2m	177.7m	254.5m	3.461m	1.354	1.35
1.5	5	33.75K	1.35	60	sf_lib	near	470.6m	140.1m	330.5m	3.28m	1.353	1.35
1.55	5	33.75K	1.35	60	ss_lib	near	443.8m	194.6m	249.2m	3.648m	1.349	1.345
1.55	7	33.75K	1.35	60	tt_lib	near	422.4m	189.5m	233m	3.476m	1.347	1.344
1.45	9	33.75K	1.35	60	ff_lib	near	489.3m	100.7m	388.6m	2.825m	1.346	1.343
1.5	7	33.75K	1.35	60	tt_lib	near	462.9m	149.7m	313.3m	3.315m	1.346	1.342
1.6	5	33.75K	1.35	-40	ss_lib	near	404.5m	254.9m	149.6m	2.999m	1.344	1.341
1.6	9	33.75K	1.35	60	ff_lib	near	383.3m	208.3m	175m	3.426m	1.344	1.34
1.5	5	33.75K	1.35	60	ss_lib	near	485.1m	154m	331.1m	3.496m	1.344	1.34
1.65	5	33.75K	1.35	-40	ss_lib	near	356.7m	302.2m	54.53m	3.057m	1.343	1.34
1.55	5	33.75K	1.35	27	ss_lib	near	442.4m	204.4m	238.1m	3.449m	1.343	1.339
1.55	5	33.75K	1.35	-40	ss_lib	near	452m	208.4m	243.6m	2.933m	1.341	1.339
1.6	5	33.75K	1.35	60	ss_lib	near	398.8m	238.8m	159.9m	3.779m	1.341	1.337
1.6	5	33.75K	1.35	27	ss_lib	near	396.4m	249.7m	146.7m	3.547m	1.34	1.336
1.45	5	33.75K	1.35	60	sf_lib	near	503.1m	108.4m	394.7m	3.047m	1.339	1.335
1.55	9	33.75K	1.35	60	fs_lib	near	410.7m	202.2m	208.5m	3.451m	1.338	1.334
1.5	5	33.75K	1.35	27	ss_lib	near	485.8m	161.9m	323.9m	3.326m	1.337	1.334
1.55	5	33.75K	1.35	-40	sf_lib	near	414.2m	211.8m	202.4m	2.808m	1.337	1.334
1.5	5	33.75K	1.35	-40	ss_lib	near	497.9m	164m	333.9m	2.839m	1.336	1.333
1.5	9	33.75K	1.35	60	fs_lib	near	453.1m	160.3m	292.8m	3.311m	1.336	1.333
1.5	5	33.75K	1.35	27	sf_lib	near	456.3m	160.6m	295.7m	3.191m	1.335	1.332
1.6	5	33.75K	1.35	-40	sf_lib	near	367.3m	258m	109.3m	2.877m	1.334	1.331
1.55	7	33.75K	1.35	27	tt_lib	near	412.1m	207.8m	204.3m	3.323m	1.334	1.331
1.55	7	33.75K	1.35	27	tt_lib	near	412.1m	207.8m	204.3m	3.323m	1.334	1.331
1.55	5	33.75K	1.35	27	sf_lib	near	413.7m	202.3m	211.4m	3.324m	1.334	1.33
1.45	7	33.75K	1.35	60	tt_lib	near	497.7m	115.4m	382.2m	3.098m	1.333	1.33
1.5	5	33.75K	1.35	-40	sf_lib	near	459.9m	167.5m	292.3m	2.722m	1.332	1.329
1.5	7	33.75K	1.35	27	tt_lib	near	455.4m	165.2m	290.2m	3.201m	1.332	1.329
1.5	7	33.75K	1.35	27	tt_lib	near	455.4m	165.2m	290.2m	3.201m	1.332	1.329
1.6	7	33.75K	1.35	-40	tt_lib	near	367.9m	264.1m	103.8m	2.906m	1.332	1.329
1.55	7	33.75K	1.35	-40	tt_lib	near	415.1m	217.5m	197.6m	2.843m	1.332	1.329
1.45	5	33.75K	1.35	60	ss_lib	near	521m	118.9m	402.1m	3.281m	1.33	1.327
1.5	9	33.75K	1.35	27	ff_lib	near	431.5m	165.4m	266.2m	3.099m	1.328	1.325
1.5	7	33.75K	1.35	-40	tt_lib	near	461.3m	172.7m	288.6m	2.76m	1.327	1.324
1.55	9	33.75K	1.35	27	fs_lib	near	405m	217.4m	187.5m	3.301m	1.327	1.324
1.45	5	33.75K	1.35	-40	ss_lib	near	539.9m	123.5m	416.4m	2.687m	1.327	1.324
1.45	5	33.75K	1.35	27	ss_lib	near	524.4m	124.3m	400m	3.141m	1.325	1.322
1.45	9	33.75K	1.35	60	fs_lib	near	490.3m	123.5m	366.8m	3.114m	1.325	1.322
1.6	7	33.75K	1.35	60	tt_lib	near	377.6m	233.1m	144.5m	3.636m	1.326	1.322
1.6	5	33.75K	1.35	60	sf_lib	near	388.4m	219.7m	168.7m	3.645m	1.326	1.322
1.5	9	33.75K	1.35	27	fs_lib	near	449.3m	173.7m	275.6m	3.193m	1.325	1.322

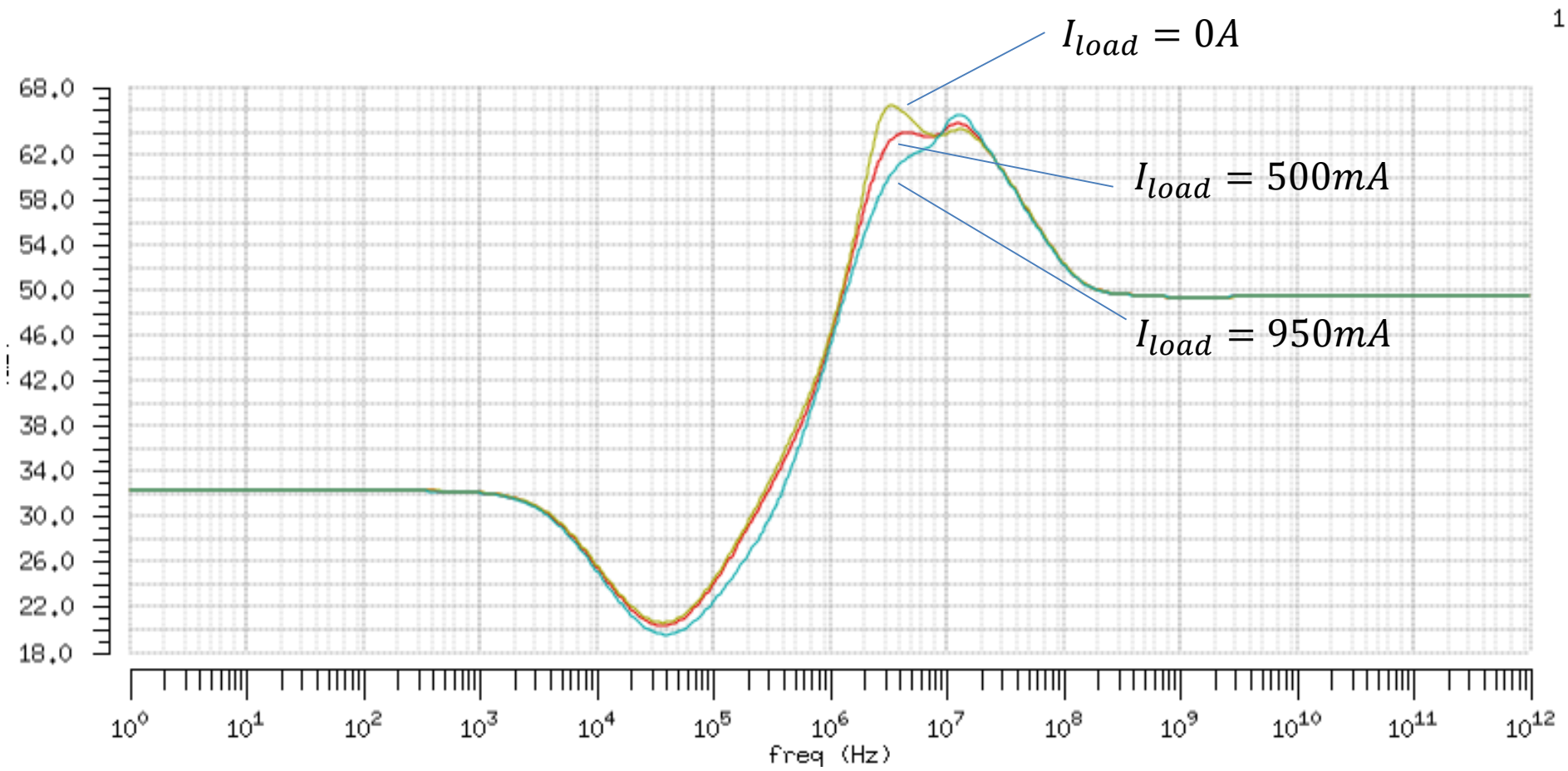
Thick Metal Dependency of Irradiation Results



PSRR Simulation LDO Mode



PSRR Simulation Shunt Mode



Conclusion

- SLDO has evolved a lot over the last 7 years
  - due to diligent effort of the collaboration members
  - 5 test chips and 3-5 big chip have been designed and characterized
- SLDO design has been adapted to new system specs
- Startup behavior has been improved
  - less bandgaps and new startup circuit introdued
- protection feature have been added
- low power mode introduced
- accuracy improved
  - input impedance (k-factor)
  - shunt sensing
  - top metal layout homogeneity