An Integrated Shunt-LDO Regulator for Serial Powered Systems

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***Abstract*—In this paper, a new type of regulator is proposed for integration in ASICs used in serially powered systems. In the serial powering scheme, modules are placed in series and fed by a constant current source to reduce the IR drop on the cables which increases powering efficiency. At the module level the needed supply voltages are generated redundantly out of the current supply by several parallel operating ASICs with integrated regulation circuitry. A Shunt-LDO regulator has been developed to allow robust and redundant regulator operation and the generation of different supply voltages by parallel placed devices. The Shunt-LDO regulator scheme combines the capability of Low Drop-Out regulators to generate a constant supply voltage with the feature of shunt regulators to assure a constant current flow through the device. The Shunt-LDO regulator has been developed for application in the framework of next generation hybrid pixel detectors used in high energy physics experiments. This circuit has been prototyped in a 130nm CMOS technology, capable of generating voltages in a range of 1.2-1.5V with a minimum drop out voltage of 200mV. The maximum shunt current is 500mA with a load regulation factor corresponding to an output impedance of 30mΩ.**

I. Introduction

The development of the Shunt-LDO regulator is motivated by the need to improve power efficiency of hybrid pixel detector systems used for particle tracking in high energy physics experiments. Current detectors like the hybrid pixel detector of the ATLAS experiment [1] in the Large Hadron Collider [2] consists of millions of channels grouped in modules. Because of the detectors size, the modules have to be powered by cables with limited cross-section and a length of up to 100m. Combined with a current consumption of 1-4A per module this gives rise to power losses in the cables which exceed the power consumption of the detector itself. Use of thicker cables is not possible because the detectors are already densely packed and additional material would increase the amount of unwanted interactions of particles with the inactive part of the detector, which in turn would highly degrade the detection performance.

A. Investigated powering schemes

Several powering schemes are investigated to increase powering efficiency. A well known approach is to distribute power at higher voltage which is then down converted close to the modules by switched DC-DC converters to the needed supply voltage value. Conventional buck converters make use of coils with ferrite core. These ferrite cores would be saturated by the 2-4 Tesla constant magnetic field which surrounds the detector. Air coils of same inductance tend to be much bigger in size which is incompatible with the need to reduce the amount of material used in the detector. Calculations and prototype studies concerning switched capacitor based converter have shown that for high current applications like in the case of hybrid pixel detectors, no improvement in material budget is achieved when powering efficiency of 70% is targeted [3]. In addition, the ripples on the supply voltage that come along with switched power supplies influence the noise performance of commonly used readout circuits which are designed with single ended input because of the single-ended nature of the sensor signal and as a result have bad PSRR. LDO regulator could be used to filter the ripples on the supply voltage but they would add additional power losses on top of the losses which are already related to the DC-DC converter itself and thus would decrease the overall powering efficiency.

B. A special powering approach for a special environment

An alternative but rather uncommon approach is serial powering [4]. In a serial powered scheme, modules are placed in series and powered by a constant current source. Shunt regulators are used at module level to generate the supply voltage out of the current supply. In a scheme with n modules connected in series, the current through the cable is reduced by a factor n with respect to the parallel powering of n modules whereas the voltage drop across the module chain corresponds to n times the voltage drop across a single module. Neglecting the inefficiency caused by the regulation circuitry, the improvement in powering efficiency can be calculated to be [5]:

$$\frac{1+\frac{nRI}{V}}{1+\frac{RI}{Vn}} \tag{1}$$

where n is the amount of powered modules, R is the cable resistance, I is the current drawn and V is the voltage across a module.

When modules are powered serially, a potential hazard that has to be avoided is the break of the supply chain. Dedicated circuitry is hence needed to bypass a broken module. In addition, redundancy of the regulation circuitry increases the system reliability. Therefore a regulation scheme is required where the devices are capable to operate in parallel at module level and to shunt additional current in case of a device failure. Furthermore, a lower supply voltage is very often applied to the digital part of the readout ASIC with respect to the analog part, to reduce the current consumption of the digital circuitry. Hence parallel operating regulators that generate different supply voltages out of the single current supply are very beneficial for this powering scheme and reduce the implementation effort.

II. First Implementation of Serial Powering

To meet the requirements mentioned in the previous section, the regulation architecture shown in Fig. 1 has been chosen to study serial powering with the FE-I3 hybrid pixel readout chip [4]. A shunt regulator generates a constant supply voltage from the input current which is used to supply the analog part of the readout chip. All the current which is not drawn by the load is shunted by transistor M1 which assures a constant current flow to the next module in the chain. A LDO regulator is connected to the voltage output of the shunt regulator and is used to generate the lower digital supply voltage.

To provide redundancy, the regulation circuitry shown in Fig. 1 is integrated in all 16 FE-I3 hybrid pixel readout chip which are

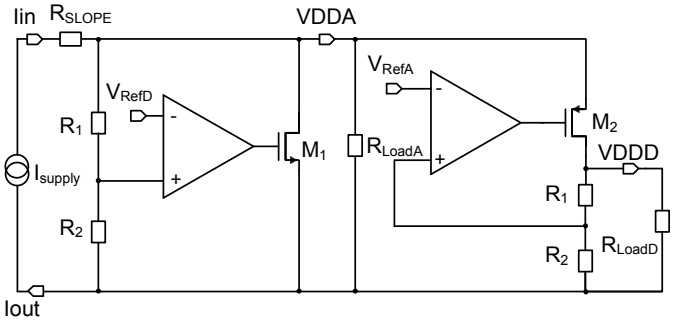

Fig. 1: Regulation scheme of the FE-I3 ATLAS hybrid pixel readout chip. VDDA is the analog and VDDD the digital supply voltage

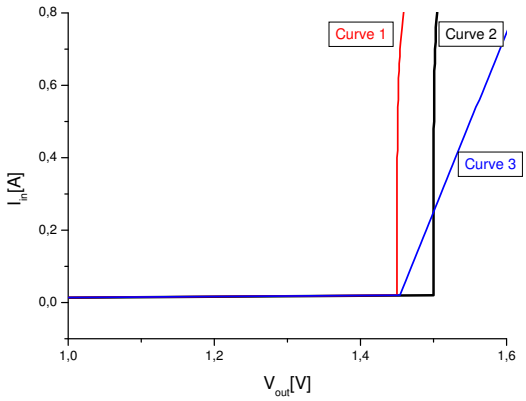

Fig. 2: Shunt regulator I-V characteristics with (3) and without (1 & 2) series resistor

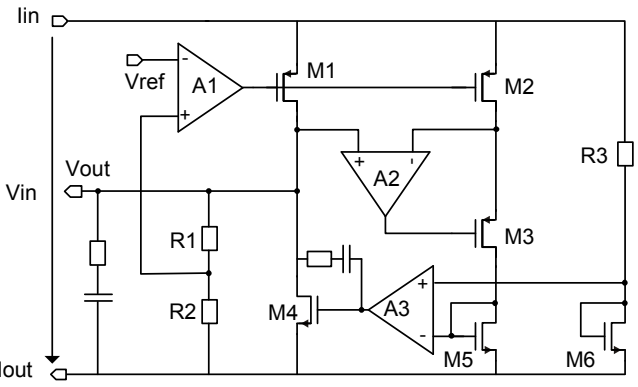

Fig. 3: LDO regulator with shunt capability (ShuLDO)

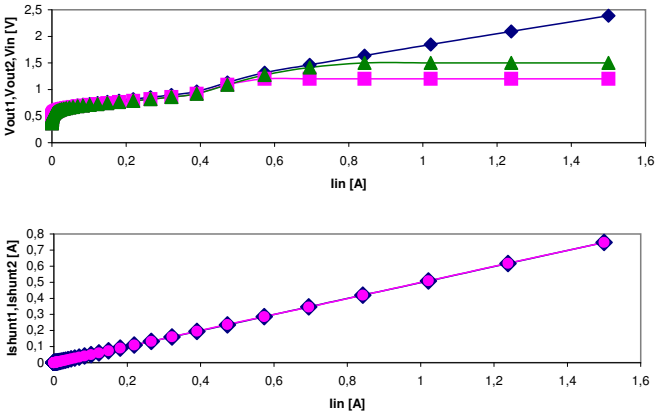

Fig. 4: Simulation result of parallel operation of two Shunt-LDO regulators

placed on a single module and operate in parallel. A critical problem with the parallel operation of shunt regulators is caused by mismatch and process variations. The I-V characteristic of shunt regulators is very steep as is illustrated in Fig. 2. If now, due to mismatch and process variation, different output voltages are generated by the parallel placed regulators (curve 1 & 2 in Fig. 2), most of the shunt current will flow through the regulator generating the smallest output voltage, which will cause a non-uniform distribution of power dissipation on the module and might lead to device break-down.

To solve this problem, the series resistor R_{Slope} shown in Fig. 1 has been placed at the input of each shunt regulator, which smoothens out the I-V characteristic (curve 3 in Fig. 2) and helps distributing the shunt current on the parallel placed regulators. In this scheme, the added resistor R_{Slope} is mandatory for safe operation but the resistor itself does not contribute to the regulation performance and the voltage drop across the resistor is causing additional power dissipation which lowers the efficiency. Furthermore this scheme is not very flexible: Although the series resistor allows for some voltage mismatch, the output voltages generated by the parallel operating shunt regulators cannot be chosen independently. In addition, it has to be decided during the design phase which part of the ASIC is powered by the shunt regulator output and which is powered by the LDO regulator because the output voltage of the shunt regulator is always higher than the LDO regulator output voltage I_{out}.

III. Functional Principle of the Shunt-LDO Regulator

The basic idea that initiated the development of the Shunt-LDO regulator is to flip the order of the regulator chain in Fig 1. The LDO regulator should be placed first so that the power PMOS transistor M2 replaces the series resistor R_{slope}. The shunt transistor M1 which is used to shunt the current that is not drawn by the load, should become part of the load of the LDO regulator. For a working implementation, a method is needed to sense the current flowing through the regulator and to steer the amount of current that has to flow through the shunt transistor.

This is realized by the circuit shown in Fig. 3. The LDO regulator is formed by the error amplifier A1, the PMOS power transistor M1 and the resistive divider formed by the resistors R1 and R2. The supply current is flowing into transistor M1 which is steered to create a voltage drop V_{DS} between regulator input Iin and the output voltage terminal Vout such that the wanted output voltage is generated with respect to the current output terminal Iout which corresponds to the local ground potential. The shunt transistor M4 is added to this LDO scheme to provide an additional current path to the regulator output Iout.

To sense the amount of current that is flowing through the regulator, a fraction of the current flowing through transistor M1, which is defined by the current mirror aspect ratio k formed by transistor M1 and M2, is drained into the gate-drain connected transistor M5. The amplifier A2 and the cascode transistor M3 are added to improve the mirroring accuracy. For an ideal amplifier without offset, the voltage difference between the drain of the transistor M1 and the drain of transistor M2 is zero. Thus the value of the copied current is not affected by their low output impedance because transistor M1 and M2 see the same V_{gs} and the same V_{ds} voltage as well. A reference current that depends on the input potential V_{in} is defined by the

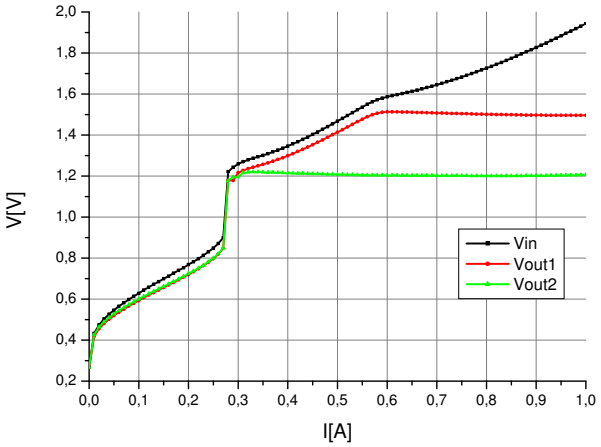

Fig. 5: Measured IV characteristics of two parallel placed Shunt-LDO regulator with different output voltages V_{out1} =1.5V & V_{out2}=1.2V

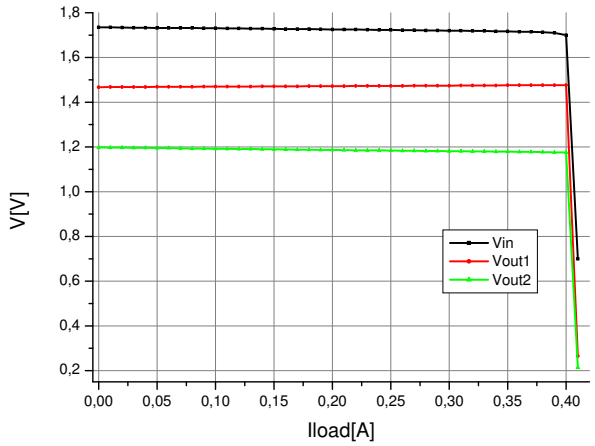

Fig. 6: Measurement of load regulation performance for two parallel placed devices. The slope corresponds to $60m\Omega$ incl. wire bonds

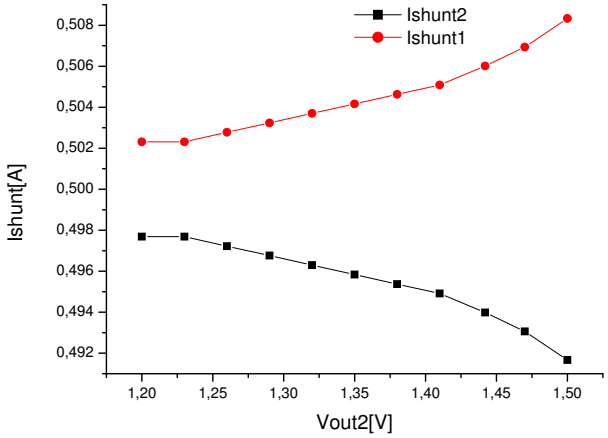

Fig. 7: Measured shunt current distribution as a function of V_{out2} with constant V_{out1}

resistor R3. This current is drained into the gate-drain connected transistor M6. For a wide transistor M6 operating in weak inversion, the reference current can be approximated by:

$$I_{ref} \approx \frac{V_{in} - V_{thM6}}{R3} \tag{2}$$

where V_{thM6} is the threshold voltage of transistor M6. The reference current is compared to the fraction of current flowing through transistor M1 by use of the differential amplifier A3. If the current drained to transistor M4 is smaller than the reference current, the shunt transistor M5 is steered to draw more current and vice versa. By this means the current that is not drawn by the load is shunted through the transistor M5 and as a result a constant current is flowing through transistor M1 with a value defined by:

$$I_{in} \approx k\frac{V_{in} - V_{thM6}}{R3} \tag{3}$$

From equation 3 it can be seen that the regulator behaves like an ohmic resistor with respect to the voltage drop V_{in} across the regulator. Neglecting the threshold voltage V_{thM6} and the current that is flowing through the amplifiers and the mirroring circuitry, the regulator has an equivalent input resistance of:

$$R_{in} \approx \frac{V_{in}}{I_{in}} = \frac{R3}{k} \tag{4}$$

In the same way, a current would be split evenly between parallel placed resistors of same resistance, the shunt current will be distributed uniformly on parallel placed regulators. As a result, a robust parallel operation of Shunt-LDO regulators is possible with the proposed regulation scheme. In addition, the output voltage that is generated by the regulator has no influence on the equivalent regulator input resistance. As a consequence, Shunt-LDO regulators generating different output voltages can be operated in parallel and supplied by the same input current source.

In Fig. 4, a simulation of the parallel operation of two regulators is shown, having an output voltage of 1.5V and 1.2V respectively. In the upper plot of Fig. 4, it is shown that the input potential V_{in} is rising linearly with increasing input current. The output voltages V_{out1} and V_{out2} follow the input potential V_{in} until the referenced voltage levels are reached. As can be seen in the lower plot of Fig. 4, the currents flowing through the regulators are exactly the same. In a real system, mismatch and process variation will lead to variation of the resistor R3 used as a reference of about 10-20% with an according influence on shunt current distribution. As will be discussed in the following section, the offset of amplifier A2 also has some influence on shunt current distribution especially during power-up.

For stable operation of the Shunt-LDO regulator, two regulation loops have to be studied and compensated. One regulation loop is voltage based and corresponds to the LDO regulator part of the circuit. For this loop, the standard LDO regulator compensation strategy is applied [6]. A dominant pole is introduced to the regulator output by use of an external capacitor. The Equivalent Series Resistance of the output capacitor introduces a zero which compensates the pole which is related to the error amplifier output impedance and the gate-source capacitance of the PMOS power transistor. The second regulation loop is current based and corresponds to the shunt circuitry. For this loop, a zero is introduced by an internal RC network which is connected between gate and drain of shunt transistor M4. Both loops have been designed to have a phase margin of minimum 65 degrees in the whole region of operation.

IV. Measurements

A Shunt-LDO regulator prototype has been implemented and produced in a 130nm CMOS technology. The prototype has been specified to generate voltages in the range of 1.2-1.5V and to draw a shunt current of up to 500mA. The reference resistor R3 has been

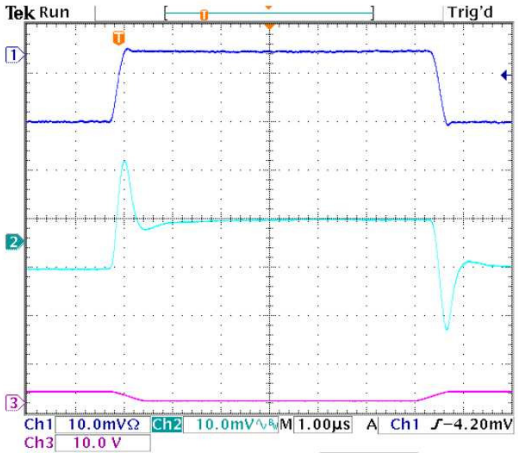

Fig. 8: Load transient behavior (2) for a load pulse of 150mA measured by the voltage drop across a series resistor of $10m\Omega$ (1)

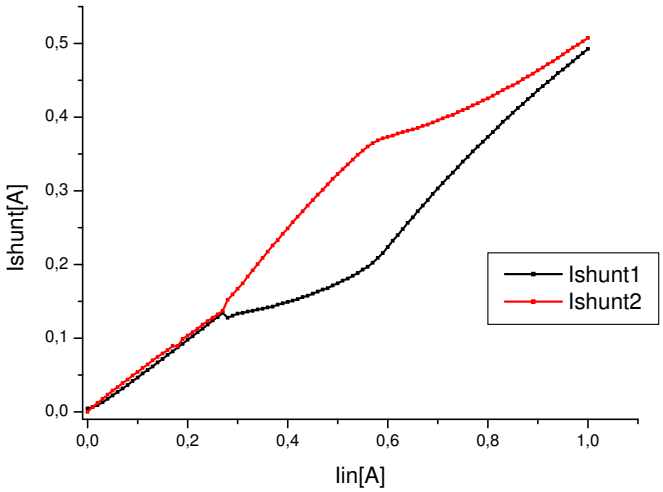

Fig. 9: Measured shunt current distribution during power-up

chosen to be $4k\Omega$ and the current mirror aspect ratio factor k has been set to 1000. In Fig. 5, the measured IV-voltage characteristic of two parallel placed regulators is shown, where one regulator is generating an output voltage of 1.2V and the other an output voltage of 1.5V. As has been predicted by the simulation, the voltage drop V_{in} across the regulator rises linear with input current as soon as a voltage potential V_{in} is reached where all transistors in the regulator are saturated. The output voltages follow the input voltage potential V_{in} until the referenced output voltages are reached. The measured slope of V_{in} is equivalent to a 2Ω resistor which corresponds to the input impedance of two parallel placed regulators.

In Fig. 6, the measured load regulation performance is depicted. A load current is drawn out of the regulator generating the output voltage of 1.2V which causes a slope at the output voltage which corresponds to $60m\Omega$ including wire bond and PCB parasitics. Taking into account the length and the specific resistance of the used wire bonds, the effective output impedance of the regulator is measured to be less than $30m\Omega$. The voltage output of the parallel operating regulator generating the 1.5V stays unaffected. In Fig. 7, the shunt current distribution between two regulators is measured at an input current of $1A$ fed to the input of both regulators. One regulator generates a fixed output voltage of 1.2V whereas the output voltage of the other regulator is swept from 1.2 to 1.5V. The shunt current changes only about 6mA in both regulators which corresponds to a change of 1.2% of the shunt current flowing through the regulator at equal output voltage potential.

An oscilloscope screenshot showing the load transient response of the regulator is found in Fig. 8. A load current pulse of 150mA is applied to a Shunt-LDO regulator which leads to an output voltage change of about 10mV in steady state (curve 2). This is equivalent to the output impedance of $60m\Omega$ which has been measured in the static case in Fig. 6.

The shunt current distribution during power-up of two parallel operating regulators with different reference voltage is shown in Fig. 9. An unbalanced shunt current distribution arises when the output voltage of one regulator reaches the referenced output voltage level whereas the other is still lower than the referenced output voltage level. More current is flowing through the regulator which is already saturated and generates the smaller output voltage. As soon as both regulators have reached the nominal output voltage level the shunt current distribution improves and becomes balanced again.

This unexpected behavior is understood and is caused by the offset of amplifier A2 which is used in the current mirror in Fig. 3. The offset of the amplifier leads to different V_{DS} voltages at transistor M1 and M2 which influences the current mirror aspect ratio when M1 and M2 are in linear region. This is the case when the output voltage is lower than the referenced value. When the referenced level is reached, transistors M1 and M2 get saturated and the influence of the offset vanishes. A similar behavior could be demonstrated in simulation when an offset voltage of 20mV is introduced to the amplifier A2. The shunt current distribution during power up can be improved when a special low offset architecture is used for amplifier A2. But still the available prototype does not exceed the maximum specified shunt current during power-up. In addition the observed behavior could be avoided completely, by choosing the same voltage reference during power-up and setting different voltages afterwards.

V. Conclusion

The proposed Shunt-LDO regulation scheme allows robust operation of parallel placed devices which increases redundancy and the reliability of serial powered systems. By use of this scheme additional flexibility is gained because parallel placed devices can generate different output voltages. The prototype study has proven the feasibility of the Shunt-LDO working principle and revealed the circuit part which is crucial for balanced shunt current distribution during start-up. For use in a conventional voltage based powering scheme, the shunt part of the regulator can be switched off and the device can be used as an ordinary LDO regulator.

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