Fachhochschule
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Shunt-LDO Regulator

RD53B Features

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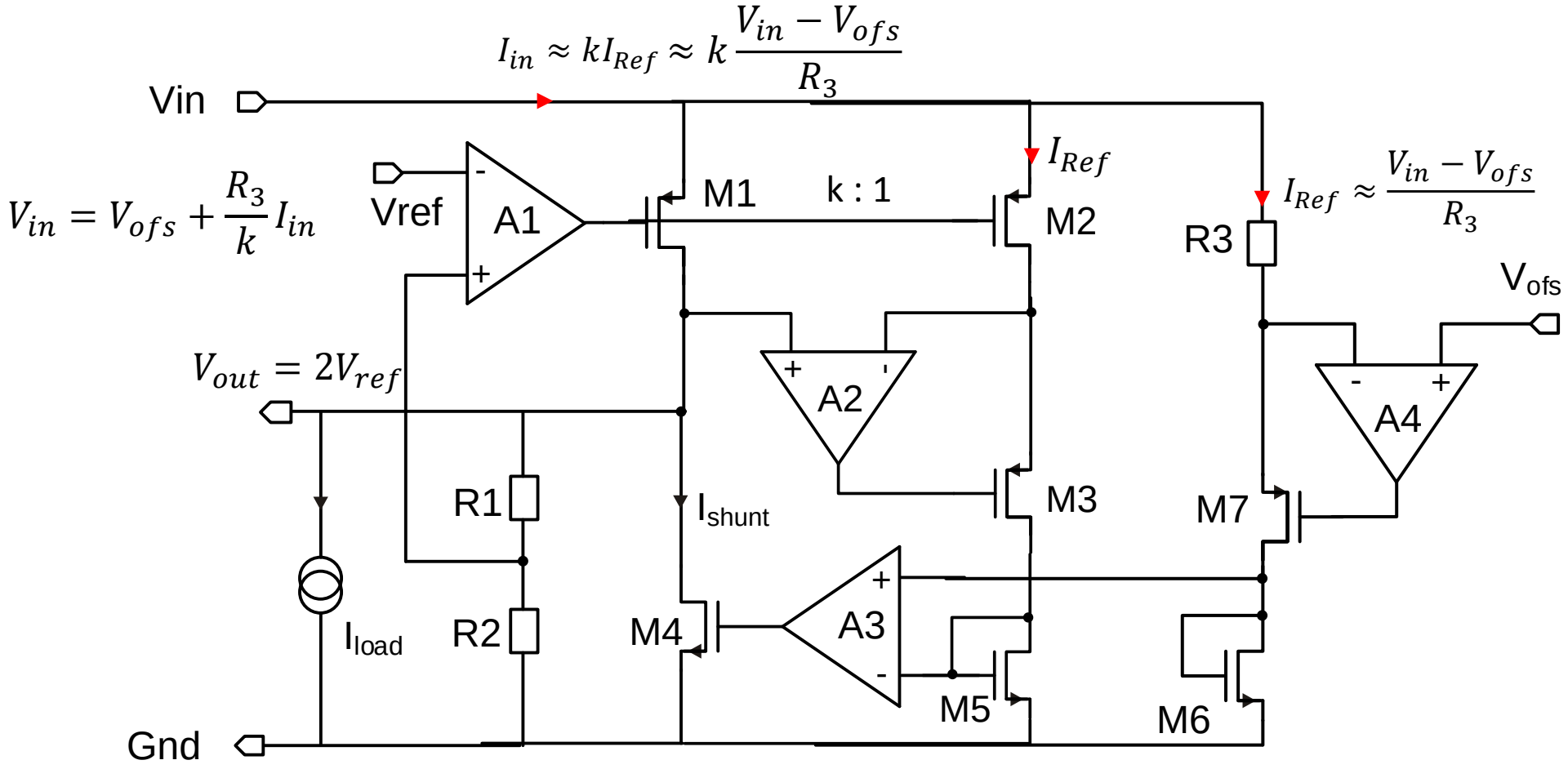
Talk Outline

- changes and improvements of RD53B with respect to RD53A SLDO version
- focus on user perspective and expected regulator behavior
  - limited information on implementation details
- modifcations to core design
  - minor issues like layout and connectivity
- protection features
  - overvoltage
  - overload
- new power mode

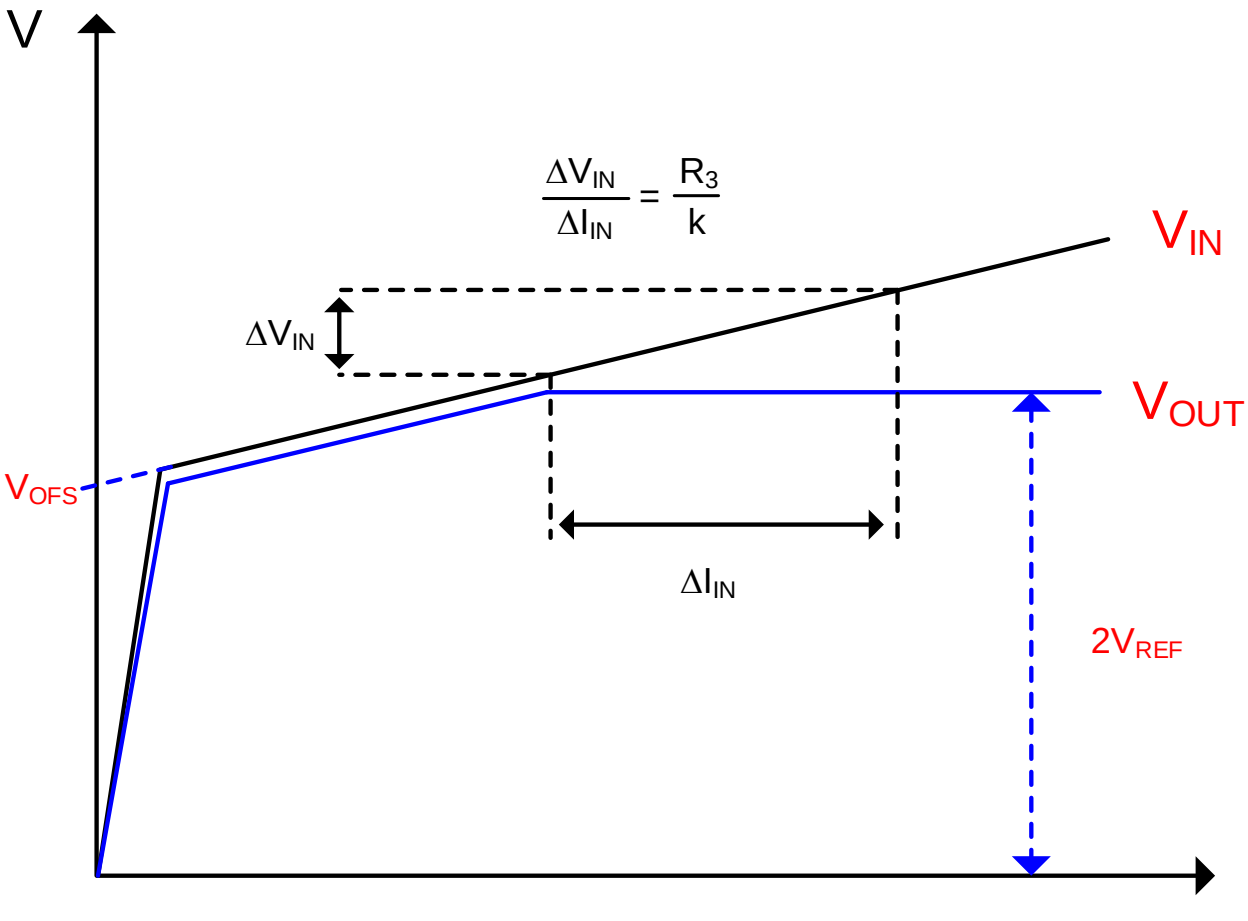
Design Concept

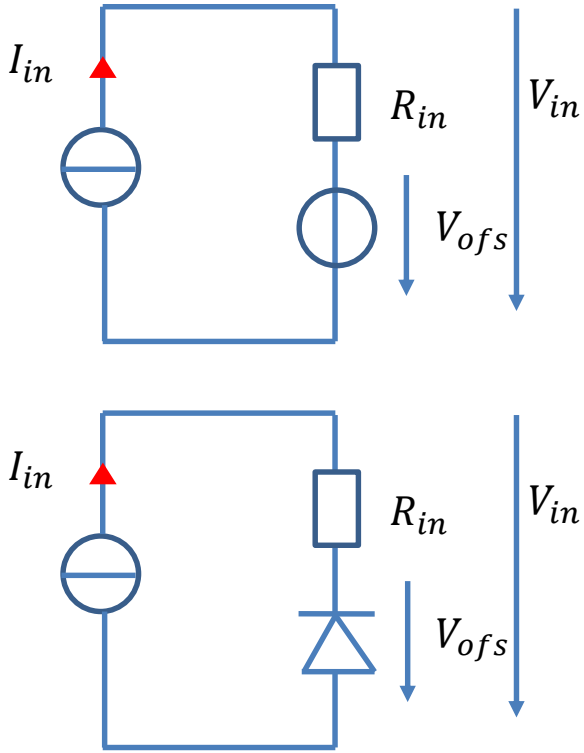
- The Shunt-LDO regulator combines the functionality of an LDO voltage regulator with the capability of a shunt regulator to drain a constant current
- Two control loops: 1) constant output voltage 2) constant current flow through the regulator



V/I Characteristic

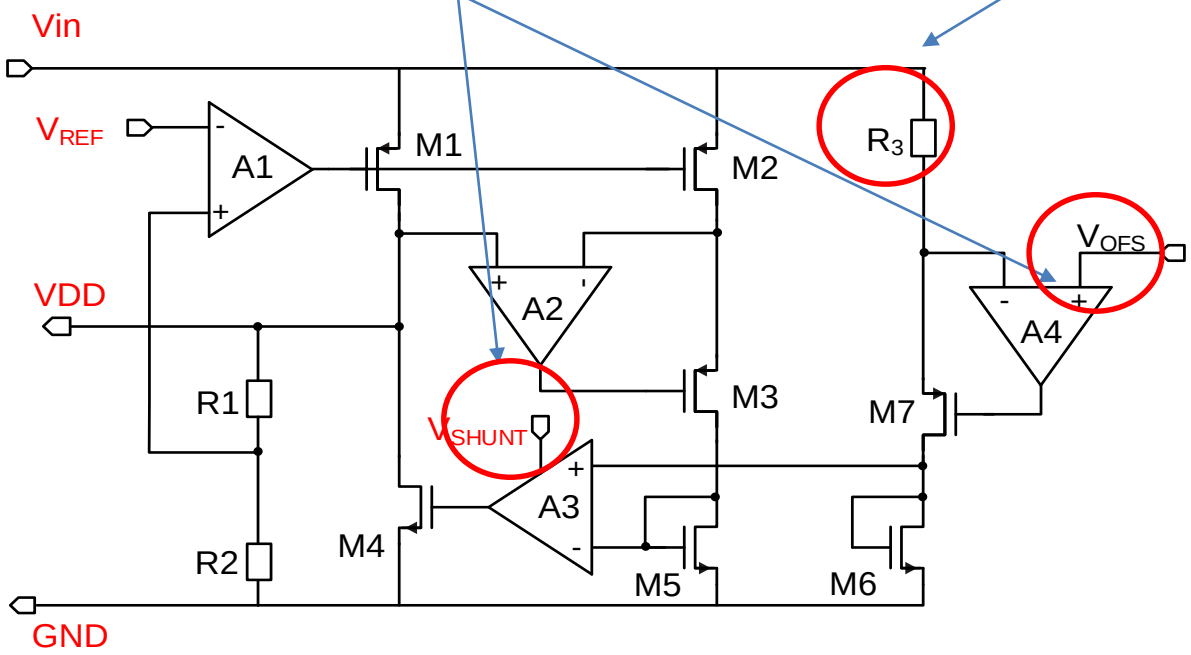
$$V_{in} = V_{ofs} + \frac{R_3}{k} I_{in}$$





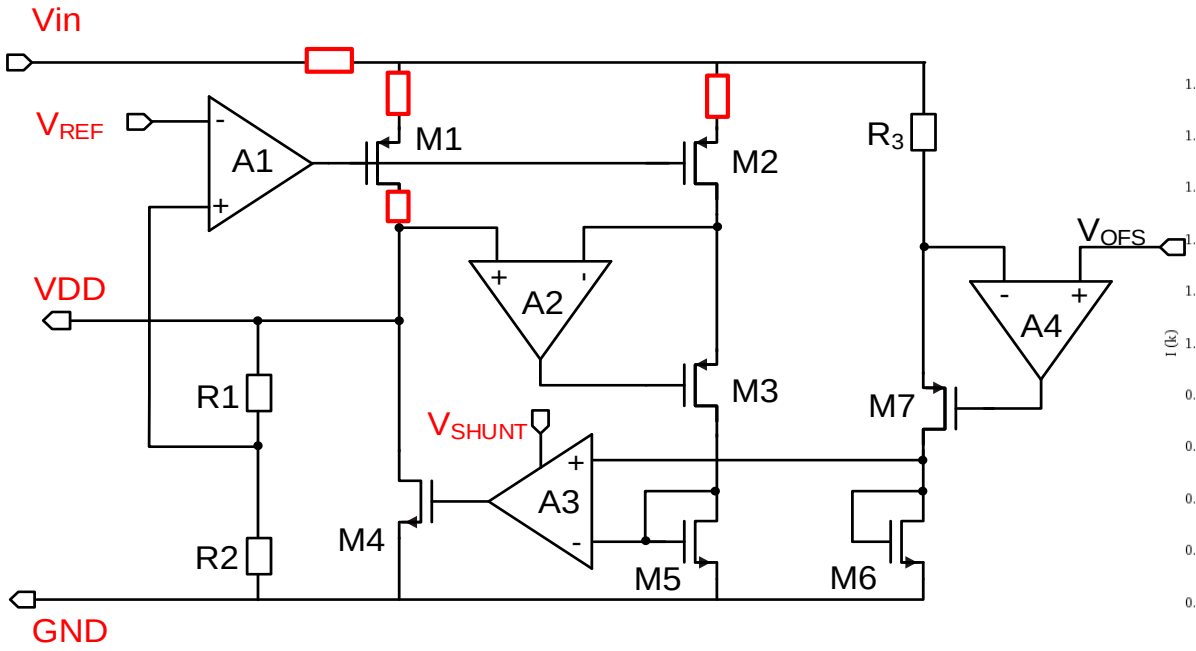
Modifications to Core Regulator Design

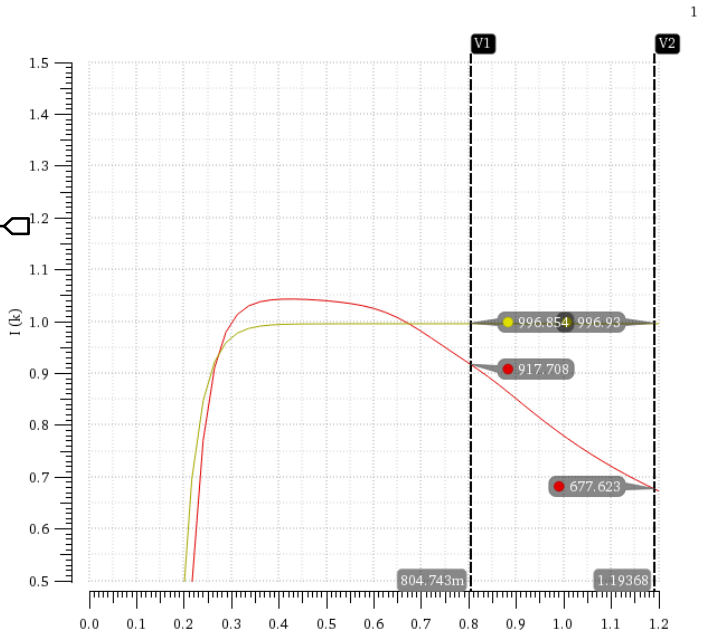
- reference resistor R3 defining the input impedance is only available as external component
  - integrated resistors show too large temperature and production variations
- common VDD_SHUNT pad for analog and digital regulator
  - regulators cannot be configured independent between Shunt/LDO mode
- Vofs terminal connected to biasing circuit off-chip
  - two addditonal pads Vofs_IN and Vofs_OUT available
  - Can be used for common Vofs voltage on module level to improve current distribution



Modifications to Core Regulator Design

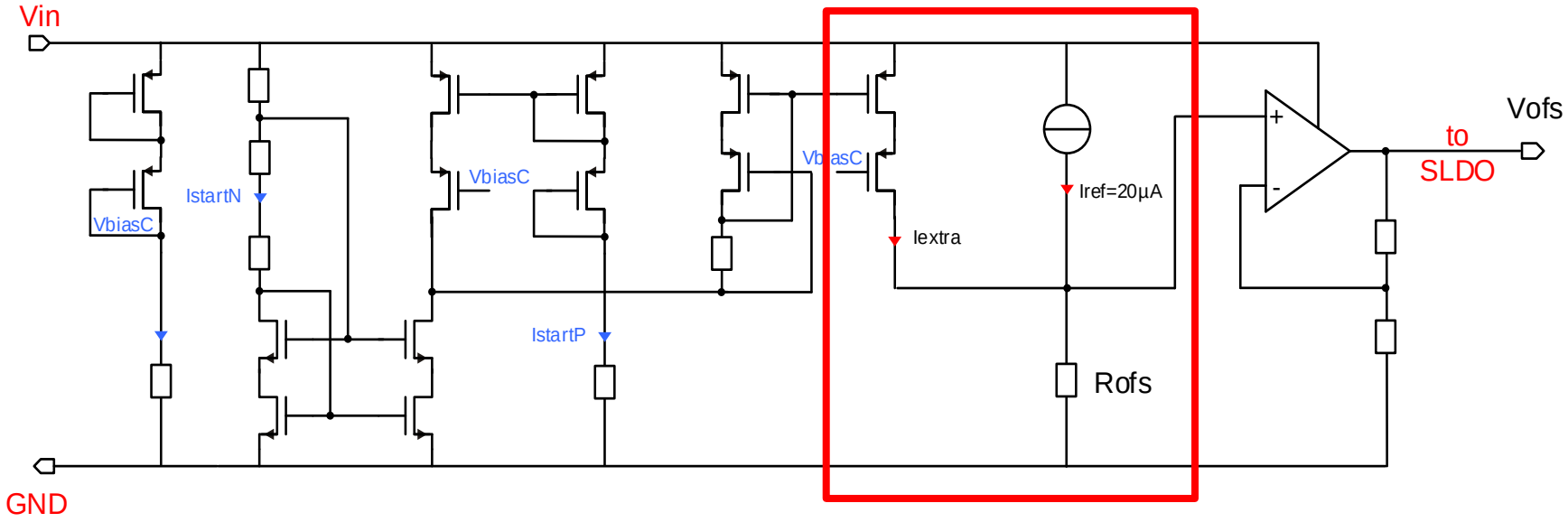
- new layout of the power transistors to reduce influence of parasitic resistors
  - measured input impedance (Vin slope) was larger than expected
  - parasitic resistors influenced M1/M2 current mirror ratio



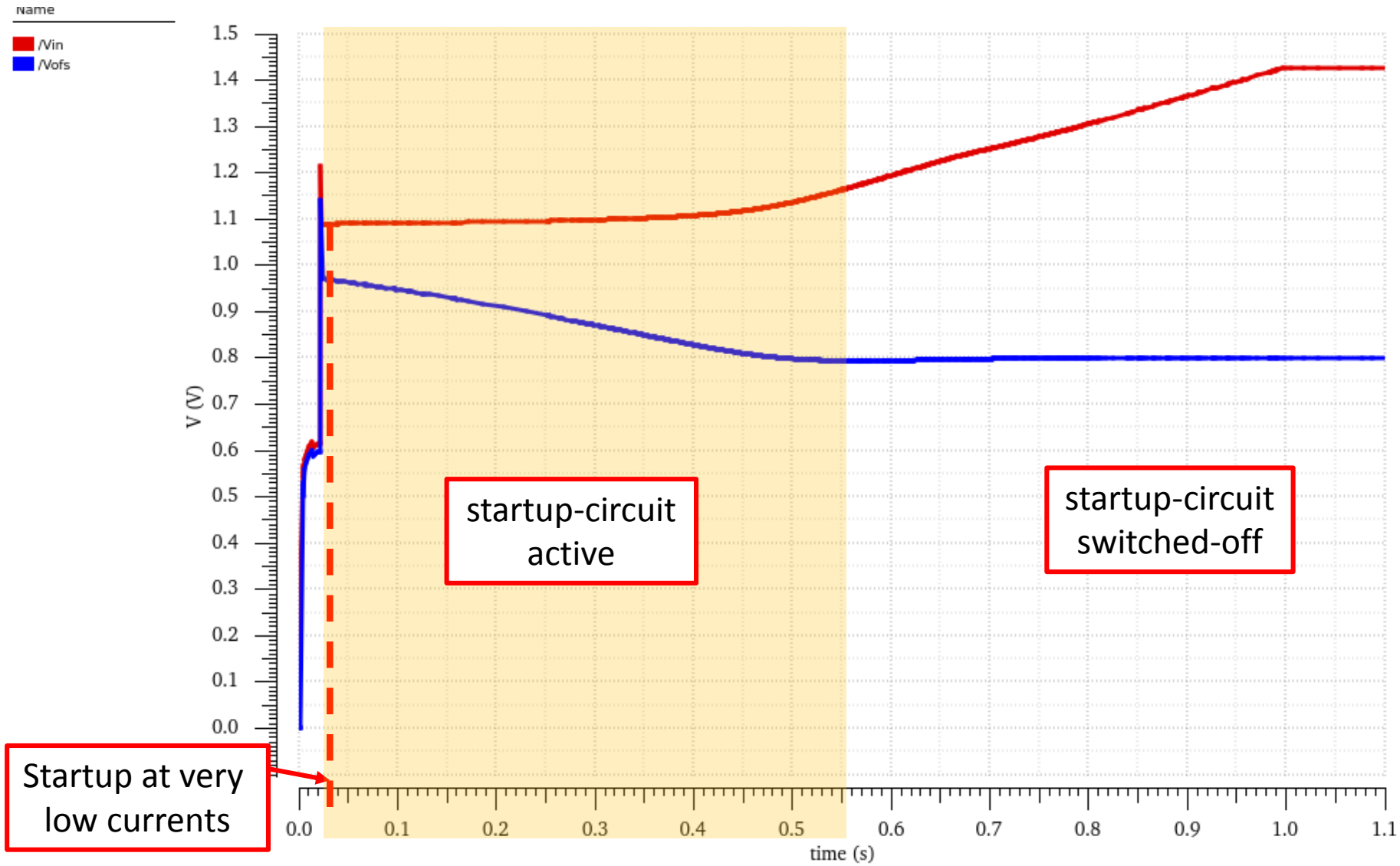


Improvements to Startup Behavior

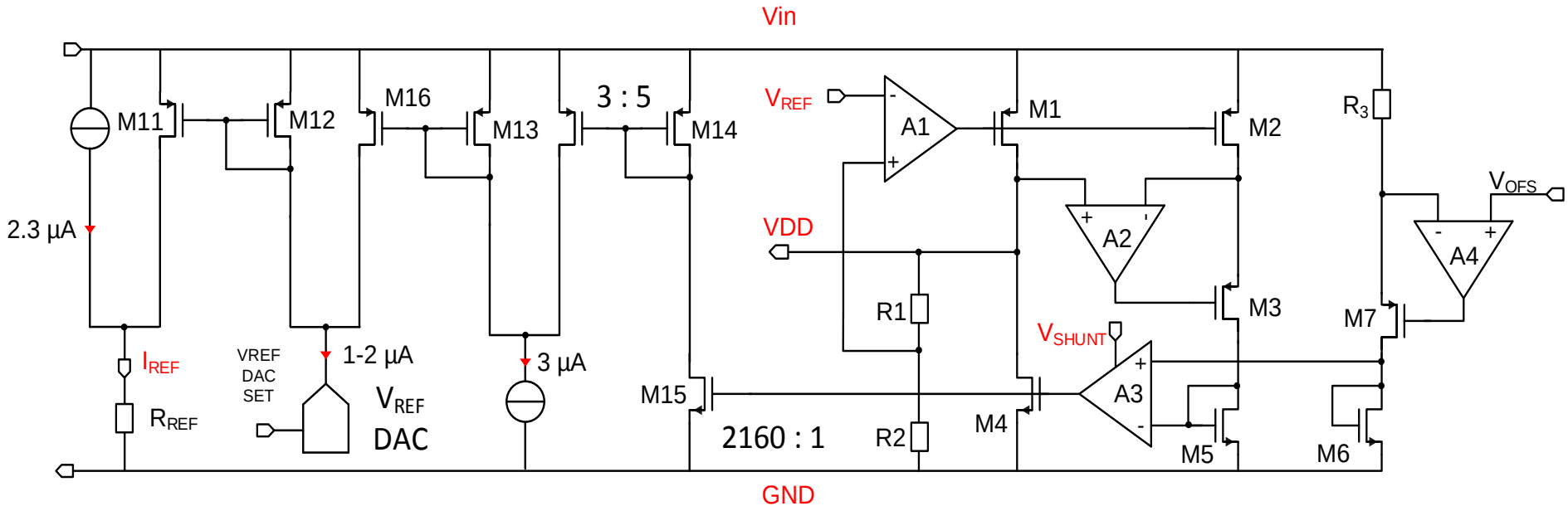
- RD53A used two independent bandgaps for the digital and analog regulator
  - different startup timing of the digital and analog regulator
- RD53B uses single bandgap for both the digital and analog regulator
  - regulators should startup at the same time
- Startup is supported by an newly introduced startup circuit
  - Vofs is drawn to high value close to Vin to increase regulator impedance
  - injection of additional current into the Rofs resistor
  - switch-off current injection after start-up



Simulation at 1A/1s start-up ramp

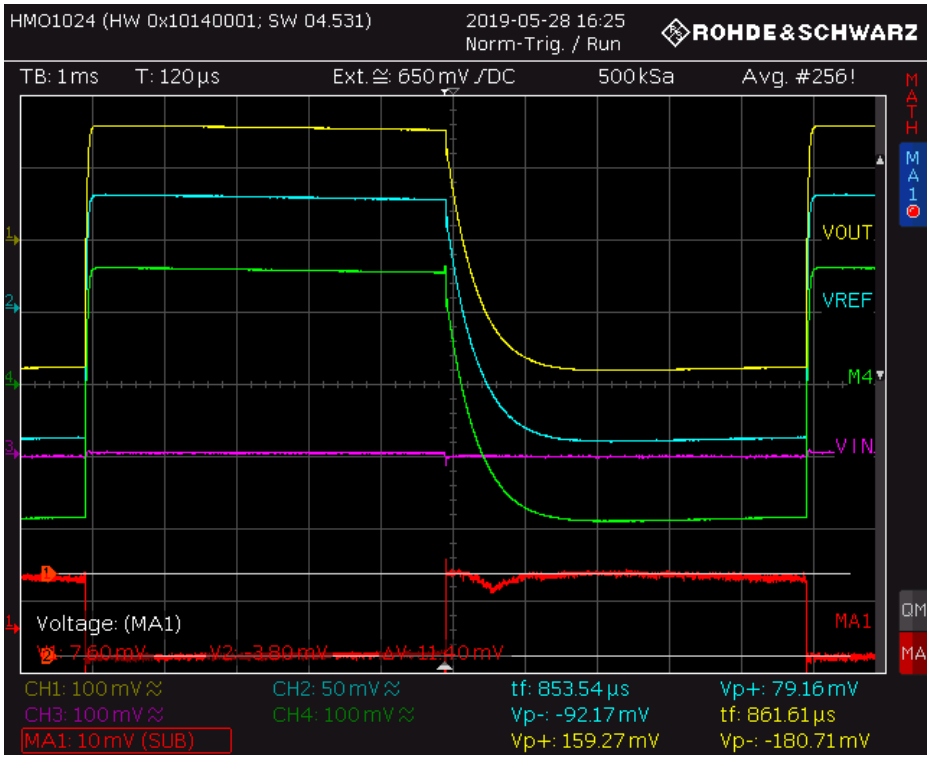


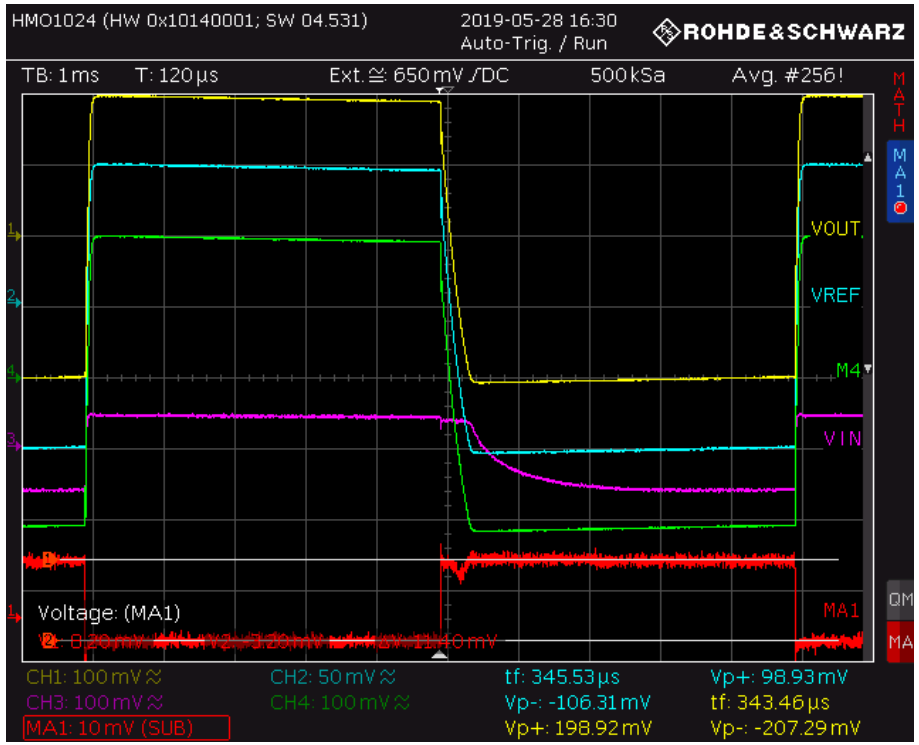
Protection Feature: Overload Protection



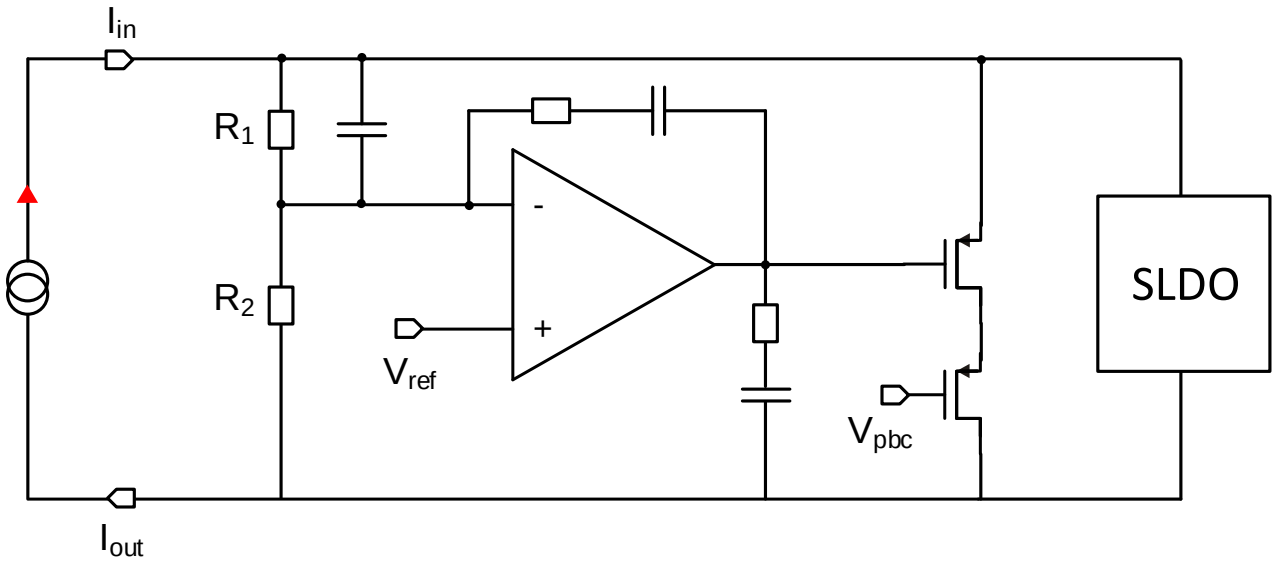
- With RD53A overload currents lead to collapse of regualtor input voltage
  - This lead to overvoltages at other modules in the serial chain
- RD53B protects against overloads which are considered as undershunt current scenarios
  - high load current reduces shunt current
- In undershunt current case Vout is reduced
  - Vout is lowered by lowering Vref
- Activation Threshold Ishunt < 10 mA
- Vout minimimum value 700mV → Vref minimum value 350 mV

Measurement of Overload/Undershunt Protection

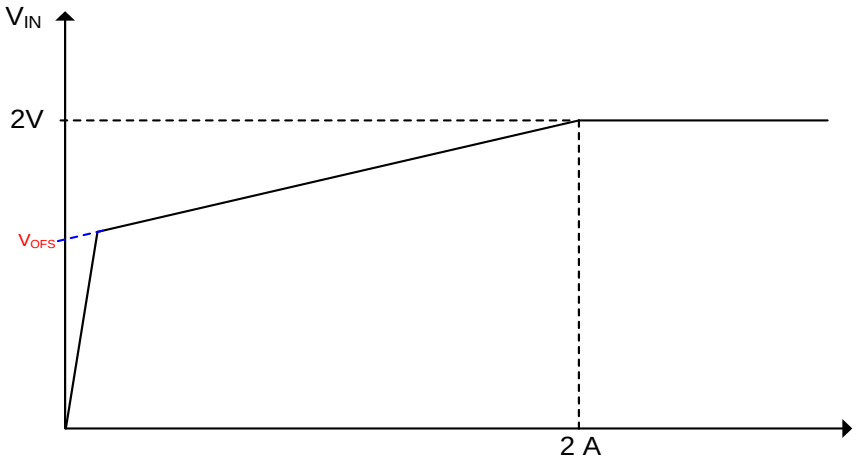




Protection Feature: Overvoltage Protection Voltage Clamp

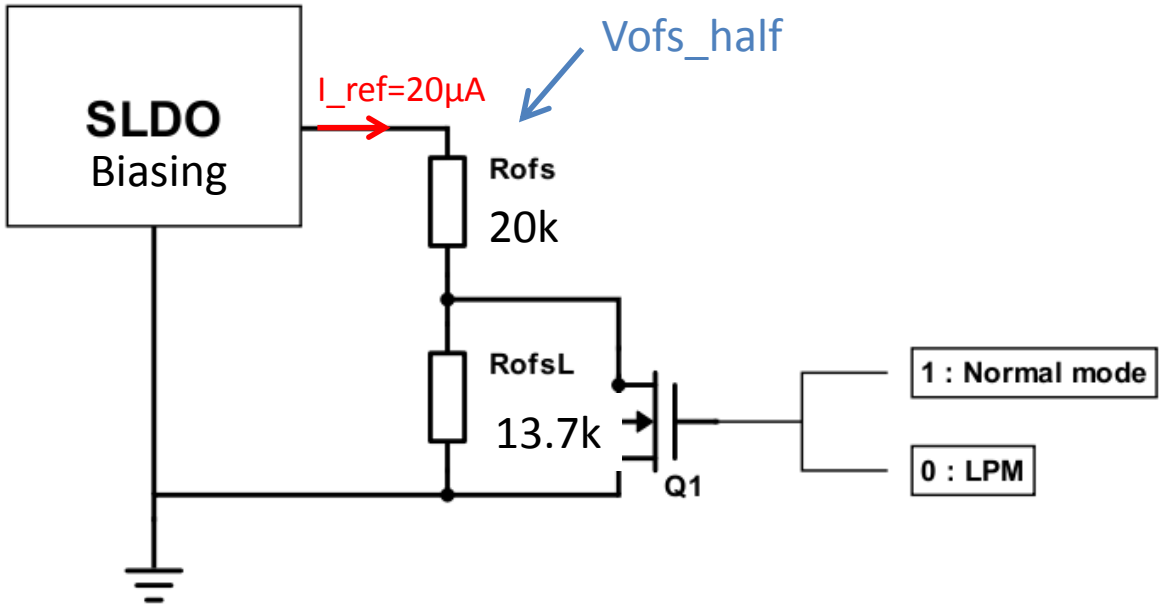


- voltage clamp implemented as shunt regulator
  - operated in parallel to SLDO
- takes all excess current in case Vin =>2v
- limits the voltage to 2V
- can absorb up to 2A additional current per chip
- OVP threshold defined by untrimmed bandgap
  - voltage limit can vary +/- 5%

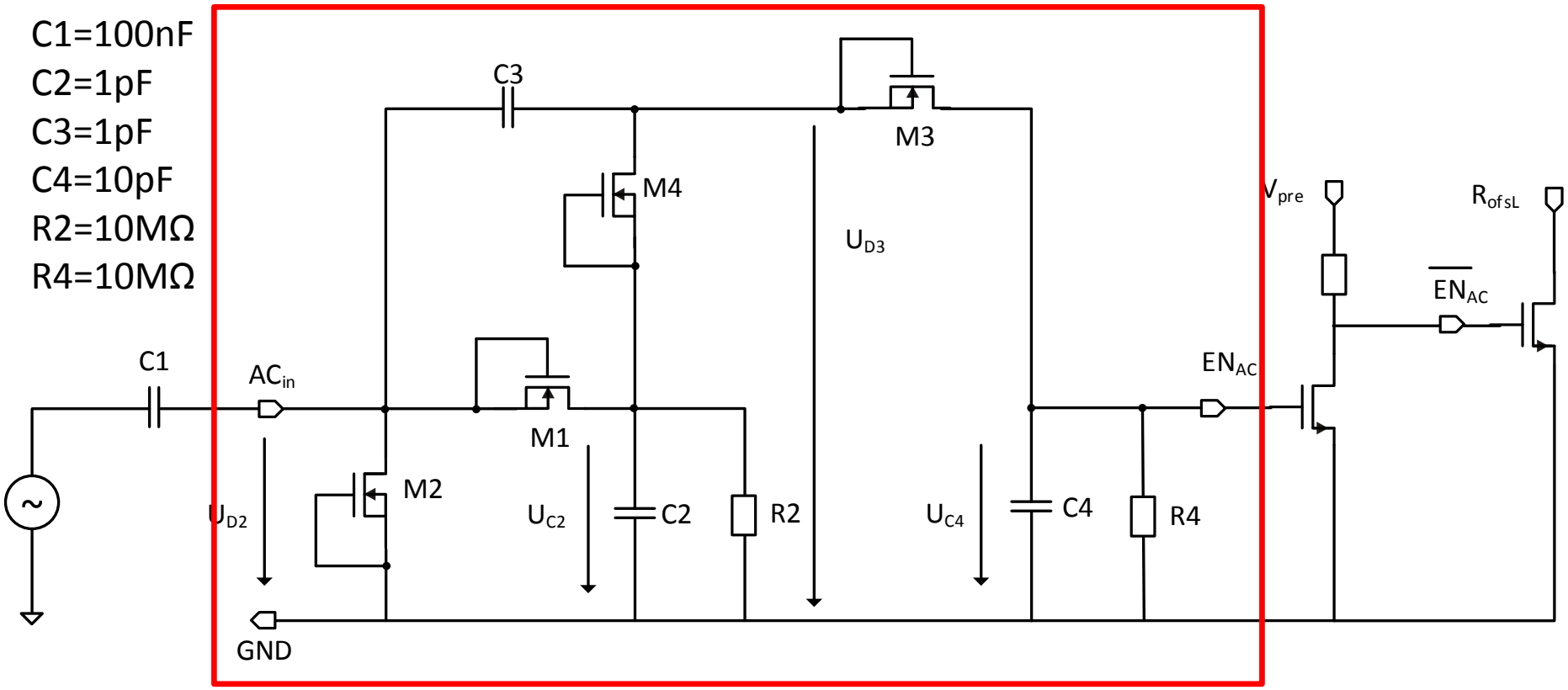


Low Power Mode

- during installation the detector will be operated without active cooling
  - to test connectivity
- detector operation mode at lower power consumption required
- SLDO has to reach the nominal operating point Vin=1.4V at lower input current
- configurable offset-voltage Vofs required
  - low Vofs for high power mode
  - high Vofs for low power mode
- switch introduce to enable/disable additional resistor in Vofs generation circuit
- switch is controlled by rectified AC signal

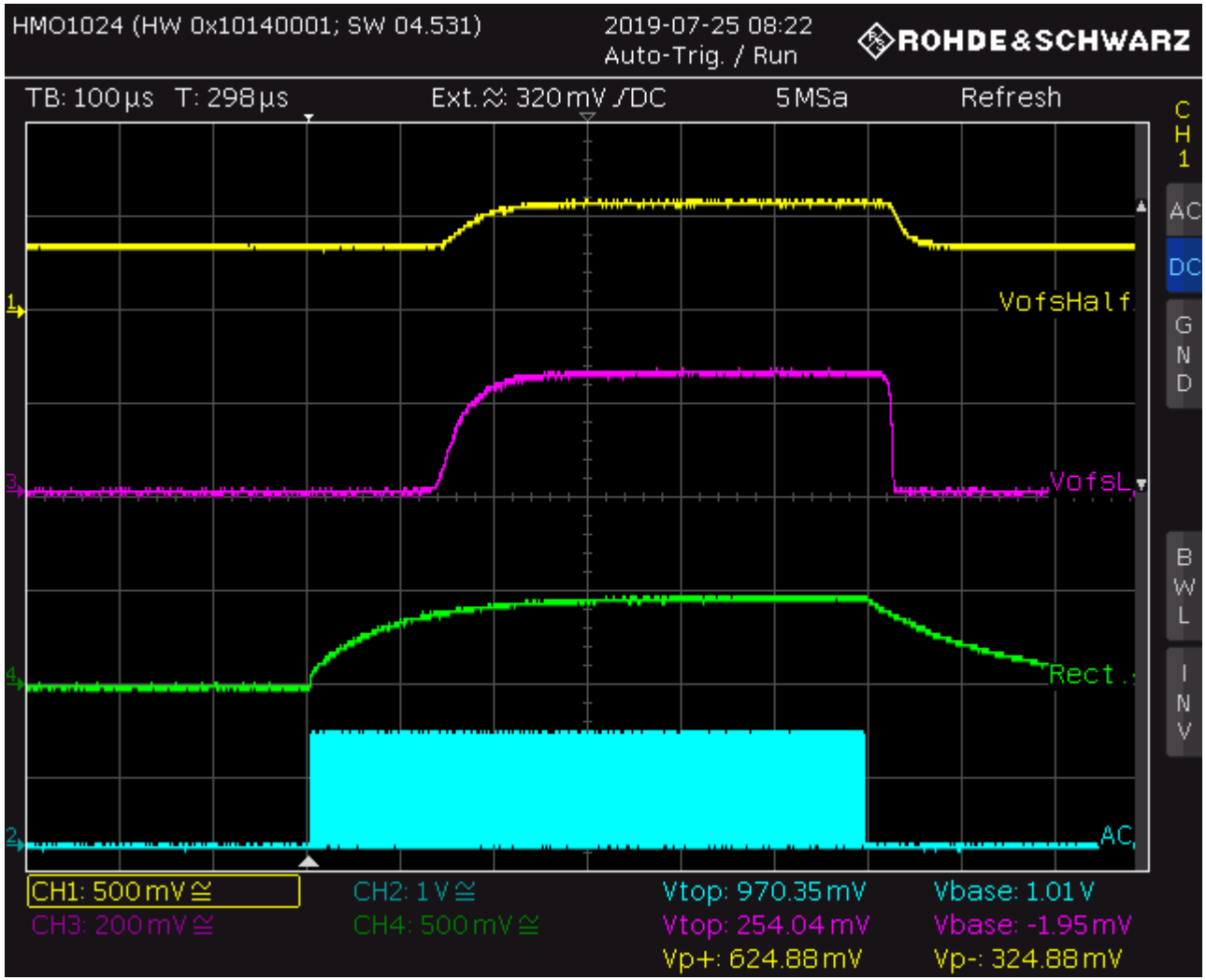


Rectification Circuit and Low Power Mode Interface



- rectification circuit with 2x multiplication
- AC signal is inverted and applied to a transistor in parallel two one of the Rofs resistors
  - Inverter is supply by Vpre using a resistor instead of PMOS to avoid SEU issues

Measurement AC Rectifier interaction with Vofs



Summary and Conclusion

- SLDO core design is almost the same
  - layout optimization and wiring modifications
- startup-behavior should become more deterministic
  - less bandgaps involved
  - startup-circuited integrated
- higher robustness and reliability aimed by protection features
  - overvoltage protection
  - overload/undershunt current protection
- Low Power mode initialization by Vofs configurability
  - AC rectification circuit integrated