Barrel module prototyping: PED request

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Introduction

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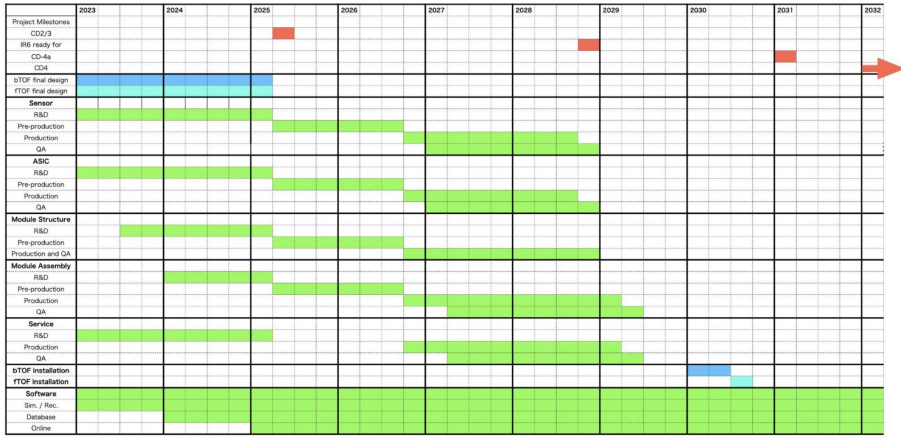
- CD 2/3 review expected at the end of 2024 (approval April 2025), and we are expected to demonstrate ~70% of the preliminary design at that point
- Over the next year, it's critical that we start assembly efforts with available components, and strengthen institutional collaboration

- Leading up to this review, we propose to demonstrate the module design for thermal and AC-LGAD signal characterization, to confirm performance obtained with standalone mini-components

Schedule and Timeline

Charge #4



Possible barrel module stack up

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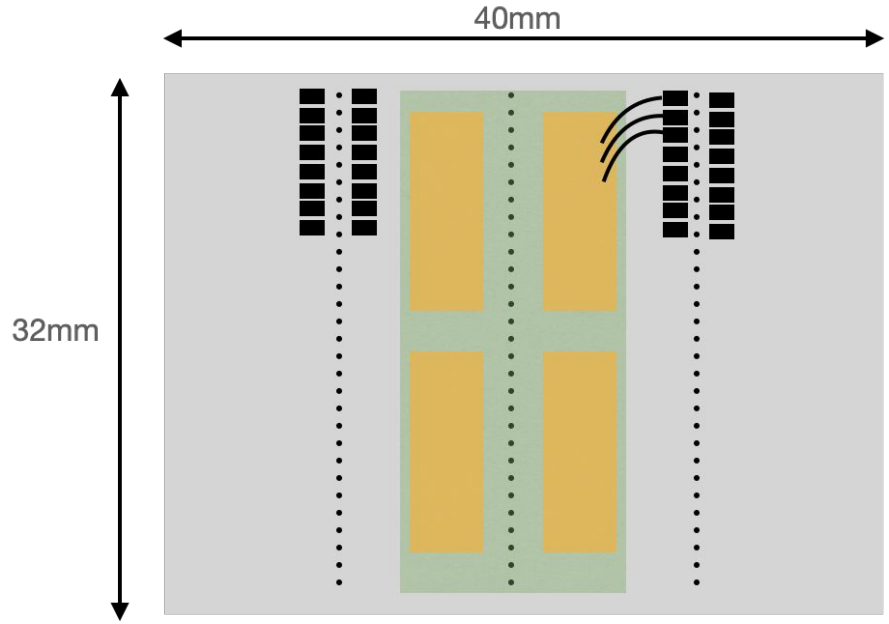
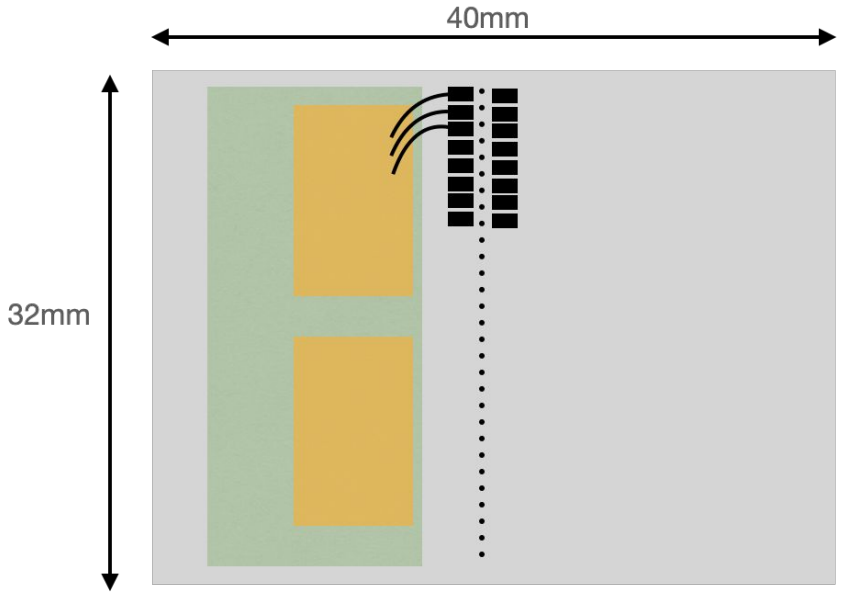
- Sensor length still an R&D topic, two possible scenarios shown below
- Hybrid flex glued onto sensor surface and ASICs wire bonded to sensor
- Would intend to use sensors from FY24 HPK and/or FBK productions





Thermal hybrid interposer

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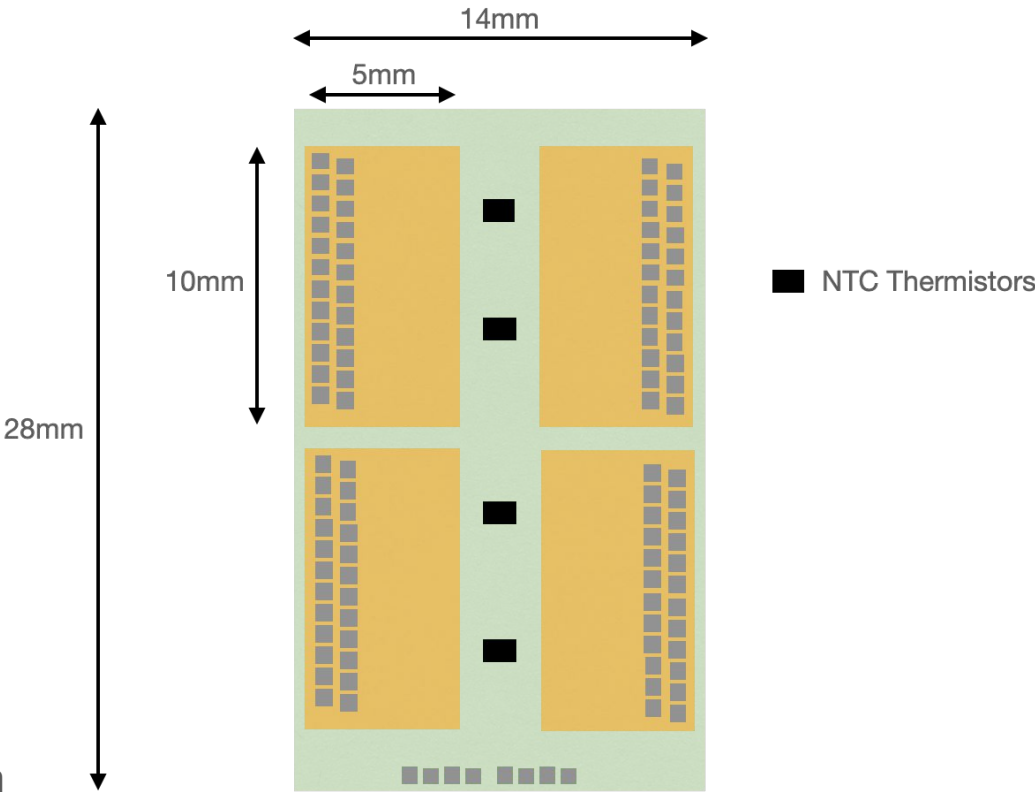
- Dimensions chosen to allow the interposer to fit onto 1 or two sensor segments, depending on strip length
- Four thermal ASICs per hybrid: these would be patterned glass ASICs, with a resistive trace to provide thermal load
  - Note: following discussing with our chip designers, long & narrow ASICs unlikely possible, and if so, would incur significant cost increase. Implications would need to be assessed, but not critical for these thermal studies
- NTC thermistors for thermal characterization
- Readout and end of board would need to be coordinated with hybrid flex design



Thermal module

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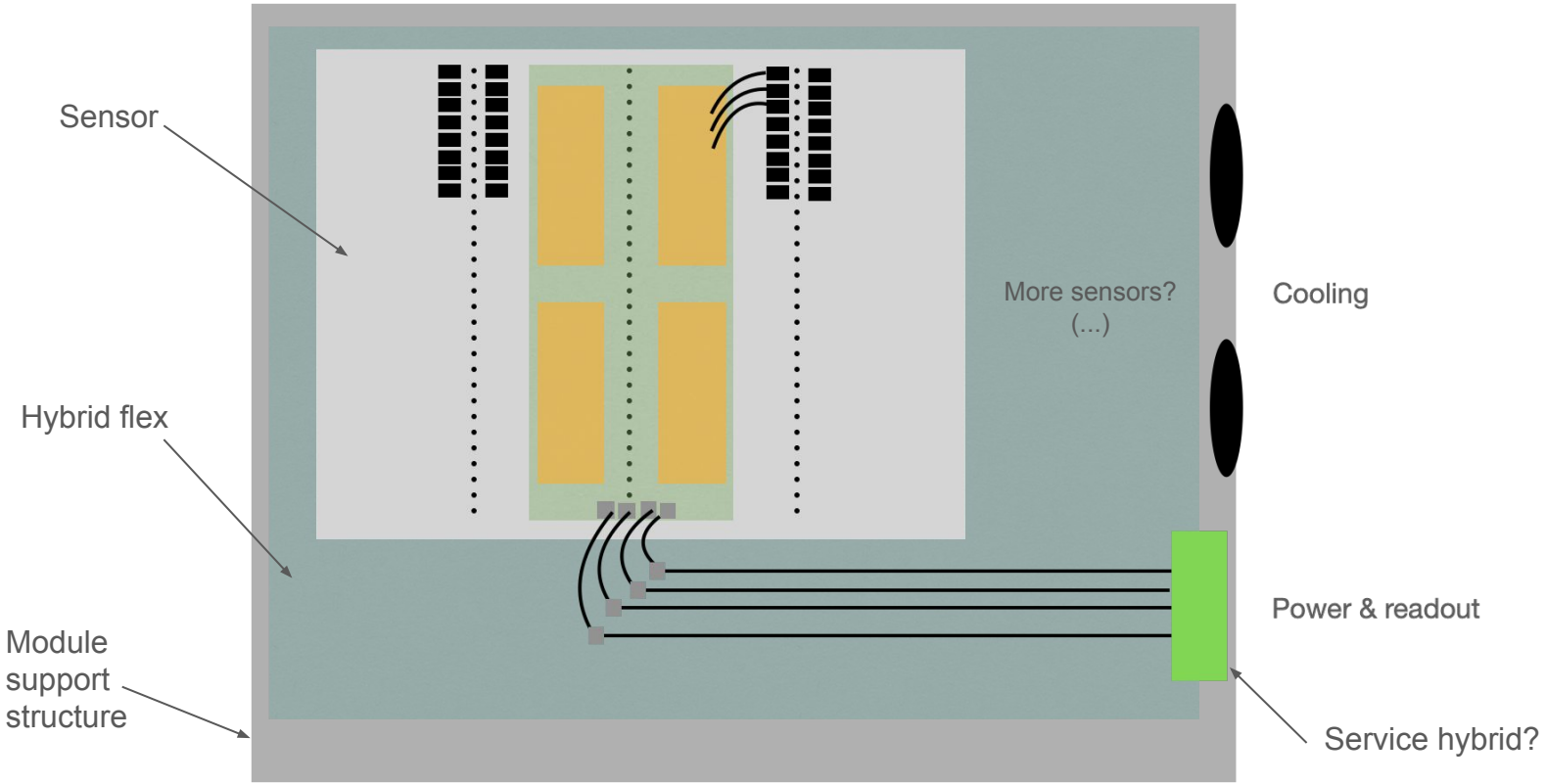

Interplay across activities

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- Several sub-components still under R&D – would require close collaboration to achieve these (small) prototypes:
  - **Module support structure** (Purdue,NCKU)
    - PED request ongoing, unsure whether short structures planned/possible?
  - **Hybrid flex** (ORNL)
    - Short flexes being worked on – details of interconnections would need to be defined
  - **Hybrid interposer** (UIC, UCSC)
    - Could be designed by UCSC for thermal characterization
    - Final design would need closer collaboration and expertise of ASIC team
  - **Thermal ASICs** (UCSC)
    - ASICs not expected until end of 2024, would plan for glass patterned ASICs with a resistive trace to simulate thermal load (in a few scenarios) as an interim solution
    - Thermal ASICs will simplify the design hybrid flex/interposer significantly
  - **Service hybrid** (Hiroshima,BNL,Rice, UIC)
    - Are early prototypes possible? Design hybrid flex to support with and without?
    - Funded in eRD109 FY24

Possible studies

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- Besides demonstrating the assembly procedure, many studies important studies could be performed with these thermal prototypes:
  - **Thermal characterization** under two possible scenarios for ASIC power consumption
    - Target 1 mW/channel, and worst case scenario 10 mW/channel ?
  - **Sensor characterization** when powered via hybrid flex
    - Current stability at operating bias voltage
    - Signal characteristics (amplitude, rise time, fall time) vs operating temperature
  - **Comparison of signal properties** for sensor segments with and without glue coverage
  - **Other ideas … ?**
- Would also intend to perform characterizations (electrical, metrology, etc) throughout the assembly procedure, and use this information to define QC/QA procedures, required tooling, etc in preparation for the TDR

Conclusions

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- PED request to develop preliminary design of module assembly
- UC Santa Cruz well positioned to perform all the technical assembly steps
- Much more discussion needed to settle upon a design and dimensions, and close collaboration needed across many different ongoing projects
- Feedback very much welcomed!