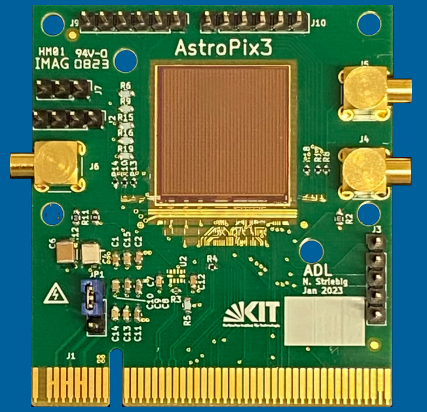
Barrel Imaging Calorimeter (BIC) Meeting

BIC - AstroPix updates



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HEP, Argonne National Laboratory

December 12, 2023

AstroPix V3

AstroPix V3 Single-Chip Board

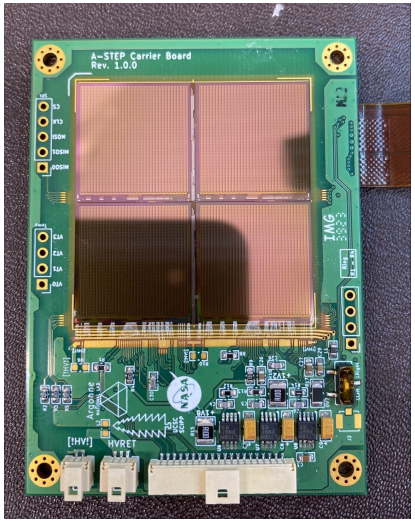
- Energy Resolution - individual pixel and full array
- Dynamic Range
- Depletion Depth measurement (~300-500 Ω.cm)
  - using α-spectroscopy ~ 100 µm
  - Edge-TCT measurement - data analysis
- Richard (KIT) developed new firmware to configure multiple chips
  - Amanda tested it - works well with single-chip

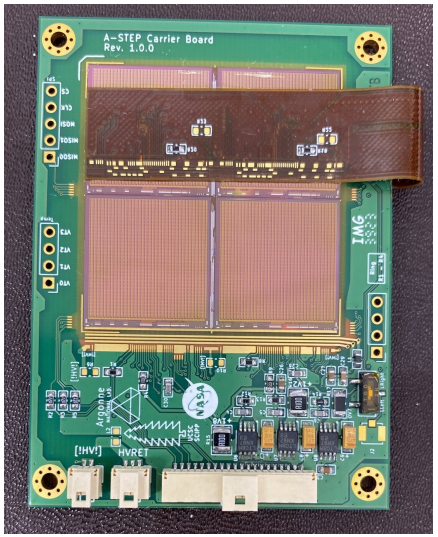
AstroPix v3 - Single Chip

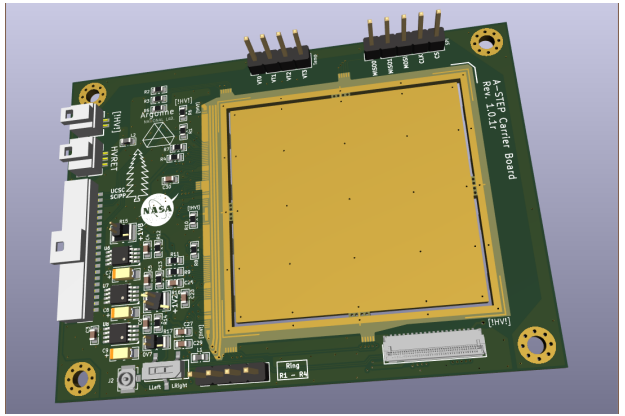
AstroPix V3

AstroPix V3 Quad-Chip Board

- The first few boards are ready to test (4)
  - Two boards were sent to Goddard
  - Two are available at ANL for testing
- Bottom-row chips available for daisy chain testing
  - The top two chips can not be wire-bonded at this moment
- The readout board needs refabrication
  - Correction in flex bus bar
  - Moving from Regid flex to connector
- Taylor re-iterated the Carrier Board Design
  - Under Review
  - Once the current board is tested, it will go for fabrication
- Taylor also designed initial schematic of 8 single-chip board - under review





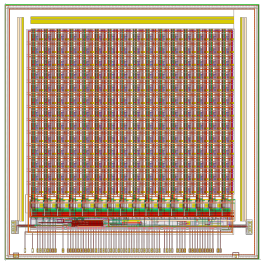


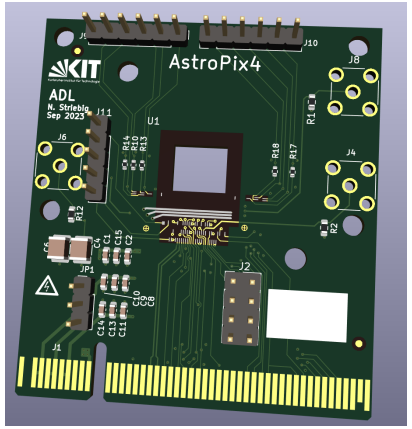
AstroPix v4

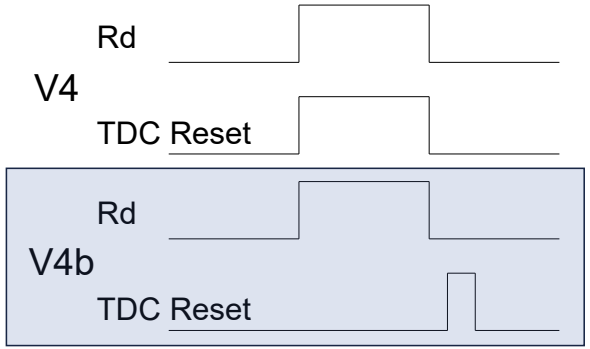
AstroPix v4 : The final design version will be small size

- The 25 low-resistivity chips are delivered to Argonne
- Two high-resistivity wafers are also Delivered to Argonne
- KIT is testing v4 chips (slides)
  - SW tested
  - Power consumption (~3mW)
  - ~400V break down
  - SPI readout noise issue - could be readout board (under test)
  - PLL/DLL works
    - TDC control logic restarts to early
    - TDC doesn't work - already fixed in v4b
    - Can provide 20MHz clock externally

AstroPix v4







AstroPix Future Runs

AstroPix v3

- TSI will deliver 24 wafers (low resistivity) this week
- There will be one more run with TSI - 25 wafers (low resistivity)
- After that TSI will stop fabrication facility
- In discussion with AMS to take over the fabrication

AstroPix v4b : Fixes from v4

- Multi-Project Run somewhere in March 2024 (so 1 cm x 1 cm chips)
- AMS will be the fabrication Foundry
- KIT is working on a few other technologies in the background just in case this happens again
  - Reanalyzing different foundries and processes
  - Reviewing other technologies (130/110 nm technologies)

AstroPix v5 : Full-size final design - Currently no changes to the timeline

- No planned design changes
- Full size chip - 2×2 cm^2, pixel pitch 500 μm,
- 35×35 pixel matrix $\rightarrow$ 1225 hit buffers

Thank you

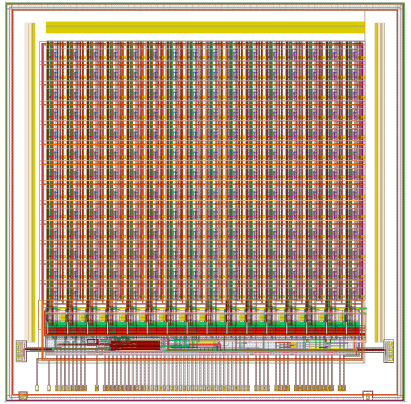
AstroPix v4

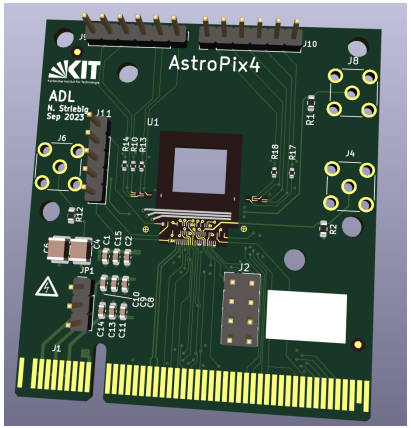
AstroPix v4 : The final design version will be small size

- Chip size 1 × 1 cm²; Thickness 700 µm, V_{BD} ~ 400V
- Pixel pitch 500 µm with pixel size 300 µm, 16 × 16 pixel matrix
- Individual pixel readout with individual hit buffer
  - No identification issue due to ghost hits
- 3 Timestamps - 2.5MHz (TS), 20 MHz (Fine TS), and 16 bit Flash TDC
  - Fast ToT and Timestamp with 3.125 ns time resolution
- TuneDACs - Pixel-by-pixel threshold tuning and pixel masking
- Daisy Chain readout - pass hits to next chip through QSPI
- Self-triggered (reads out active hits)

- The 25 low-resistivity chips are delivered to Argonne
- 2 high-resistivity wafers are also Delivered to Argonne
- KIT is testing v4 chips
  - ~400V break down

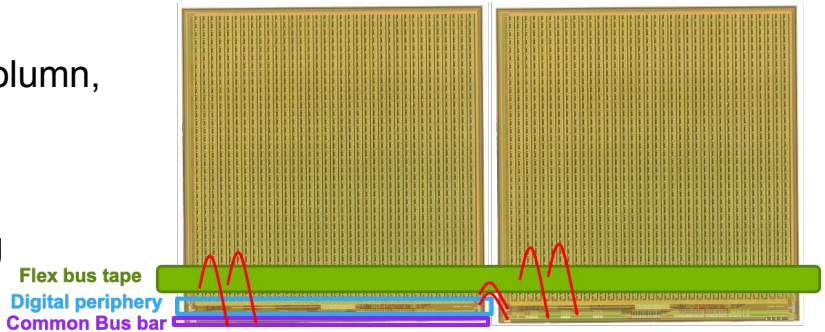
AstroPix v4

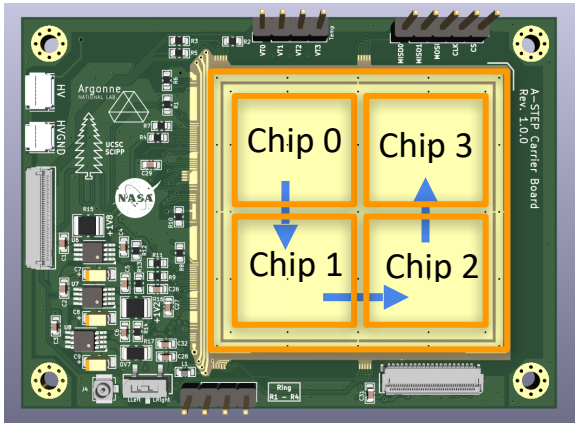




AstroPix Readout

- 8 bytes data per hit - header (chipID, payload), row/column, timestamp, ToT
- SPI I/O daisy chained - chip-to-chip signal transfer
  - signals are digitized & routed out to the neighboring chip using 5 SPI lines via wire bond
- Power/Logic I/O distribution on the module (through a bus tape)
  - 4 power lines (LV, HV), ~20 Logic I/O (SPI, clk, timestamp, interrupt, digital Injection, etc.)
  - HV, VDDA/VDDD(1.8V), VSSA(1.2V), Vminuspix(0.7V)
  - power distribution can be controlled using voltage regulators
  - mostly part of end of the stave services
- Data will be received by FPGA at the end of stave
  - FPGA aggregates data before sending off-detector
- Low heat load at chip, only cooling of end of the stave card
- Operational temperature for AstroPix is at room temperature and considered to be operated at 22 °C





AstroPix v3 quad-chip carrier board
- Demonstrate required services
- Daisy chaining