VTRX+ numbers for SVT (plus extra)

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EIC-UK WP1

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UNIVERSITY OF BIRMINGHAM

Readout considerations

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Left End Cap Data Switch

NEW!
CAN WE USE ONLY THE LINKS (LEC PADS) WE NEED? E.G. NO NEED FOR ADDITIONAL MUX IN EIC-LAS??

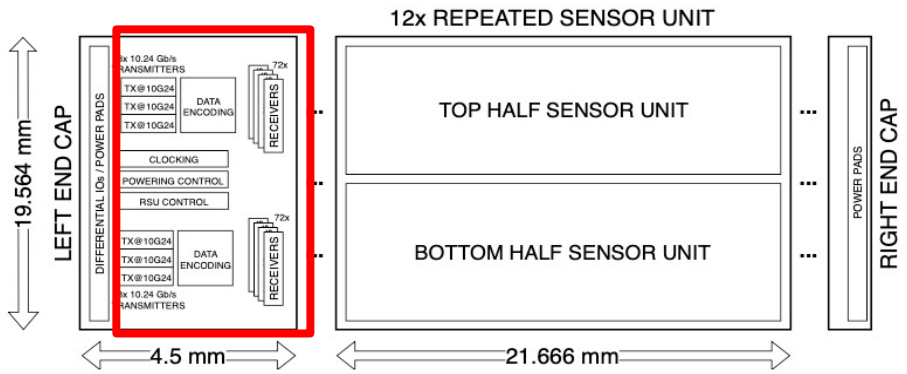


Figure 3.34: Block diagram of the sensor segment.

8x high speed serializers

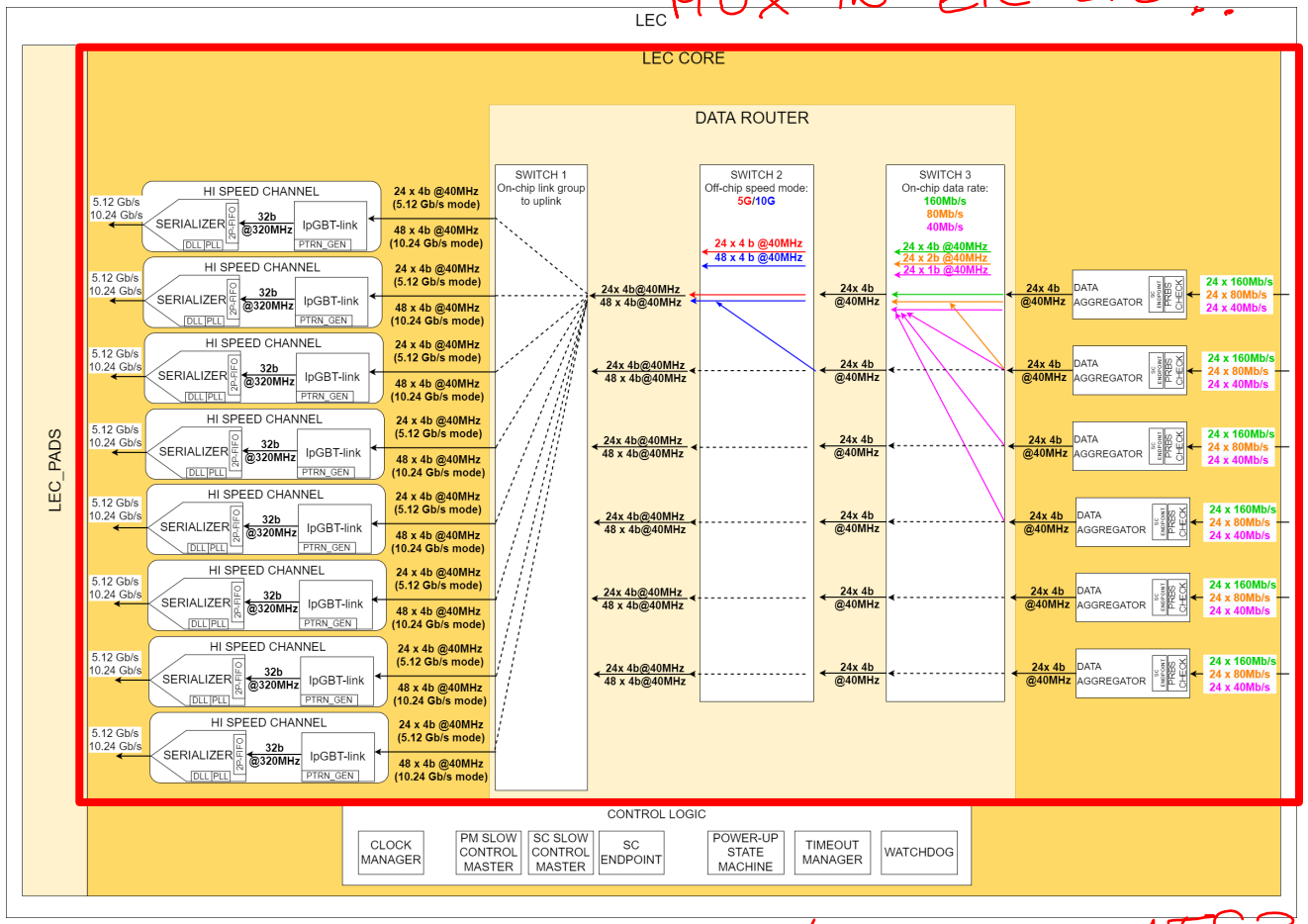
- Full capacity 80 Gb/s, 10 Gb/s each
- Fallback 40 Gb/s, 5 Gb/s each, bit stretching
- 4 outputs into one VTRx+

No memory nor data processing in LEC

- Max input capacity 144x160 Mb/s = 23 Gb/s

Switch matrix between tile inputs and outputs

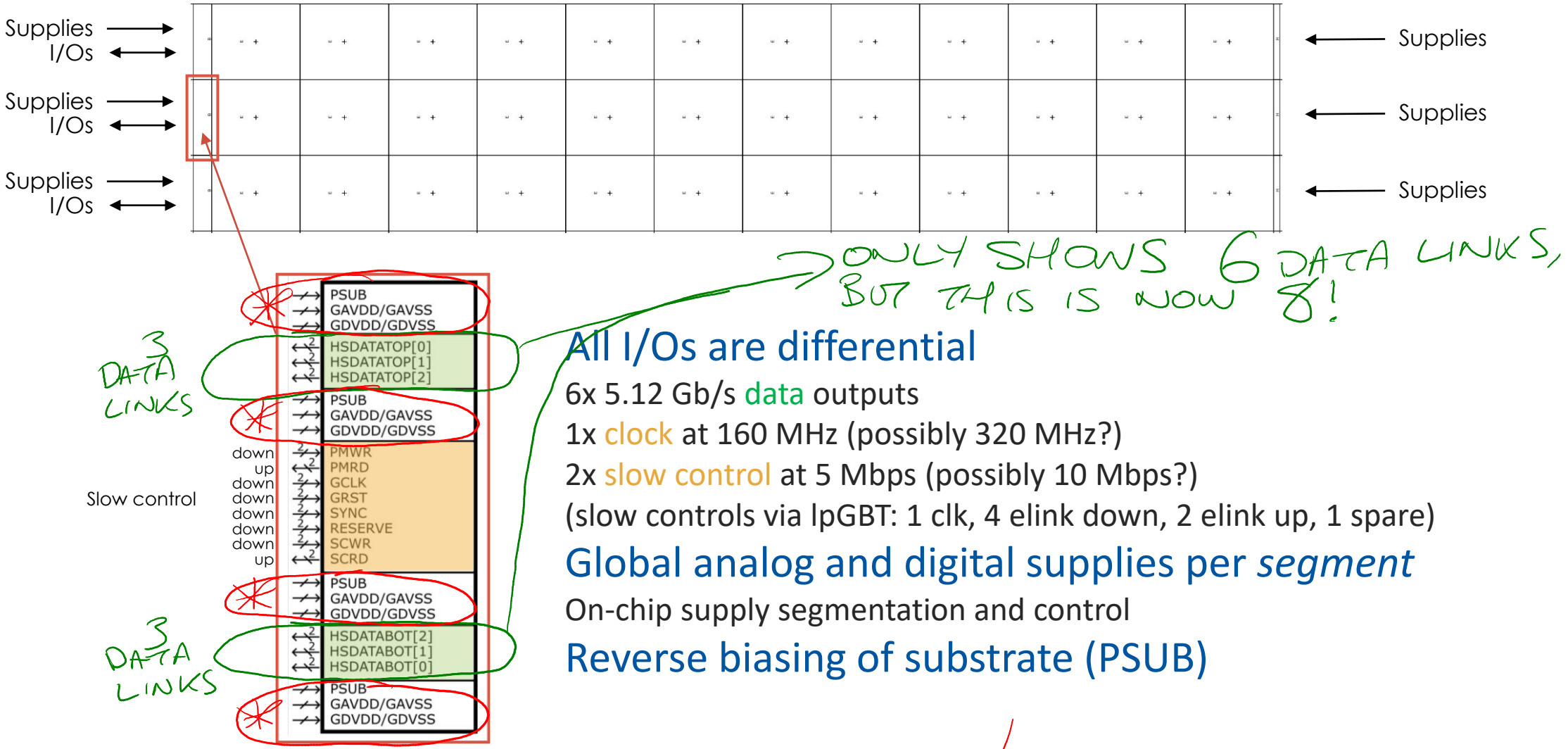
- Multiple data paths for redundancy to mitigate consequences of system faults



TILES

IF SO, DO WE USE ALL 8 LINK ON ITS3-LIKE IB LAYERS? WOULD 4 (E.G. 1 VTRX+) BE ENOUGH?

Supplies and I/Os



All I/Os are differential

6x 5.12 Gb/s data outputs

1x clock at 160 MHz (possibly 320 MHz?)

2x slow control at 5 Mbps (possibly 10 Mbps?)

(slow controls via lpGBT: 1 clk, 4 elink down, 2 elink up, 1 spare)

Global analog and digital supplies per *segment*

On-chip supply segmentation and control

Reverse biasing of substrate (PSUB)

lpGBT / FPGA for Slow Controls

FOR ALL EIC-LAS, Jo ASSUMES 1 DATALINK PER LEC (NO REDUNDANCY LINKS)

ASSUMES 6 LINKS PER LEC.

PETER'S OPTION 3 (LARGEST r AND L)

Barrel Layer Index	radius (mm)	z (mm)		Area (mm^2)	Sensor reticles in width	reticles in length	# of sensors in r-phi	# of sensors in z	# pixels	# sensors	Notes	# Readout Links	# Staves	# FPGAs / lpGBT
0	36	270		61,073	3	12	4	1	119,149,056	4	bent ITS3	72		4
1	48	270		81,430	4	12	4	1	158,865,408	4	bent ITS3	96		5
2	120	270		203,575	5	12	8	1	397,163,520	8	bent ITS3	240		13
3	270	540		916,088	1	5	87	5	1,799,647,200	435	1x5 LAS	435	87	11
4	420	840		2,216,706	1	5	135	8	4,468,089,600	1080	1x5 LAS	1080	135	17
e-endcap														
Disk index	**z (mm)**	**inner r (mm)**	**outer r (mm)**											
1	-250	36.76	240	176,710	1	5			347,518,080	84	1x5 LAS	84	52	7
2	-450	36.76	415	536,815	1	5			1,050,828,480	254	1x5 LAS	254	86	11
3	-650	36.76	421.4	553,632	1	5			1,083,925,440	262	1x5 LAS	262	88	11
4	-900	40.0614	421.4	552,835	1	5			1,079,788,320	261	1x5 LAS	261	88	11
5	-1150	46.3529	421.4	551,127	1	5			1,079,788,320	261	1x5 LAS	261	88	11
h-endcap														
Disk index														
1	250	36.76	240	176,710	1	5			347,518,080	84	1x5 LAS	84	52	7
2	450	36.76	415	536,815	1	5			1,050,828,480	254	1x5 LAS	254	86	11
3	700	38.52	421.4	553,216	1	5			1,083,925,440	262	1x5 LAS	262	88	11
4	1000	53.43	421.4	548,909	1	5			1,071,514,080	259	1x5 LAS	259	88	11
5	1350	70.14	421.4	542,422	1	5			1,059,102,720	256	1x5 LAS	256	88	11
TOTAL				**8,208,062**					**16,197,652,224**	**3768**		**4160**	1026	152
									# of segments:	**3820**	#VTRx+	**1040**		
									# of elinks down	19100	# lpGBT	**1194**		
									# of elinks up	7640				

ONLY 5 RSU LAS CONSIDERED

OAK RIDGE National Laboratory

Powering considerations

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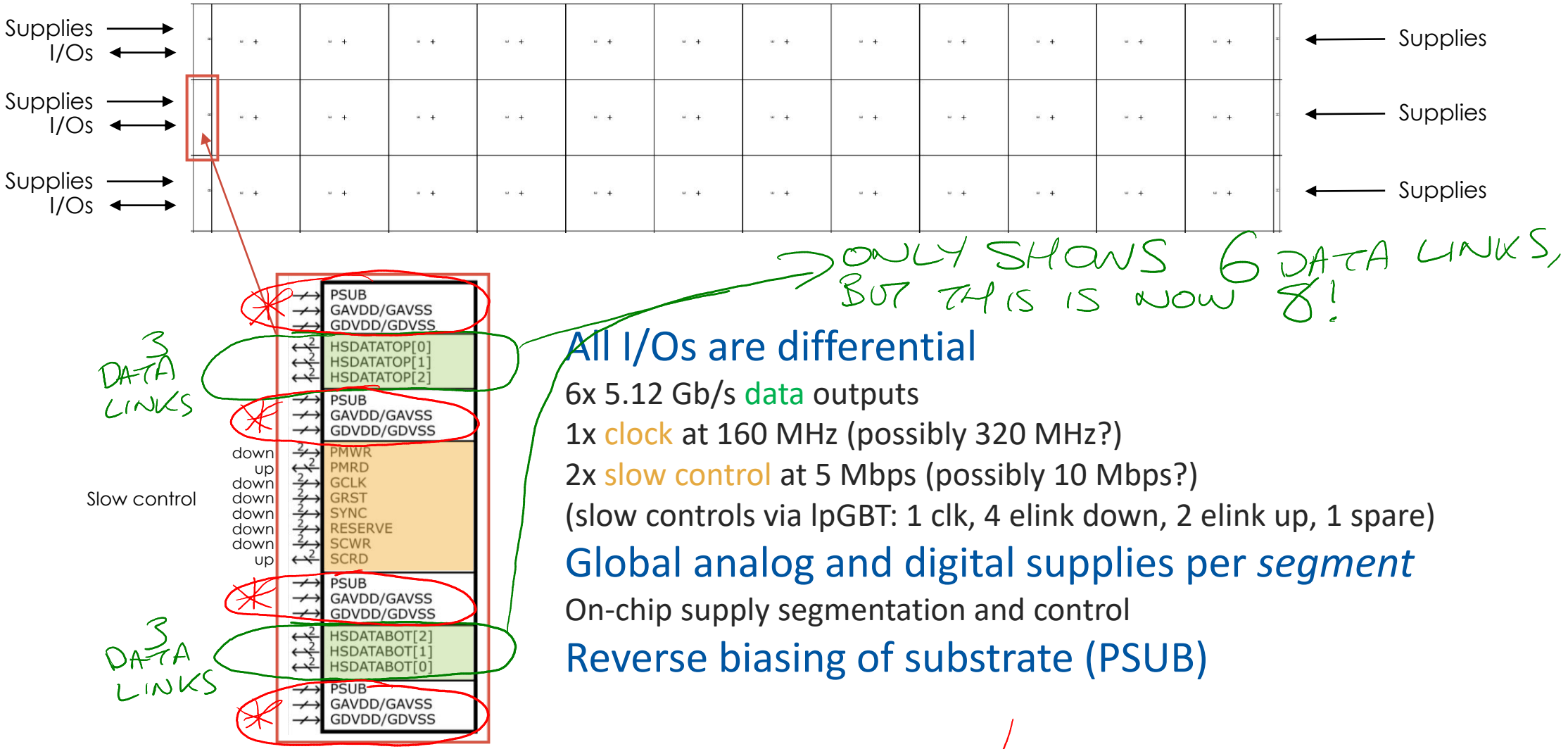
Power Domains and Currents

Supply purpose	Nets	Voltage [V]	Current [mA]	Pads on LEC	Pads on REC
Services	SDVDD-SDVSS	1.2 to 1.32	227	Yes	Yes
Global analog	GAVDD-GAVSS	1.2 to 1.32	540	Yes	Yes
Global digital	GDVDD-GDVSS	1.2 to 1.32	1369	Yes	Yes
Serializers	TXVDD-TXVSS	1.8	200	Yes	No
Substrate bias	PSUB	−1.2 to 0			

NEW, EXTRA PADS? THERE IS NO REFERENCE TO THESE IN PREVIOUS LEC CONNECTION SCHEMES.

Table 3.11: Power domains of one sensor segment. The substrate bias is common to all the segments composing a sensor. The nominal operating voltage are referred to the potential of the GAVSS input net. The input currents are obtained assuming the maximum estimated power consumption of the LEC and RSU circuits at 25 °C.

Supplies and I/Os



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Global analog and digital supplies per *segment*

On-chip supply segmentation and control

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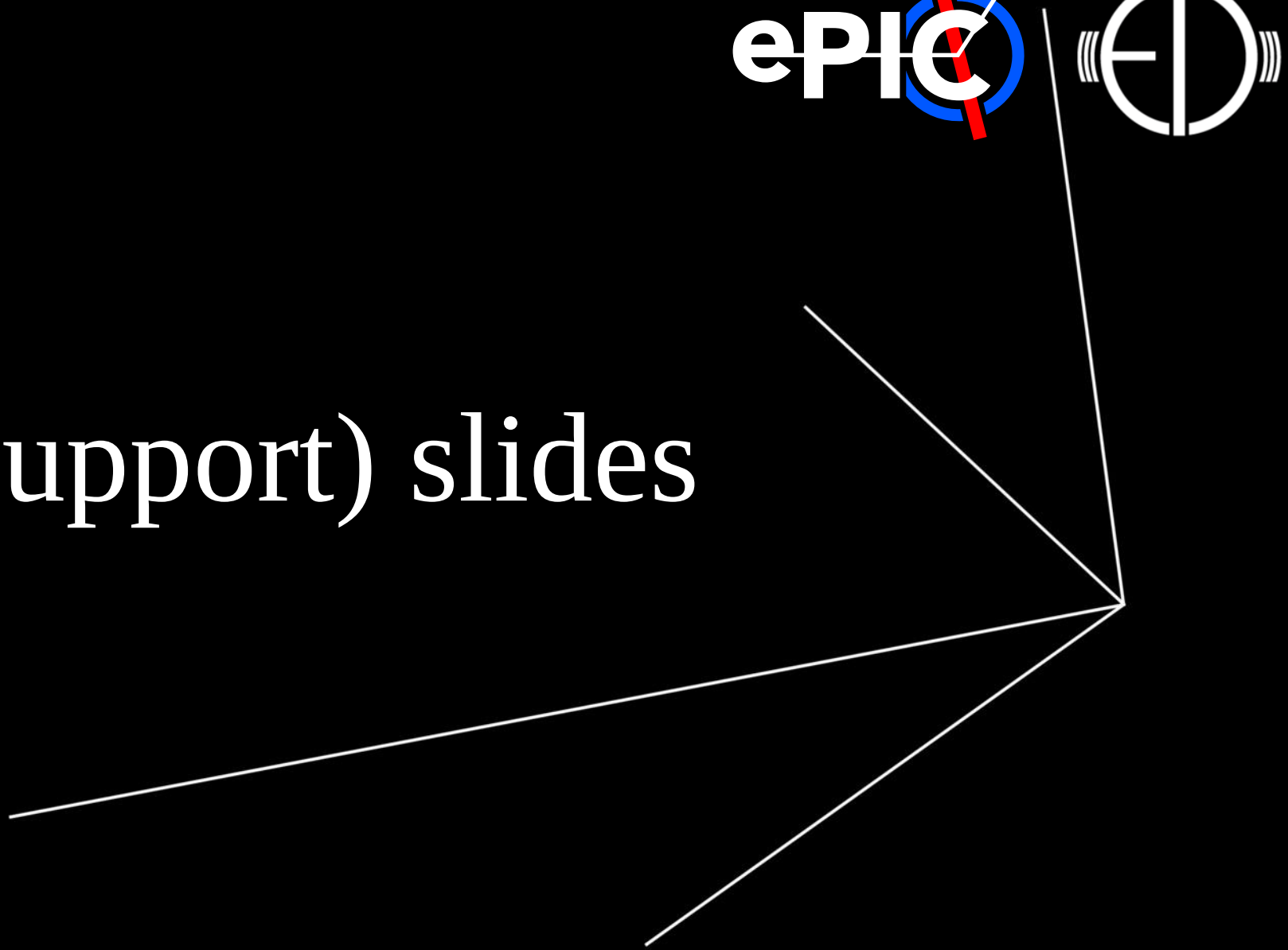
Additional (support) slides



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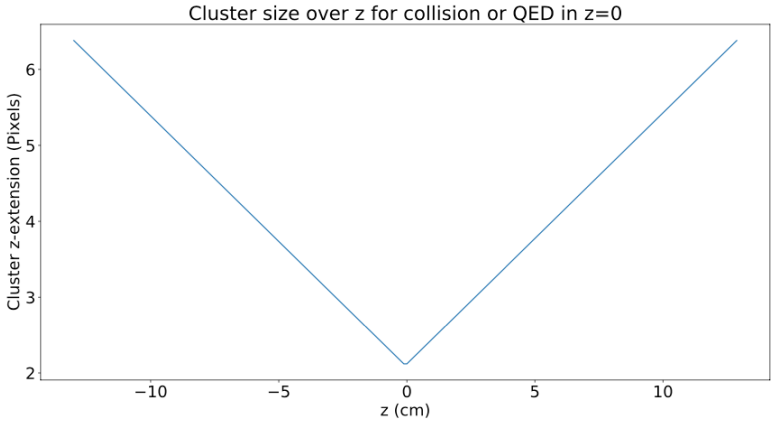
Readout

Simulation parameters	Value	Unit	Conditions
Particle Rates			
Average Pb-Pb Interaction Rate	164	kHz	
Particle flux (Hadronic)	2.55	MHz cm^{-2}	z=0 cm, all centralities.
Particle flux (QED)	3.20	MHz cm^{-2}	z=0 cm.
Total particle flux	5.75	MHz cm^{-2}	z=0 cm, all centralities.
Geometry, timing, encoding, data transfer capacity			
Pixel dimensions	20.8 × 22.8	µm × µm	
Tile pixel array size	442 × 156		
Pixels per Tile	68952		
Sensitive Area of the tile	0.327	cm^2	
Tiles per segment	144		
Readout regions per tile	3 or 4		
Frame Interval Duration (FD)	2 or 5	µs	
Minimum average cluster size	2.1		$\Delta z = 0$ cm, fig. 3.41.
Maximum average cluster size	6.3		$\Delta z = 13.5$ cm, fig. 3.41.
Pixel hit encoding time	25	ns	
Bits per pixel hit	16	bit	
Capacity of tile link	160	Mbit s^{-1}	
Aggregated capacity (Segment)	23.04	Gbit s^{-1}	



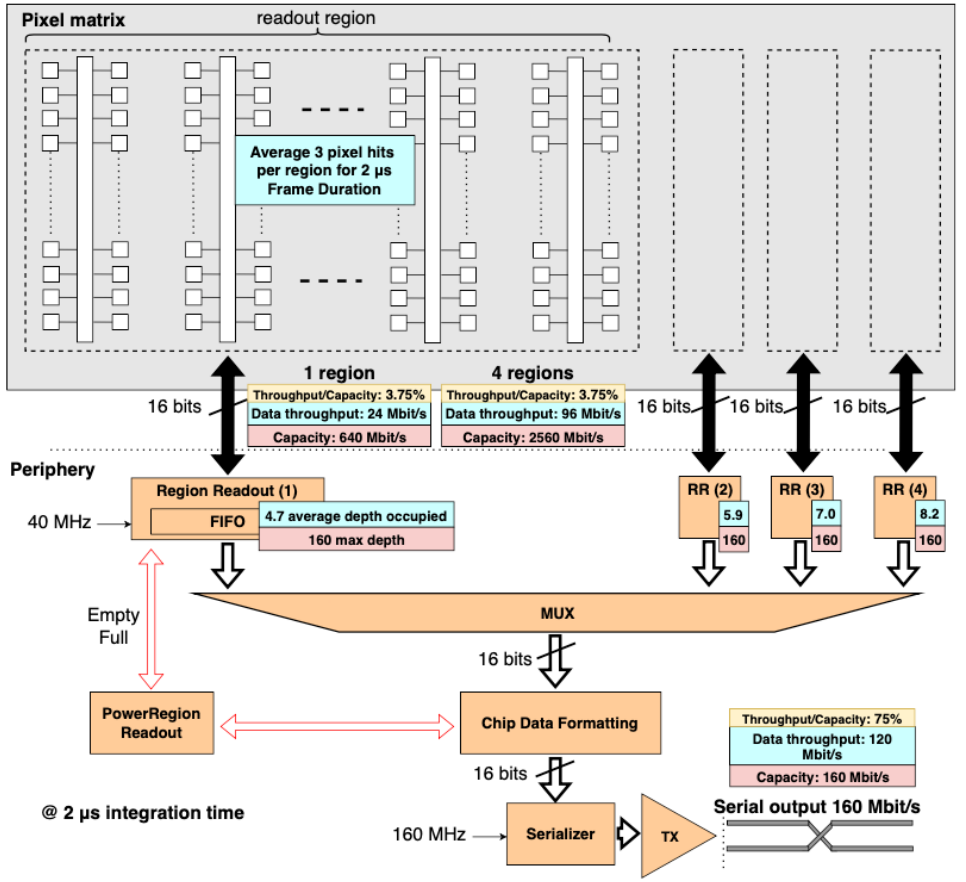
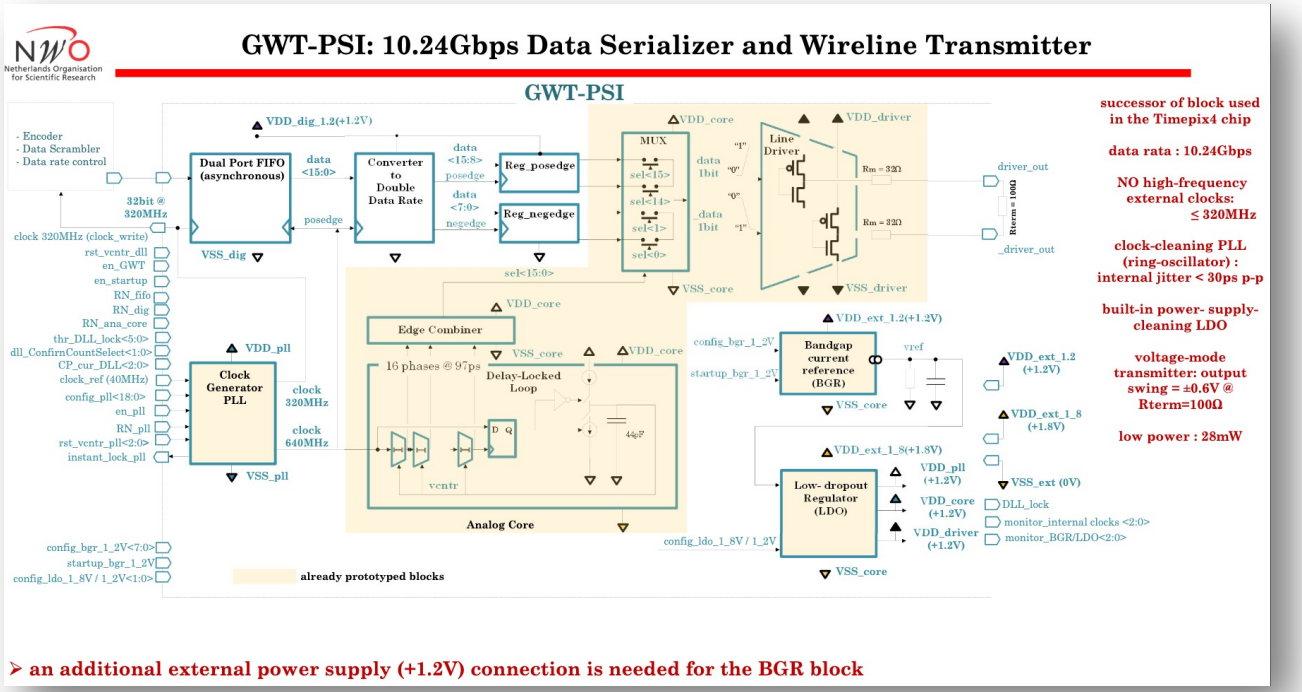
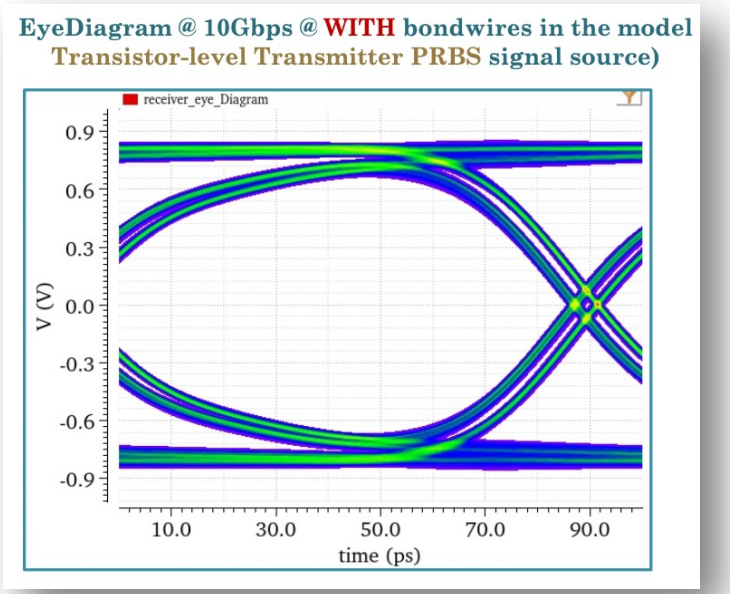


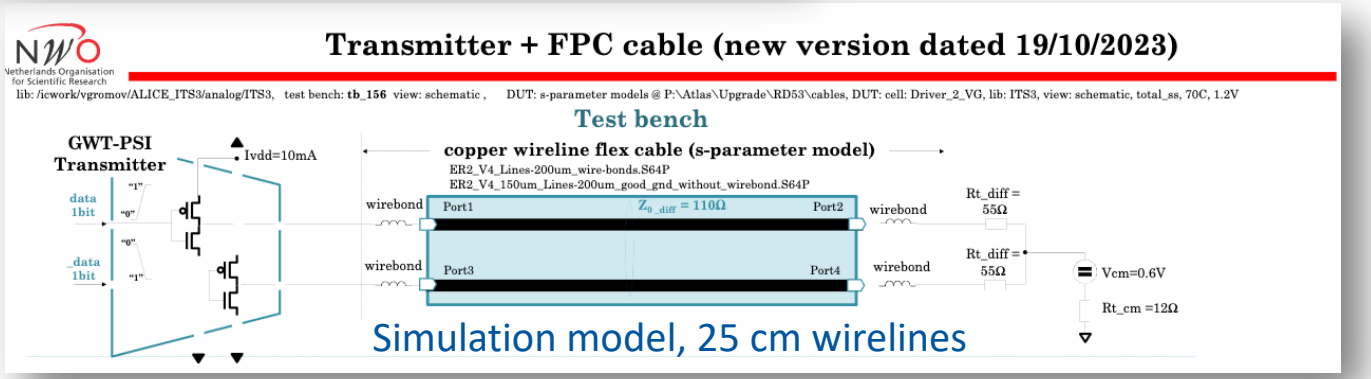
Figure 3.40: Block diagram of the peripheral readout of one tile. The illustration assumes four readout regions, FIFOs of 160 words depth and an integration time of 2 µs. The values of occupancy and data throughput of the internal busses reported on the diagram are results from the simulation runs.

Serializers





Circuit without pre-emphasis



Simulation model, 25 cm wirelines