20231205
M.Borri

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Flexible Printed Circuits (FPCs) for ePIC-SVT: An initial configuration

WP3: Electrical interfaces

Objective & outline

Objective:

To capture an initial configuration of the Flexible Printed Circuits (FPCs), based on the existing concepts of staves and disks.

The initial configuration will follow the iterations related to the evolutionary development of the SVT.

Outline:

- Material budget
- Stave and disk configurations
- Bill of materials
- Layout
- Conclusions

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Material budget

IB	r [mm]	l [mm]	X/X0 %
L0	36	270	0.05
L1	48	270	0.05
L2	120	270	0.05

LAS T5

BARREL	r [mm]	l [mm]	X/X0 %
Layer 3	270	540	0.25
Layer 4	420	840	0.55

LAS T5

DISKS	+z [mm]	-z [mm]	r_out [mm]	X/X0 %
Disk 0	250	-250	240	0.25
Disk 1	450	-450	420	0.25
Disk 2	700	-650	420	0.25
Disk 3	1000	-850	420	0.25
Disk 4	1350	-1050	420	0.25

J. Glover
Current and future tracking and vertexing detectors
7 Nov 2023

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B Abelev et al and The ALICE Collaboration 2014 J. Phys. G: Nucl. Part. Phys. 41 087002

Table 4.1: Estimated contributions of the Inner Layer Stave to the material budget.

Stave element	Component	Material	Thickness (μm)	X_0 (cm)	X_0 (%)
HIC	FPC Metal layers	Aluminium	50	8.896	0.056
	FPC Insulating layers	Polyimide	100	28.41	0.035
	Pixel Chip	Silicon	50	9.369	0.053
Cold Plate		Carbon fleece	40	106.80	0.004
		Carbon paper	30	26.56	0.011
	Cooling tube wall	Polyimide	25	28.41	0.003
	Cooling fluid	Water		35.76	0.032
	Carbon plate	Carbon fibre	70	26.08	0.027
	Glue	Eccobond 45	100	44.37	0.023
Space Frame		Carbon rowing			0.018
Total					0.262

Target material budget

ITS2 IB stave length ~270mm, width ~1.5cm, ALPIDE PWR <40m W/cm2

FPC breakdown from Di Mauro and o.b.o.t.A. Collaboration
Nuclear Inst. and Methods in Physics Research, A 936 (2019) 625–629

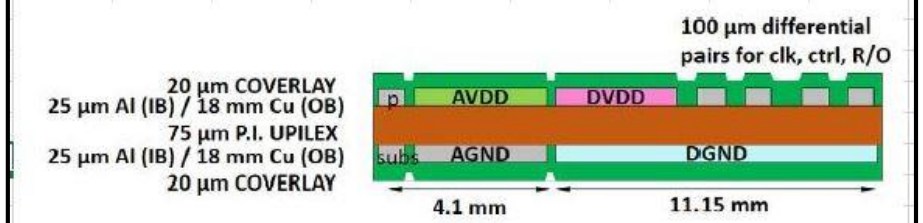


Fig. 4. Schematic cross section of the IB FPC (vias are not represented).

Two layers FPC, w Al tracks, w impedance matched tracks

Material budget & impedance matching

FPC breakdown from Di Mauro and o.b.o.t.A. Collaboration
Nuclear Inst. and Methods in Physics Research, A 936 (2019) 625–629

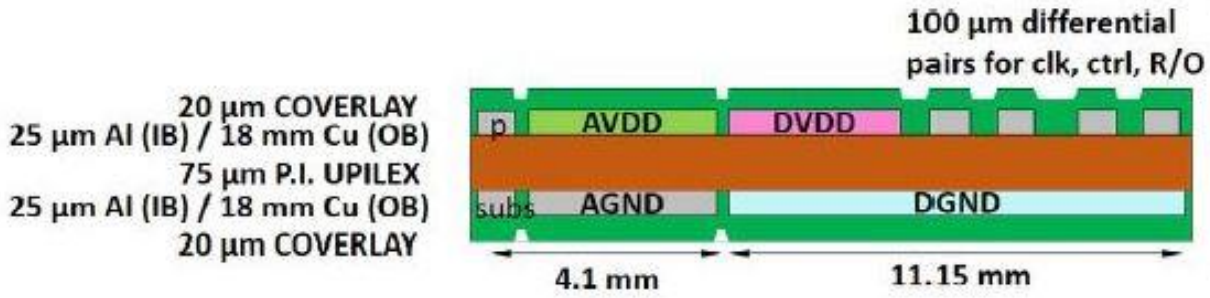
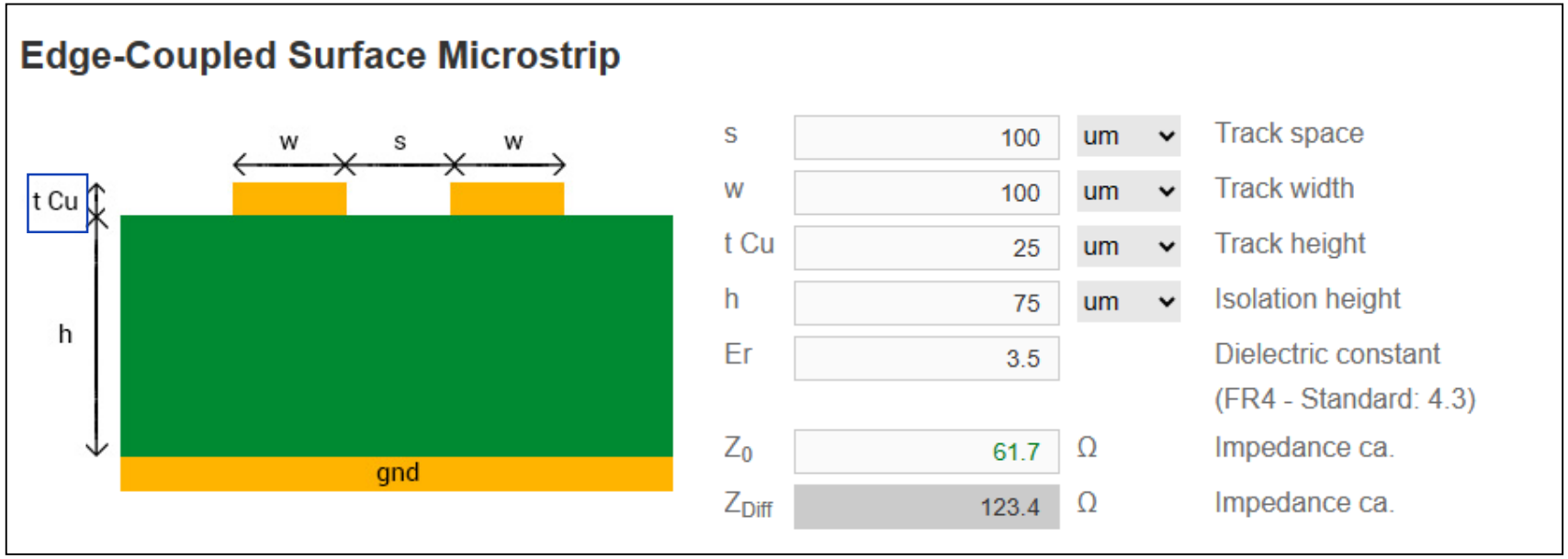


Fig. 4. Schematic cross section of the IB FPC (vias are not represented).

Sanity check on impedance

OK ~100 ohm impedance
for 100um diff pairs



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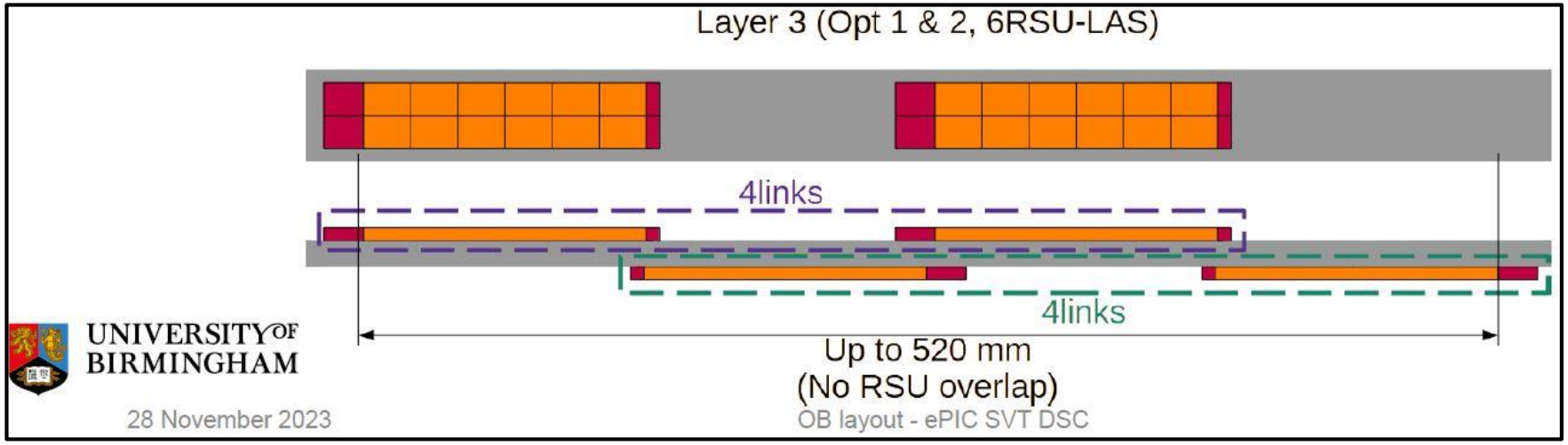
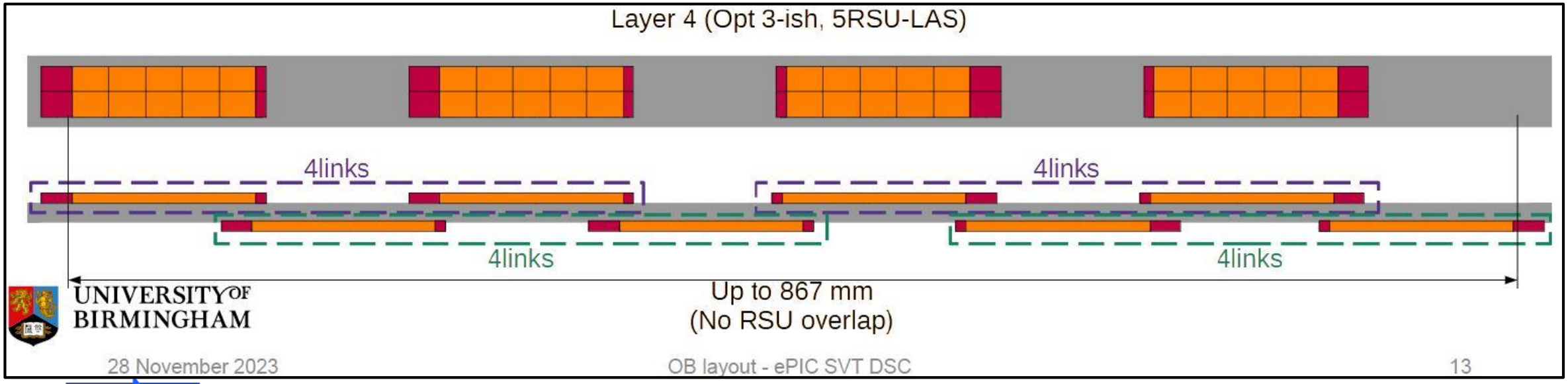
Stave configuration

Credit J.Glover



Assumptions:

- Sensor mounted on top and bottom of cold plate;
- LEC overlaps REC;
- Services from left and right sides of staves



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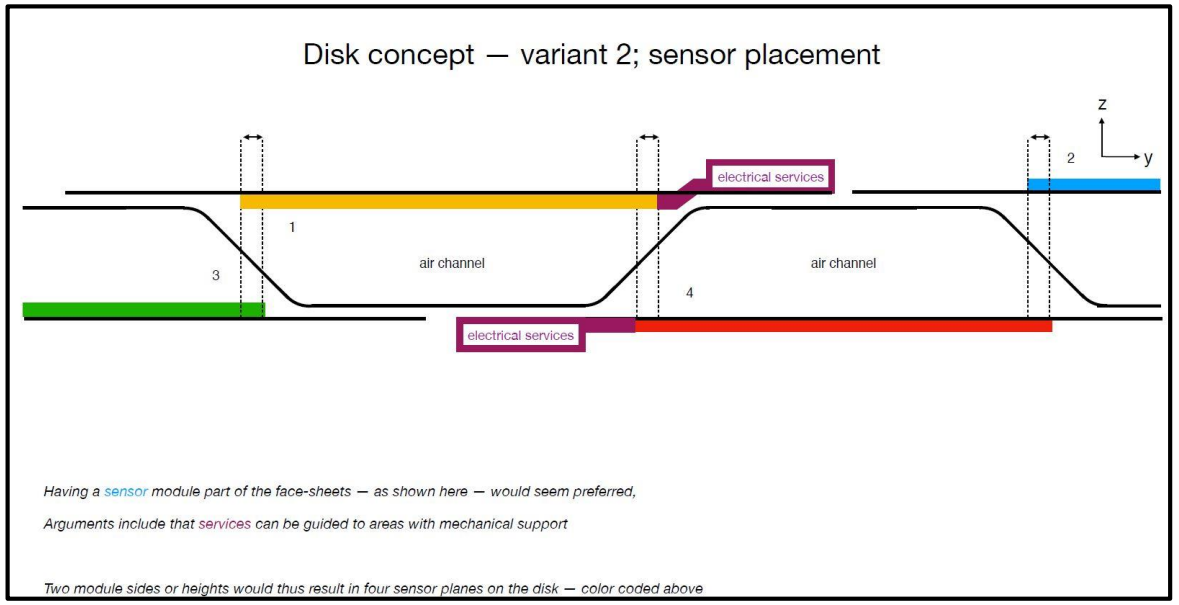
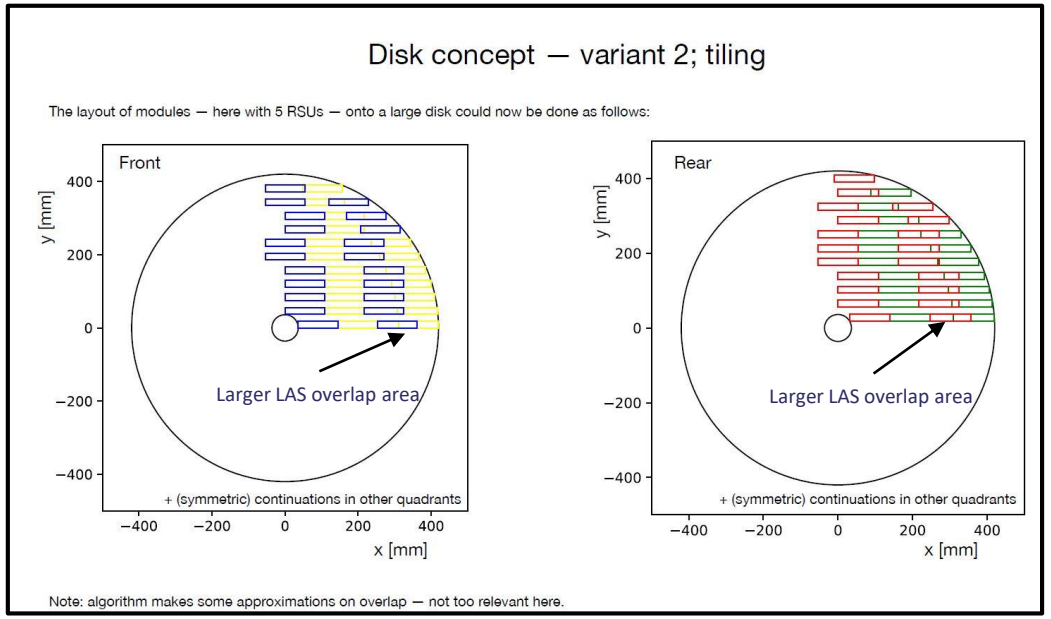
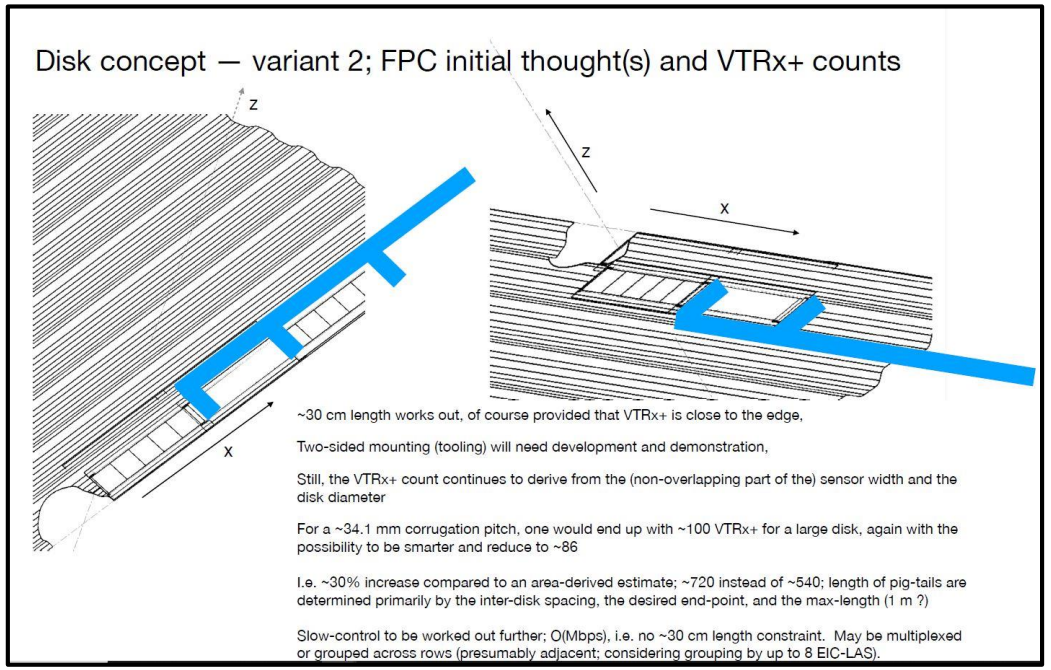
Disk configuration

Credit E.Sichtermann, N.Apadula







Note:
Only T5 LAS considered for tiling disks;

LEC overlaps REC like in barrels to increase hermeticity;

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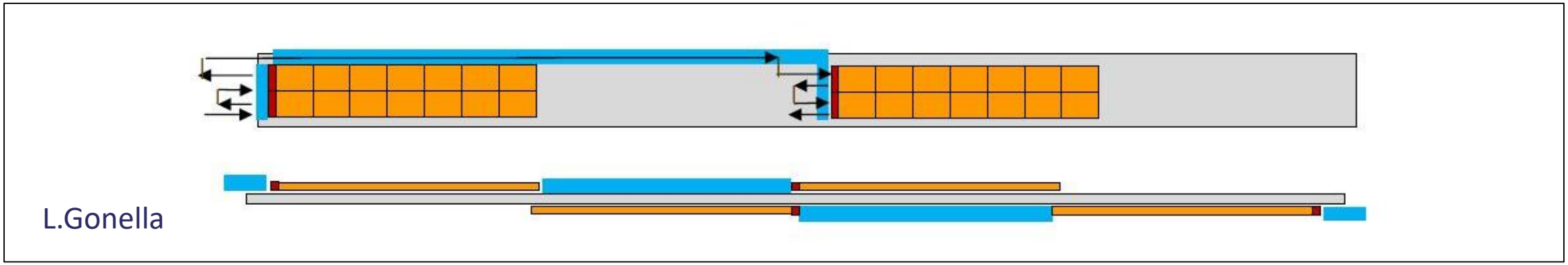
Case study: OB L4 half stave



OB L4 half stave:

A sequence of 4 T5 LAS, the longest chain of sensors in SVT

This layout is similar and inspired to that of disks.

BOM (so far)

sLDO: notes

"My datasheet

Pin-out description

SLDO	Signal		
	I_in	input	2.5 A (or 1.7 A) (Id+ Ia) worst case scenario
	I_out	input	2.5 A (or 1.7 A) (Id+ Ia) worst case scenario
	Vout	output	4 options: SDVDD/SDVSS = 1.2 to 1.32 V (services) (227mA) GAVDD/GAVSS = 1.2 to 1.32 V (global analogue) (540mA) GDVDD/GDVSS = 1.2 to 1.32 V (global digital) (1369mA) TXVDD/TXVSS = 1.8 V (serialisers) (200mA)
			Note: PSUB -1.2 to 0 V not included

Physical layout

I_in		I_out
		Vout
foot print	2mmx2mm	

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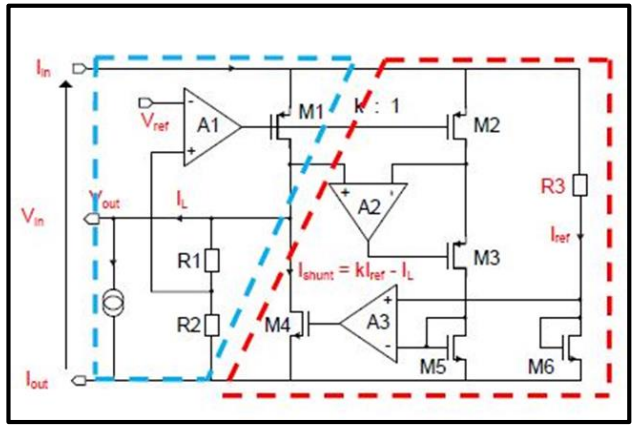
Assuming 4 sLDOs need per LAS

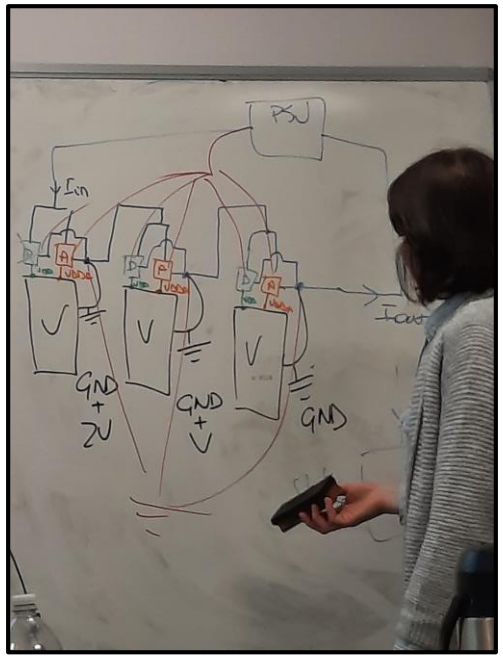


Power Domains and Currents

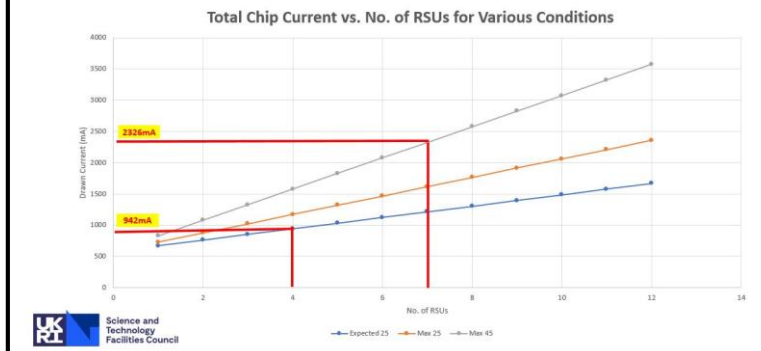
Supply purpose	Nets	Voltage [V]	Current [mA]	Pads on LEC	Pads on REC
Services	SDVDD-SDVSS	1.2 to 1.32	227	Yes	Yes
Global analog	GAVDD-GAVSS	1.2 to 1.32	540	Yes	Yes
Global digital	GDVDD-GDVSS	1.2 to 1.32	1369	Yes	Yes
Serializers	TXVDD-TXVSS	1.8	200	Yes	No
Substrate bias	PSUB	−1.2 to 0			

NEW, EXTRA PADS? THERE IS NO REFERENCE TO THESE IN PREVIOUS LEC CONNECTION SCHEMES.

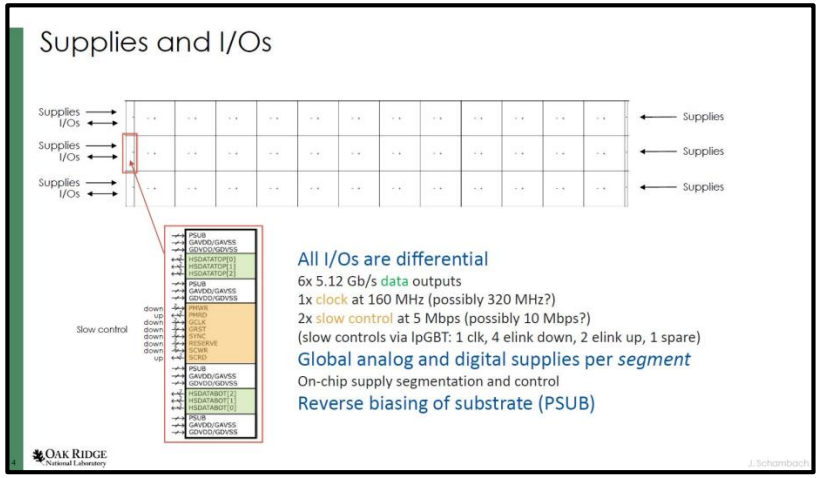
Table 3.11: Power domains of one sensor segment. The substrate bias is common to all the segments composing a sensor. The nominal operating voltage are referred to the potential of the GAVSS input net. The input currents are obtained assuming the maximum estimated power consumption of the LEC and RSU circuits at 25 °C.

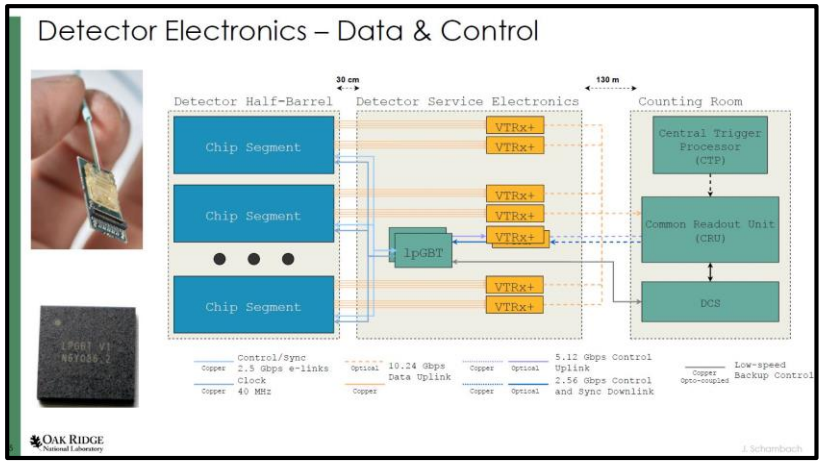


ITS3 – Power Density



Mux/Demux IC: notes





Assuming 1 Mux/Demux IC need per LAS

Assuming that it is Pwr'd via one of the existing sLDOs

"My datasheet"

Pin-out description

slowCtrlChip	S1down+	Input	down	1 CONTROL link (down) carries MUX'd: (PMWR, SCWR, RST, SYNC)
	S1down-	Input	down	
	S2down+	Input	down	1 link for GCLK Assuming that global clock gets buffered
	S2down-	Input	down	
	S1up+	Output	up	1 Ctrl link (up) carries MUX'd PMRD(up) and SCRD(up)
	S1up-	Output	up	
	S_GLCK+	Output	down	160MHz (or 320MHz)
	S_GLCK-	Output	down	
	S_PMWR+	Output	down	5Mbps (10Mbps)
	S_PMWR-	Output	down	
	S_PMRD+	Input	up	5Mbps (10Mbps)
	S_PMRD-	Input	up	
	S_SCWR+	Output	down	5Mbps (10Mbps)
	S_SCWR-	Output	down	
	S_SCRD+	Input	up	5Mbps (10Mbps)
	S_SCRD-	Input	up	
	S_GRST+	Output	down	
	S_GRST-	Output	down	
	G_SYNC+	Output	down	
	G_SYNC-	Output	down	
	G_RESERVE+	N/A	N/A	
	G_RESERVE-	N/A	N/A	
	VDD	Input		supplied locally from sLDO multiple pads Supply voltage and power?
	GND	Input		

Physical layout

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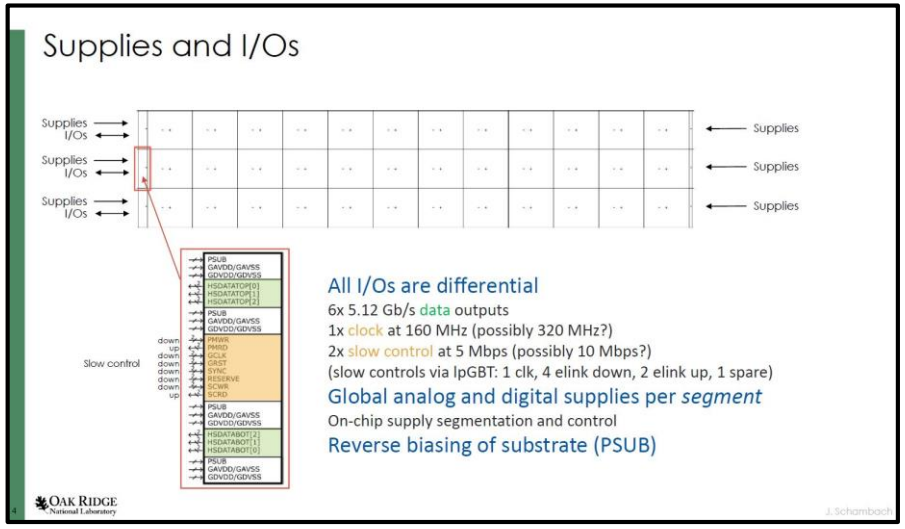
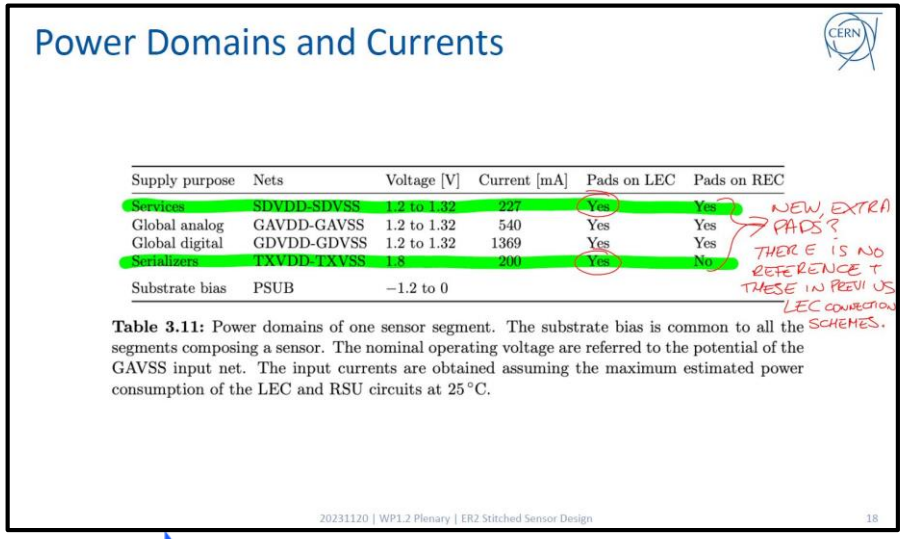
LAS: notes



Assuming LAS is T5 only



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"My datasheet"

Pin-out description

LAS	S_GLCK+	Input	down	160MHz (or 320MHz)	Clk
	S_GLCK-	Input	down		
	S_PMWR+	Input	down	5Mbps (10Mbps)	Slow ctrl
	S_PMWR-	Input	down		
	S_PMRD+	Output	up	5Mbps (10Mbps)	
	S_PMRD-	Output	up		
	S_SCWR+	Input	down	5Mbps (10Mbps)	
	S_SCWR-	Input	down		
	S_SCRD+	Output	up	5Mbps (10Mbps)	
	S_SCRD-	Output	up		
	S_GRST+	Input	down		
	S_GRST-	Input	down		
	G_SYNC+	Input	down		
	G_SYNC-	Input	down		
	G_RESERVE+	N/A			
	G_RESERVE-	N/A			
	HSDATA+	Output	up	5.12 Gb/s	Data
	HSDATA-	Output	up		
	SDVDD	Input		1.2 to 1.32 V (services) (227mA)	Pwr
	SDVSS	Input			
	GAVDDS	Input		1.2 to 1.32 V (global analogue) (540mA)	
	GAVSS	Input			
	GDVDD	Input		1.2 to 1.32 V (global digital) (1369mA)	
	GDVSS	Input			
	TXVDD	Input		1.8 V (serialisers) (200mA)	
	TXVSS	Input			
	PSUB	Input			Sensor bias

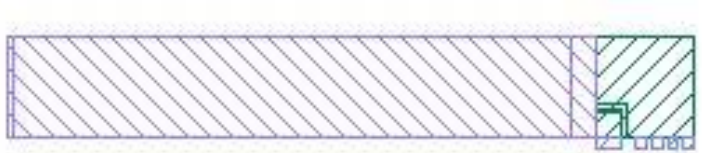
Physical layout

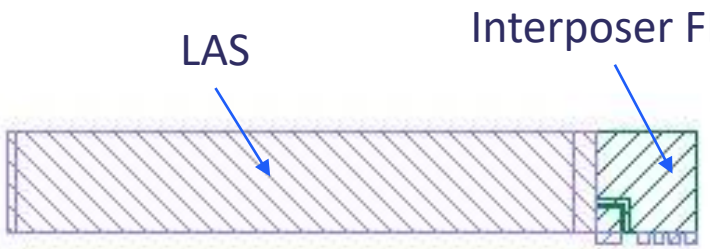
	l (mm)	w (mm)
RSU	21.666	19.564
LEC	4.5	19.564
REC	1.5	19.564
T5 LAS	114.33	19.564
T6 LAS	135.996	19.564

Layout

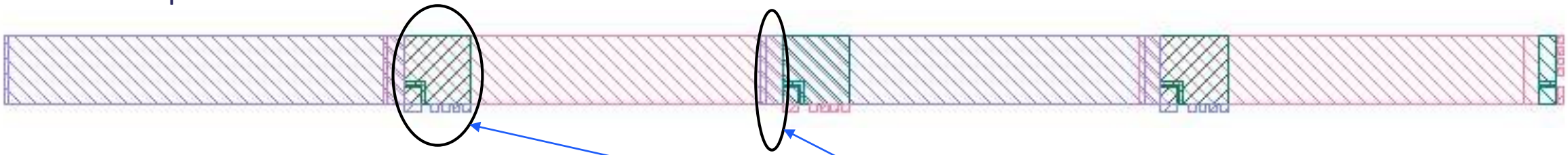
Layout into

Sensors: top only





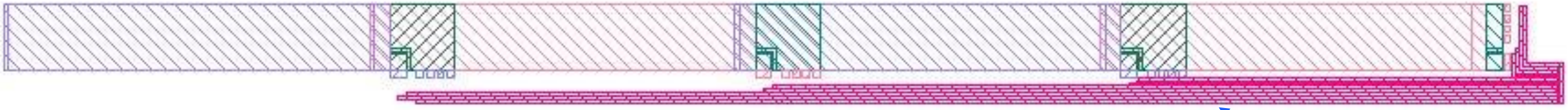
Sensors: top and bottom



High material budget region:

- 2 LAS overlap
- 1 LAS + interposer FPC

Sensors: top and bottom and common bus FPC



Common bus FPC
(supported by CFF)

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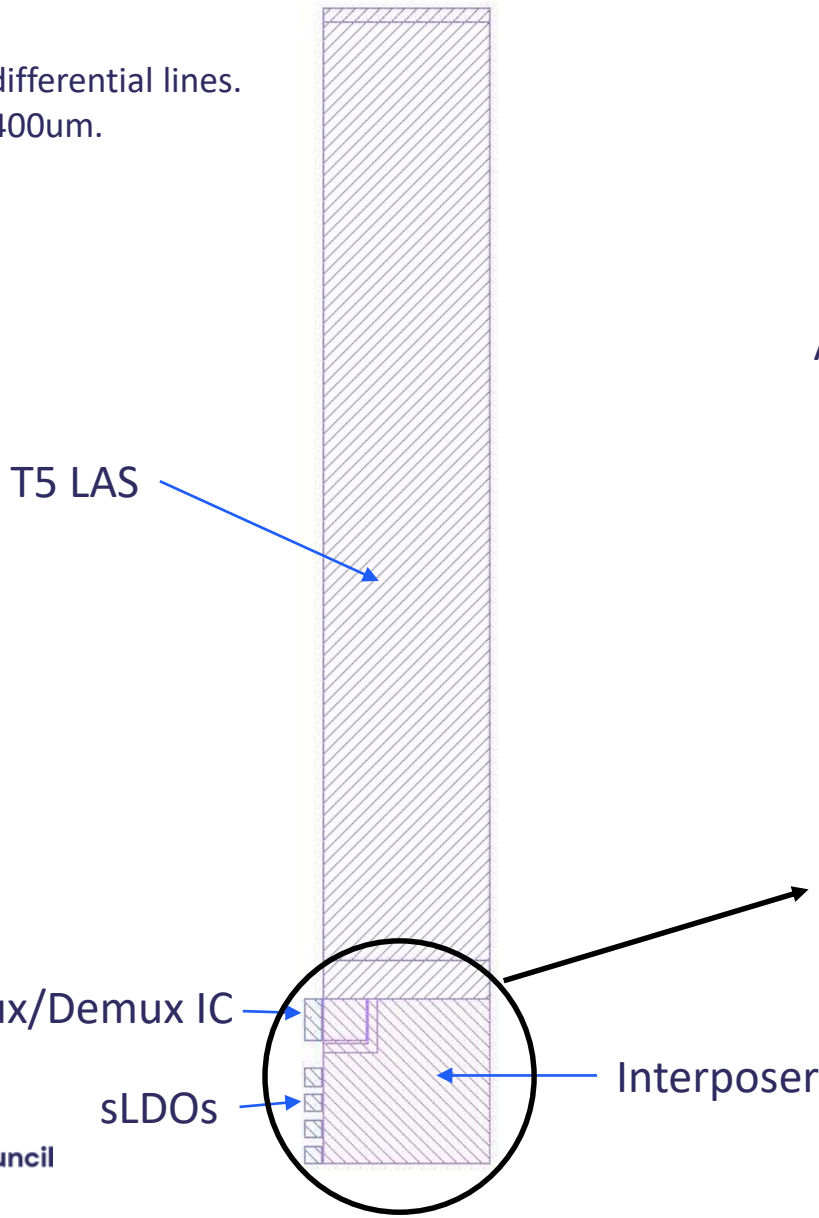
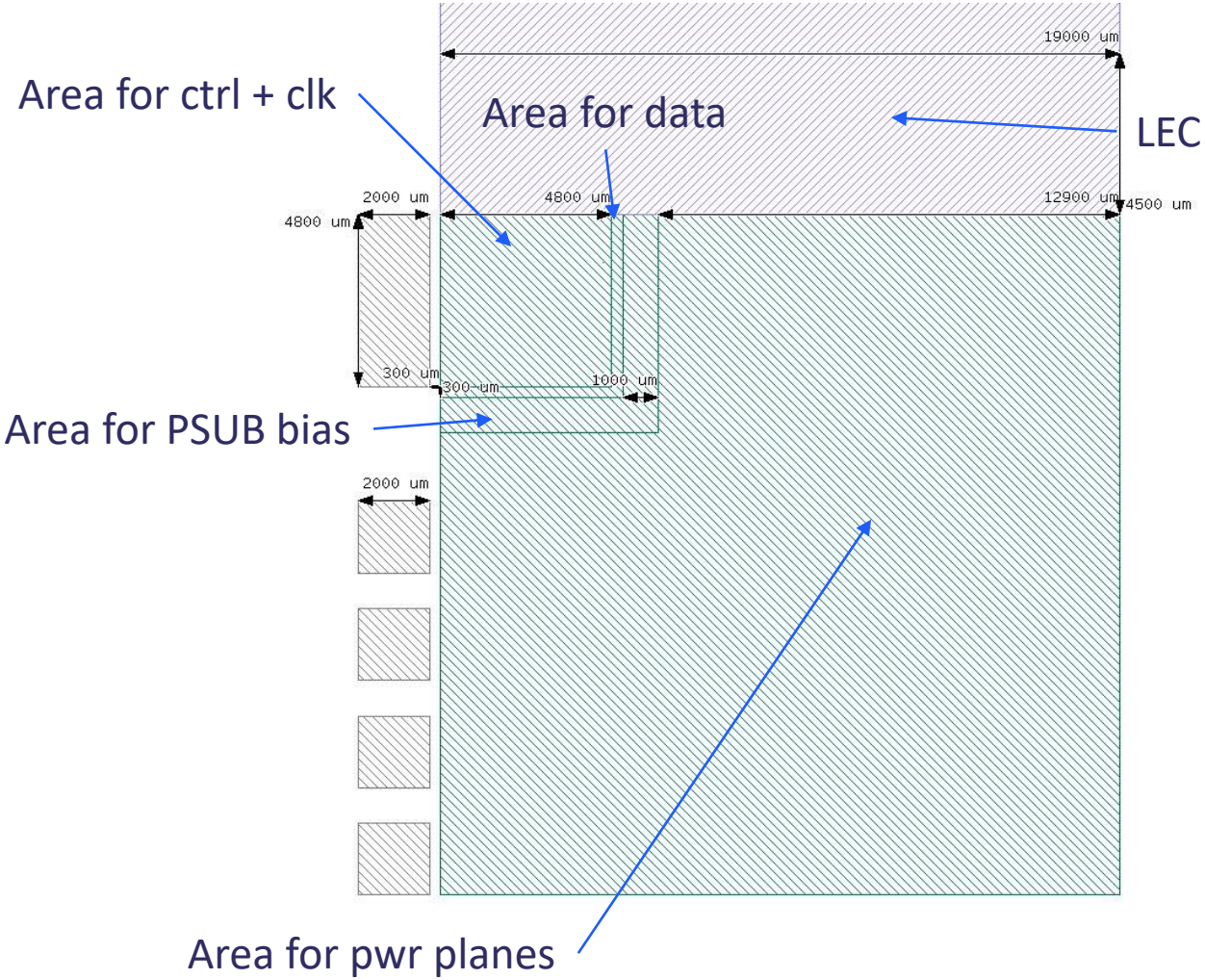
Interposer FPC

Note: to redo, bug on pitch of differential lines.
300um considered, instead of 400um.





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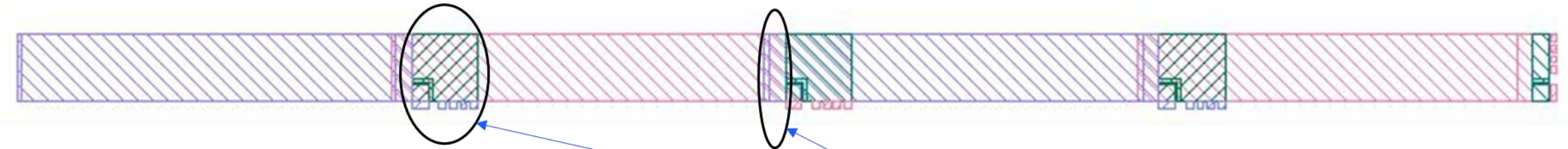
Interposer FPC: material budget

	Components	Thickness (um)	Material	X0 (cm)	X0 (%)	Comment
HIC	FPC metal layers	50	Al	8.897	0.056	25um/layer x 2 layers = 50um
	FPC insulating layers 1	75	UPILEX-S75	28.57	0.026	UPILEX-S75 is a type of polyimide
	FPC insulating layers 2	40	Coverlay	28.57	0.014	20um/layer x 2 layers = 40um, coverlay is polyimide
	Pixel Chip	50	Si	9.37	0.053	
	Glue	50	Araldite2011	39.07	0.0128	ATLAS assumes phenol epoxy C6 H6 O
Total (FPC + Pixel chip + glue)					0.163	
Total w/o glue (FPC + Pixel chip)					0.150	
Total FPC only					0.096	consider Si interposer as option: Si 50um thin equates to X0 (%) 0.053. N.B. ~50% saving in material budget



High material budget region:

- 2 LAS overlap
- 1 LAS + interposer FPC

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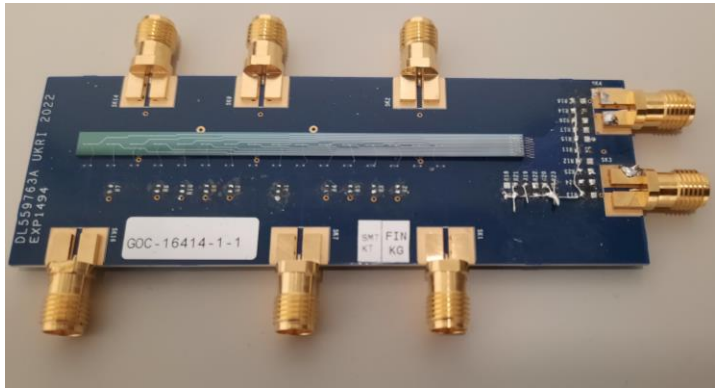
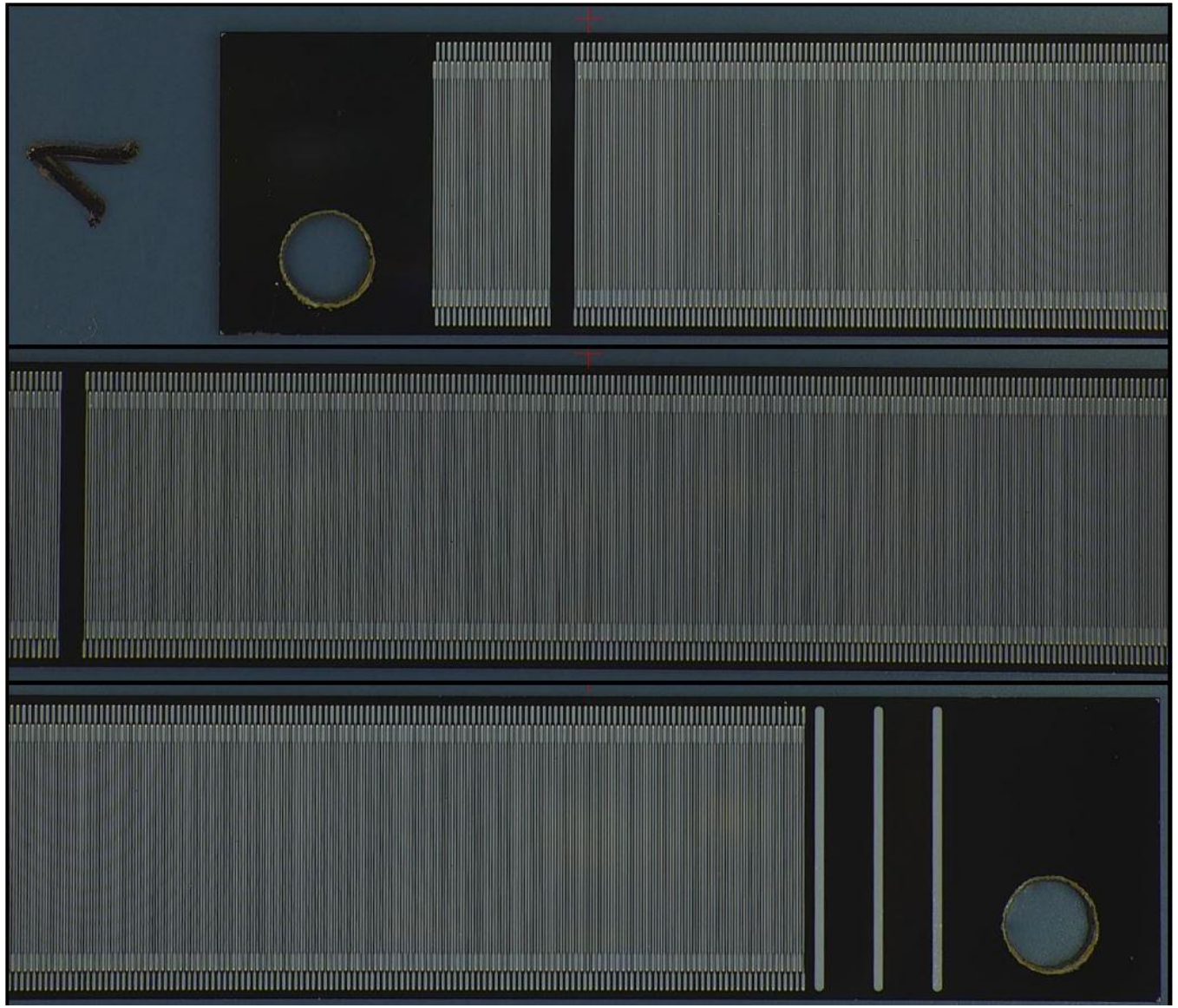
Si interposer (1 layer): examples





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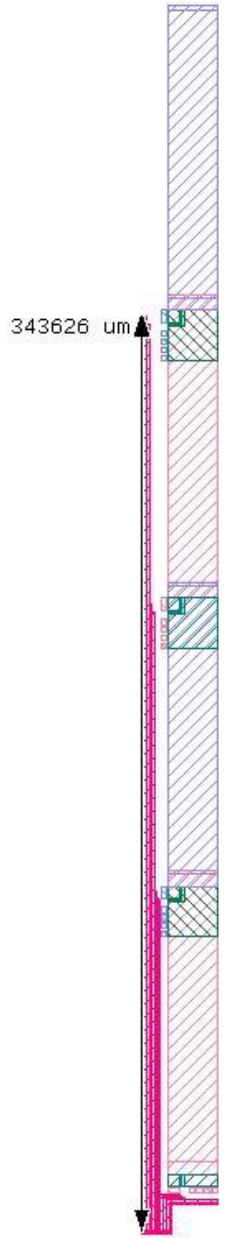
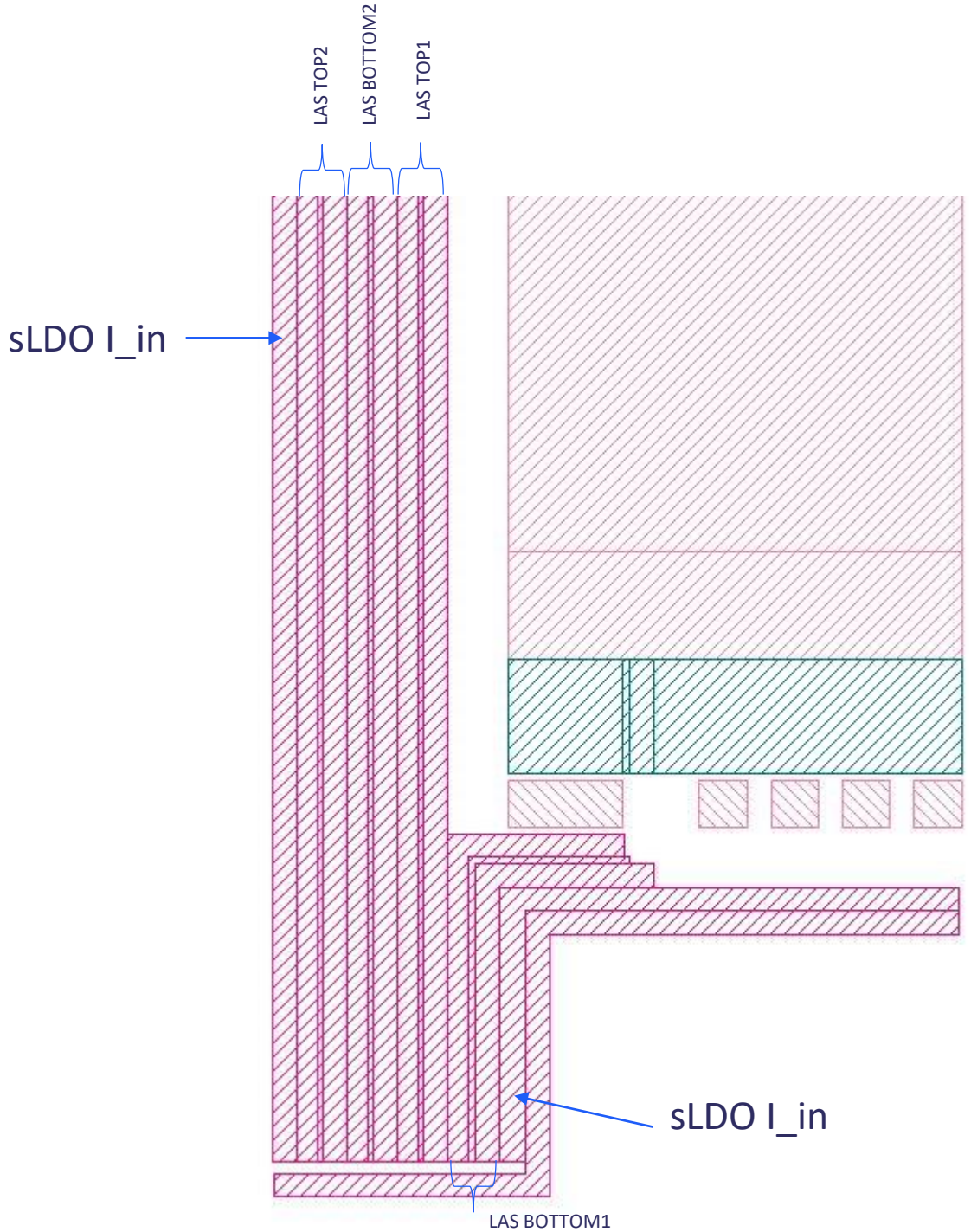
Common bus FPC





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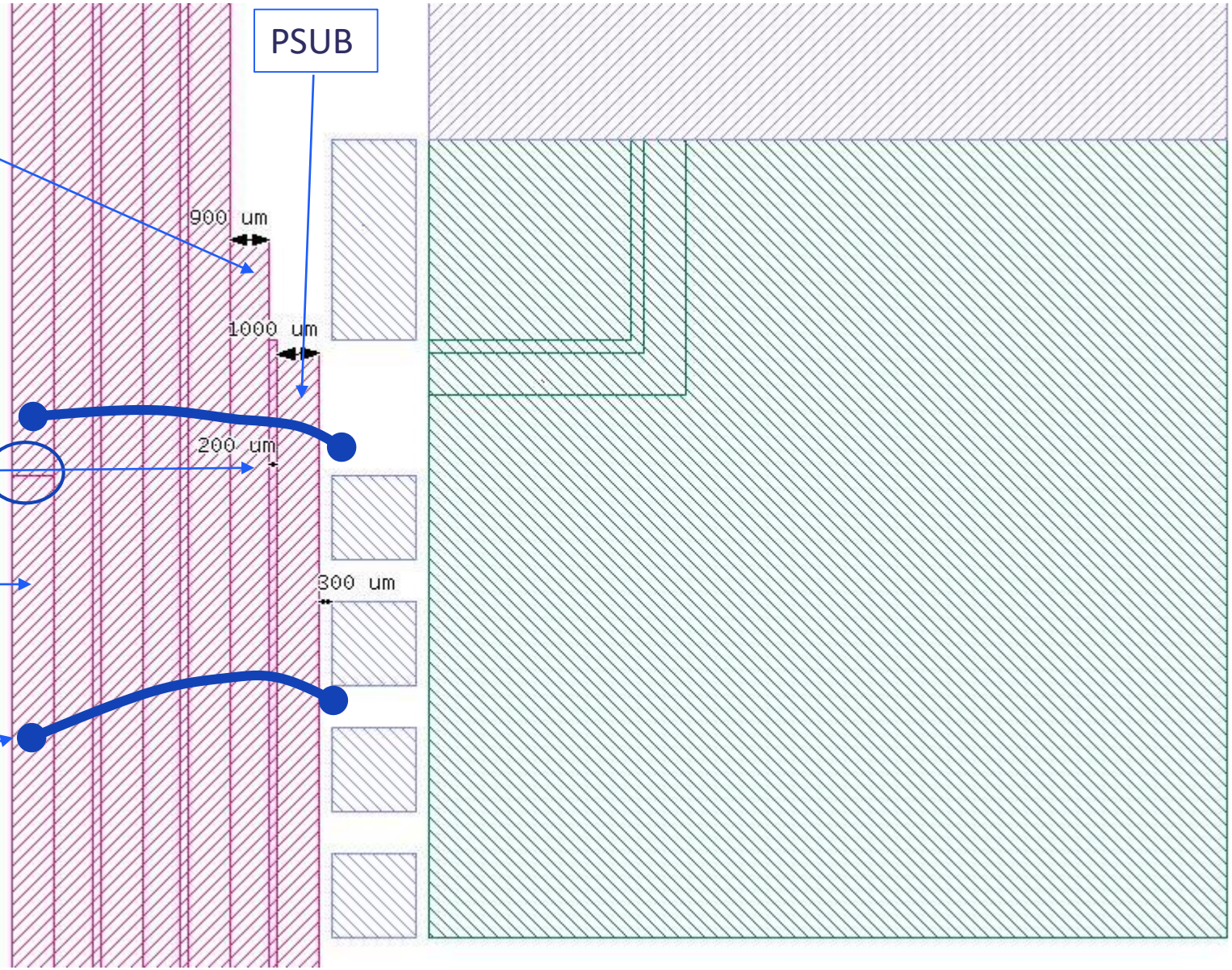
Common bus FPC



3 differential lines:
S1down; S2down; S1up;
(bug on pitch of differential lines.
300um considered, instead of >400um.)

1 data line
(bug: should be >400um)

sLDO I_in

Solder bridge

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Conclusion

- An initial FPC layout has been captured.
- L4 half stave configuration was used a case study, representative for disks and staves.
- Improvements required e.g.
  - Definition of LAS layout on staves.

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Thank you

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