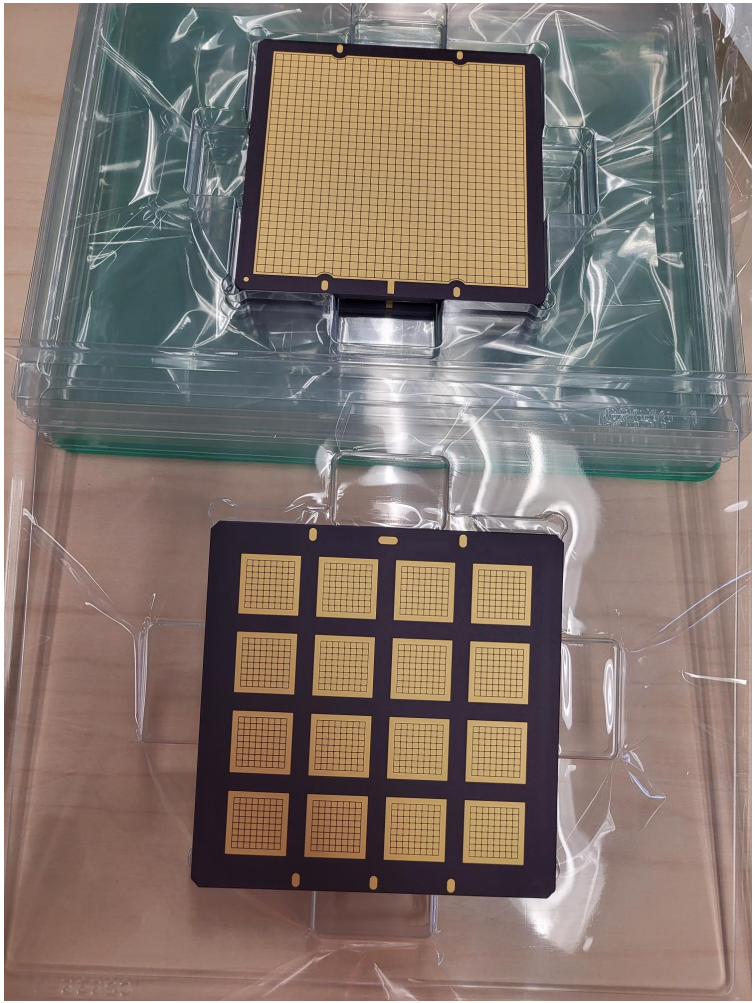
HRPPD manufacturing

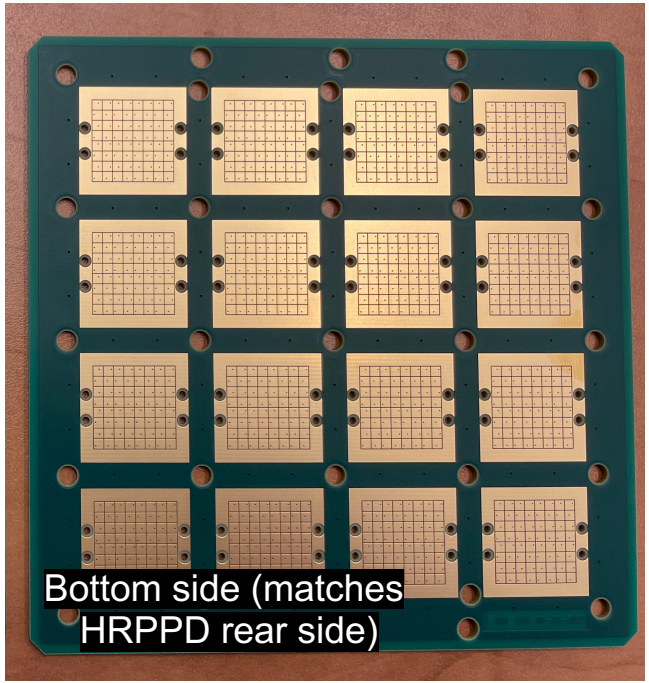
- All ten Kyocera anodes received by now
  - Should suffice for five HRPPDs assuming >50% yield
- Flatness tests are very encouraging: ~50 μm RMS
- Next steps of the QA procedure
  - Verify pad connectivity
  - Verify compatibility with the UHV
  - Verify C_d and trace resistivity (at BNL)

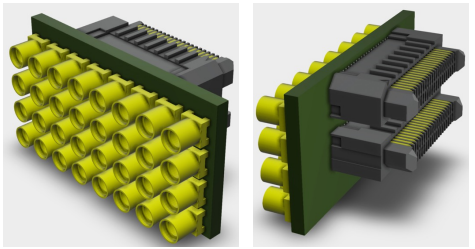
- ~~Right now, Incom is sealing a HRPPD based on the Techtra plate (then it gets sent to BNL)~~
- Samtec interposers are being shipped to BNL

- If everything goes smoothly, we should really see a first functional “EIC HRPPD” tile by Christmas

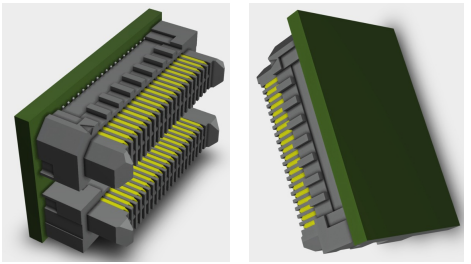


HRPPD passive interface #1





1x MMCX adapter



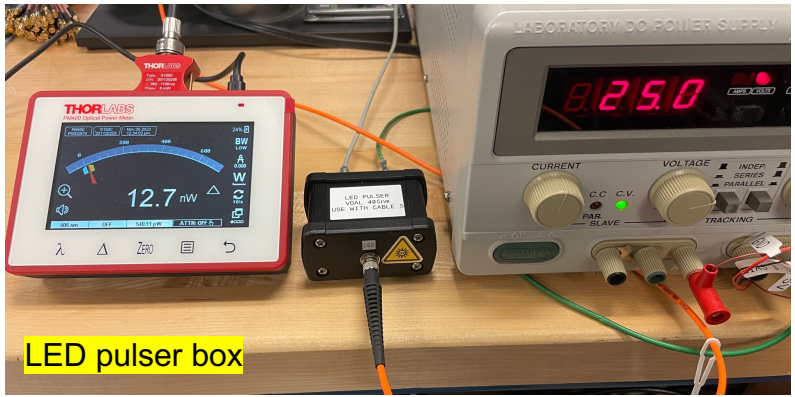
15x grounding caps

- The boards were received weeks ago, nothing new here
- Order for small Samtec -> MMCX adapter cards placed last week

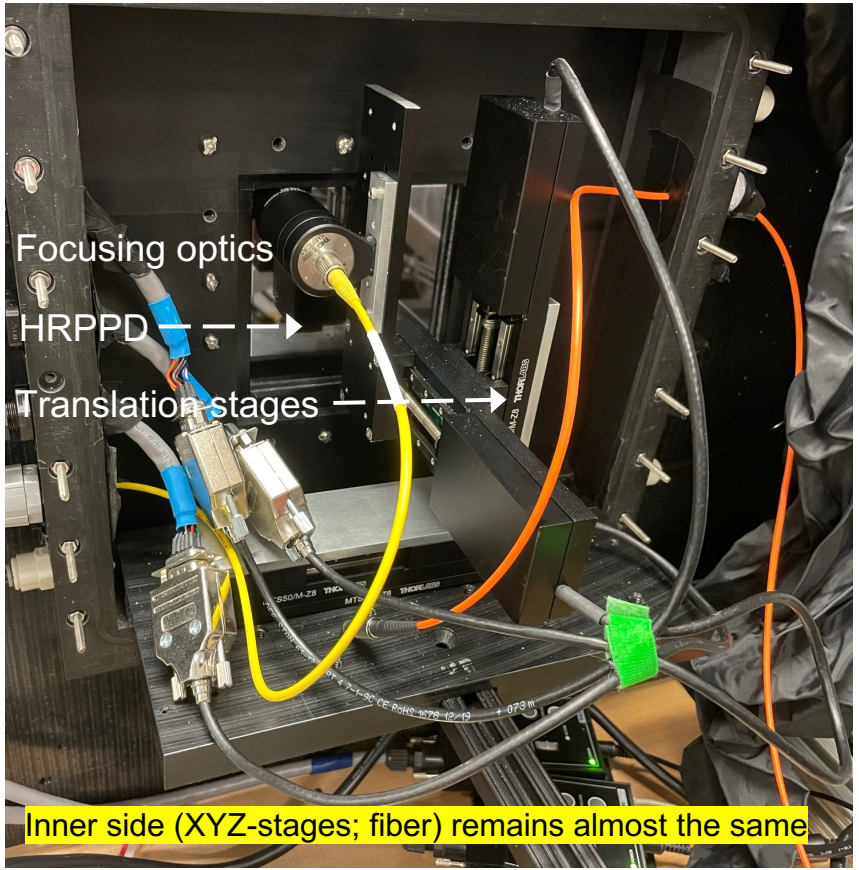
Mostly of interest for colleagues @ INFN, Glasgow, Jlab & Yale

HRPPD QA station @ BNL

- Consolidate all HRPPD-related equipment in a new lab space during this coming week
  - A slightly modified existing dark box
    - 2” XY-translation stages (>52mm travel) suffice to scan a single quadrant of a 104mm x 104mm HRPPD active area at a time, pixel by pixel
  - PiLas (picosecond) and Elmo (femtosecond) lasers
  - DAQ PC, NIM & VME crates, 8x V1742s
  - LED pulser box by Fernando [for QE measurements]



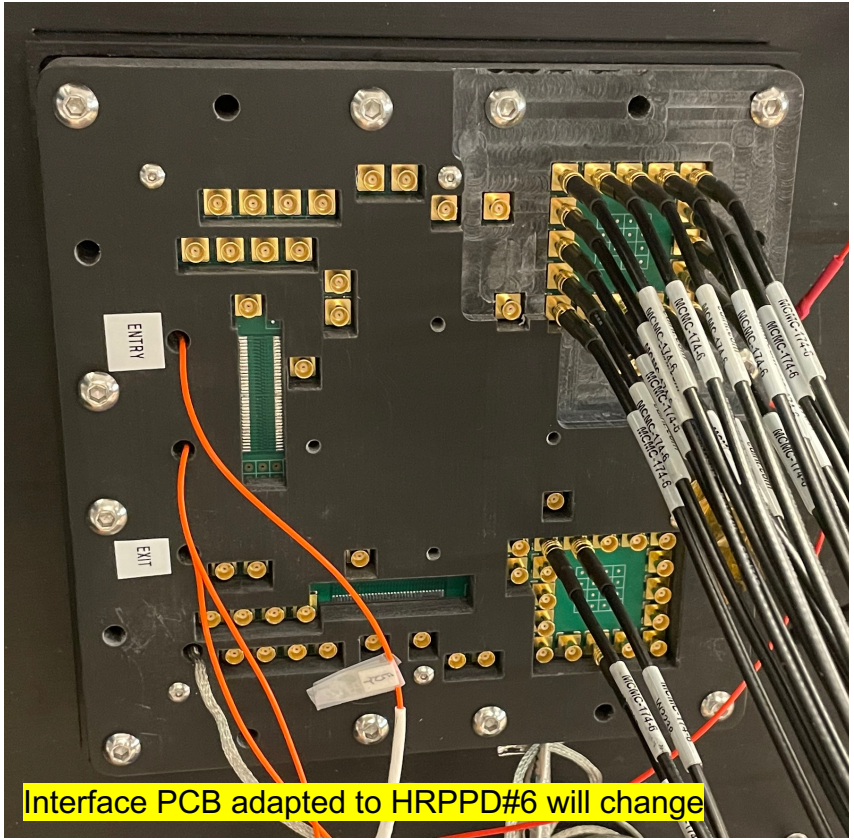
LED pulser box



Inner side (XYZ-stages; fiber) remains almost the same

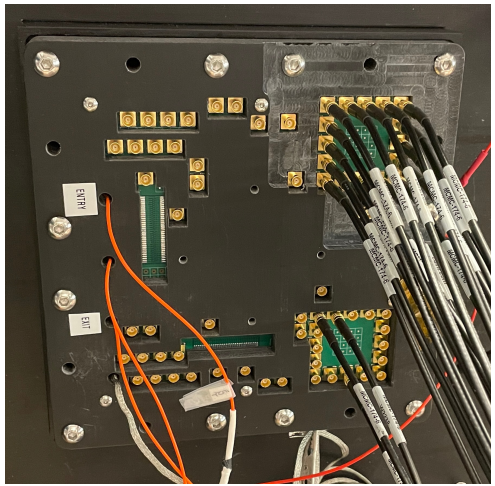
HRPPD QA station @ BNL

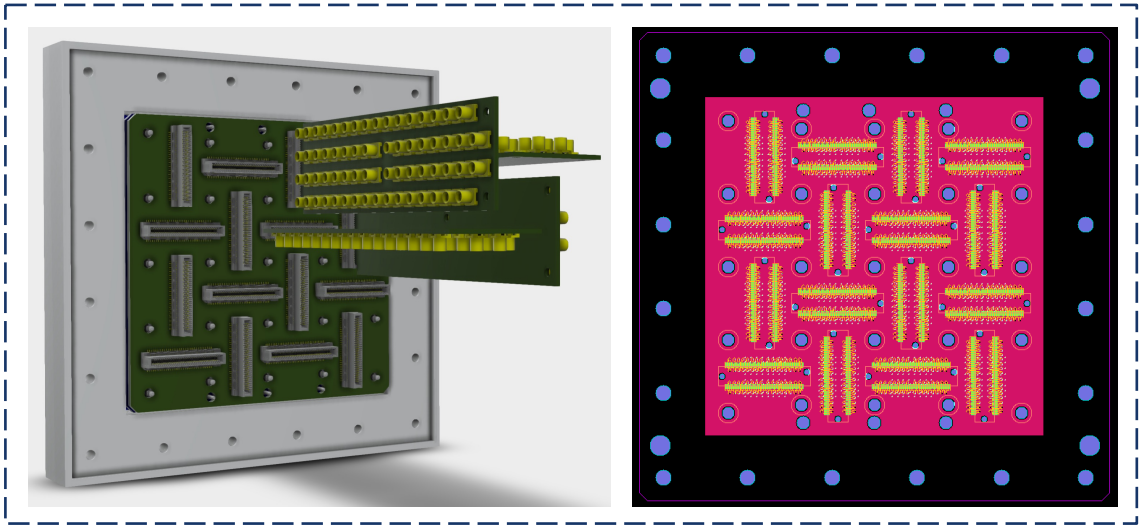
- Optimize data taking procedure
  - Synchronize DRS4 configuration with the XY-stage positioning (we are interested only in the illuminated pad data for these scans)
  - Read out only one of the 8x4 DRS4 chips and only the first 136 out of 1024 samples at 5GS/s (event size reduction from ~50kB to <2kB)
  - Then both the data volume and the CPU needs are manageable (assume 10^5 events per pixel @ ~5kHz, with ~5% single photon events)
- Plan to perform per pixel surface scans:
  - PDE (*in a counting mode*) & gain uniformity, timing
  - DCR in a self-triggering mode at 2.5GS/s (?)
  - QE via a direct photocathode current measurement
    - Consider adding a pair of NIST traceable photodiodes



Interface PCB adapted to HRPPD#6 will change

HRPPD passive interface #2



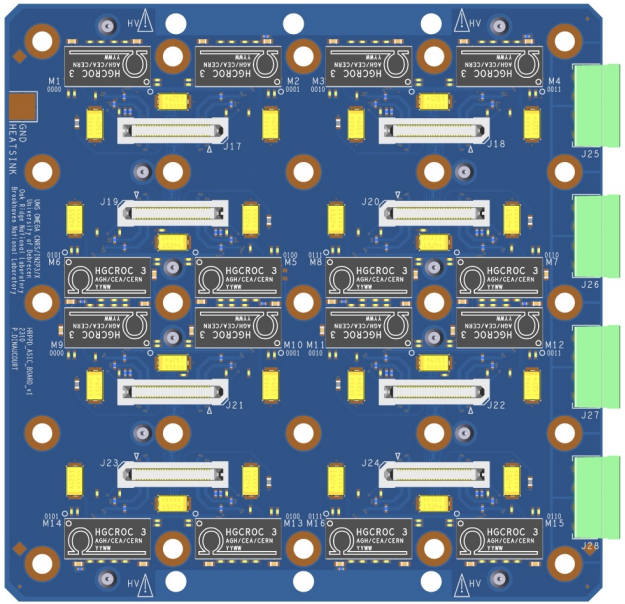


- Recycle existing 64ch MCX adapters, 3D printed clam shell enclosure, etc
- Order another custom PCB with a single 64ch Samtec MEC8 DV per 8x8 pixel field
  - Design is pretty much finalized; it is getting to become an HRPPD support; proceed with the PO shortly
- Equip one HRPPD quadrant at a time for a scan and shorten to ground all other connectors
- Do not touch either HRPPD (after the installation) or translation stages (ever)
  - Rather reposition the MCX adapters and the fiber inside of the dark box

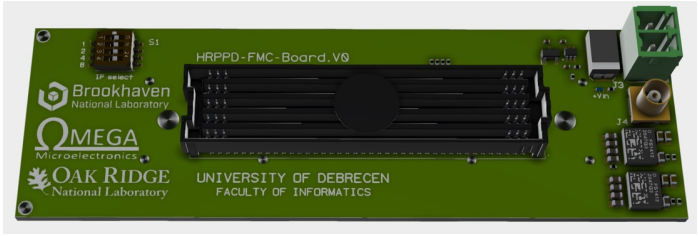
HGCROC3 ASIC / FPGA backplane

All: V0 iteration

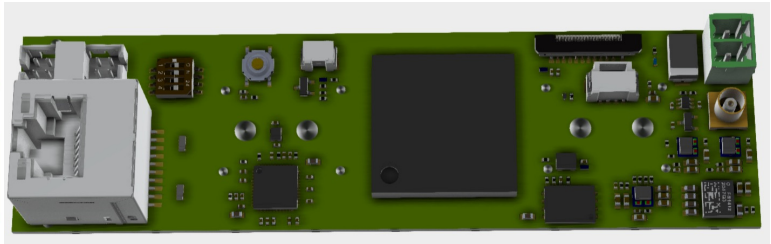
IN2P3 [OMEGA] (Pierrick, Damien), Uni Debrecen (Gabor, Miklos)
BNL (Daniel), Oak Ridge (Norbert)



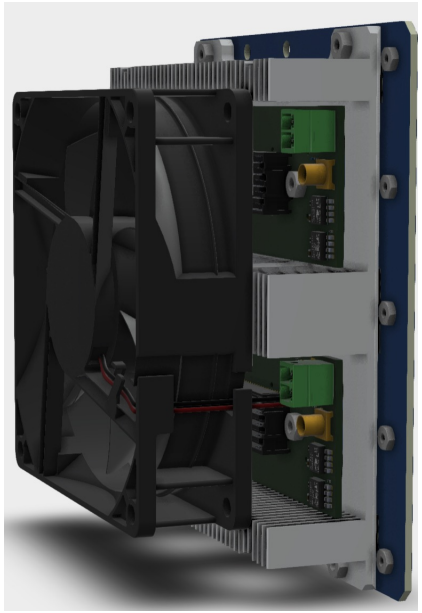
ASIC board



"Passive" interface to a KCU105 kit



A fully fledged FPGA control board



Full assembly; cooling

- ASIC & FMC (passive) boards ordered; expected by Christmas time; suffice for basic evaluation
- FPGA board design to be ready by Monday; then place a PO shortly

A clone of a BNL HRPPD test stand for Yale

- Prakhar and Andrew visited BNL for a couple of days this week
  - We used spare parts (except for the laser) to build a 32-channel clone of the BNL setup

Beam test plans in 2024

- Default option: both “HRPPD” and “pfRICH” parts at Fermilab in May 2024

- Other possible options (in Europe, then “HRPPD” setup only?):
  - DESY in June 2024 (parasitic to AC-LGAD team)
    - Staffed by Glasgow, 1-2 people from BNL, ..?

  - In parallel with LHCb PID folks?
  - Perhaps in parallel with dRICH?