Third Party ASICs for ePIC

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UC Santa Cruz team

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SCIPP
SANTA CRUZ INSTITUTE
FOR PARTICLE PHYSICS
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Introduction

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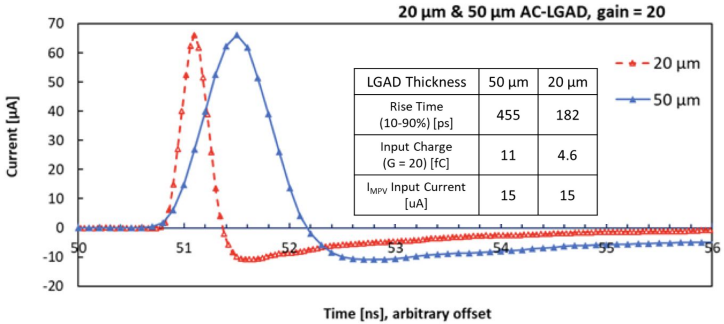
- UC Santa Cruz has been working on ASICs for readout of fast signals generated by AC-LGADs silicon sensors
- Overarching design goals:
  - **Fast timing** (Jitter < 10ps)
  - **Low-power consumption,** (<1mW per channel)



- Targeting applications for EIC Time of Flight detector using AC-LGADs

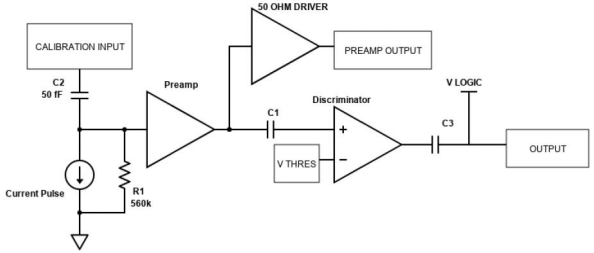
Institution	Name	Technology	Output	# of Chan	Funding	Specific Goals	Status
INFN Torino	FAST	110 nm CMOS	Waveform & TDC	20	INFN	Large Capacitance TDC	Testing
NALU Scientific	HPSoC*	65 nm CMOS	Waveform	5 (Prototype) > 81 (Final)	DoE SBIR	Digital back-end	**V2 ready**
Anadyne Inc	ASROC**	Si-Ge BiCMOS	Discrim.	16	DoE SBIR	Low Power	**Testing**

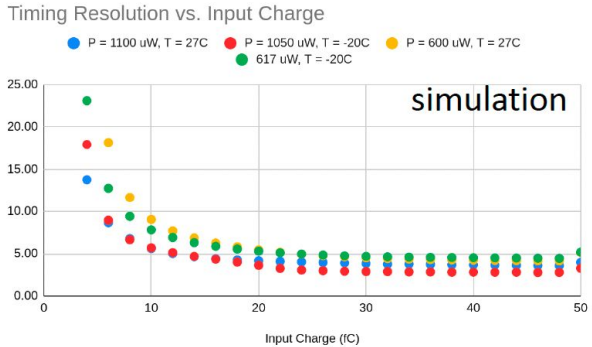
Focus of today's presentation

AS-ROC chip

AS-ROC

- Chip developed together with Anadyne Inc. & Joel DeWitt using Tower Semiconductor Silicon Germanium (SiGe) BiCMOS technology
  - Target very low power consumption (<1mW/ch)
  - Current prototype with 16 channels output
  - Both analog preamp, and discriminator output
- **Expected jitter <10ps @ 8fC from simulations**
- Readout board developed by SCIPP team





AS-ROC: Status

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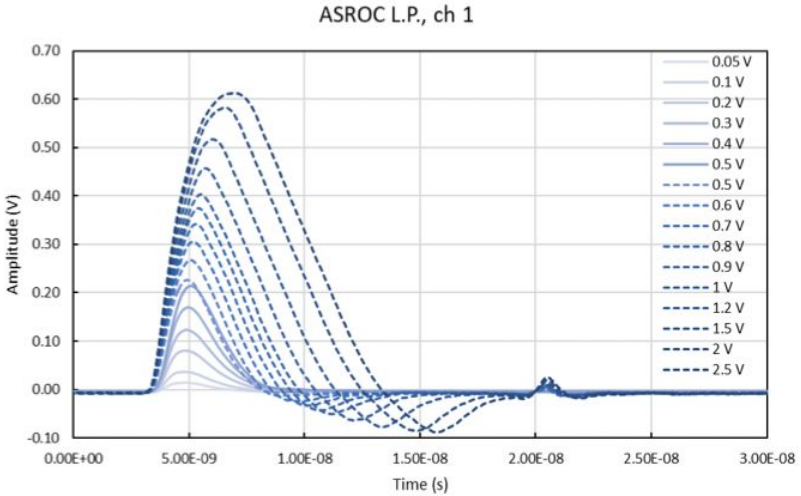
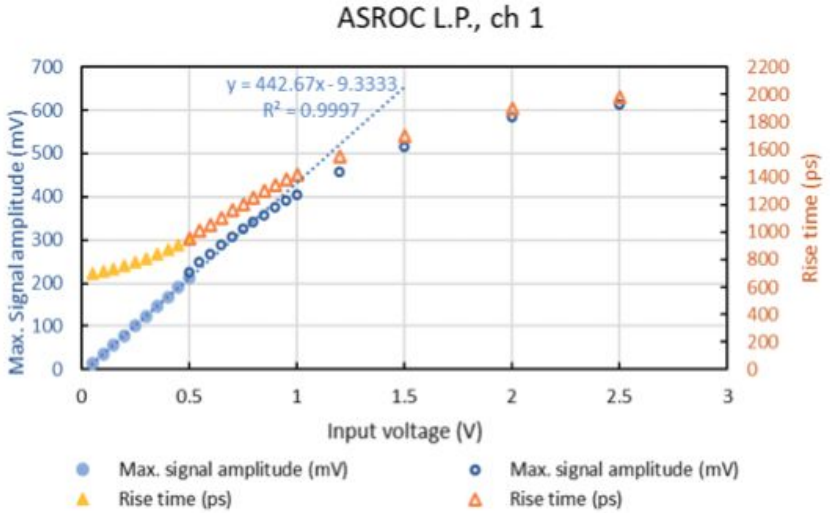
- Characterization of **analog front end** well advanced
  - Good pulse shape and excellent gain for most of the dynamic range
  - Rise time from 700 ps – 2ns at saturation point





AS-ROC: Status

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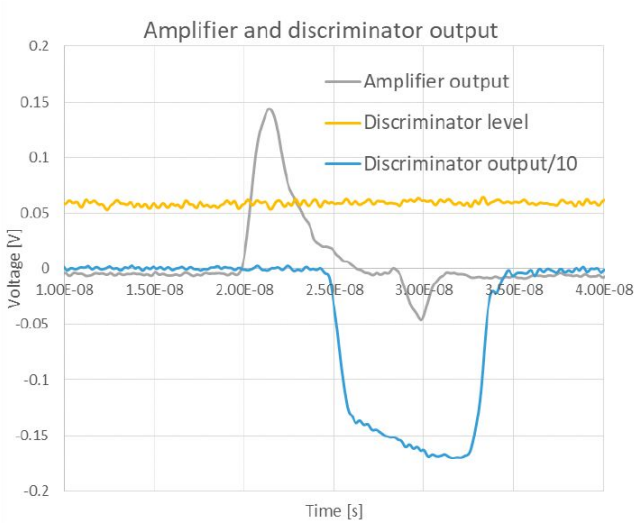
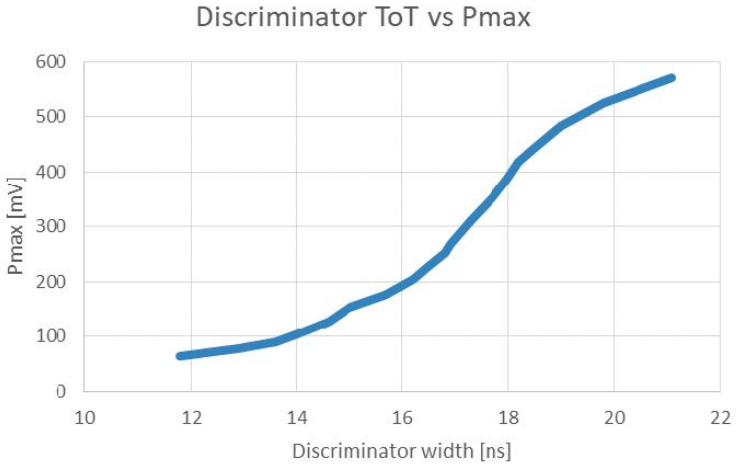
- Characterization of **analog front end** well advanced
- Discriminator output functioning as expected, with jitter < 10ps
  - Discriminator output is a 1.5V step function with rise time < 1ns
  - Width proportional to pulse maximum → can be used to correct time walk





AS-ROC: Sensor beta-testing

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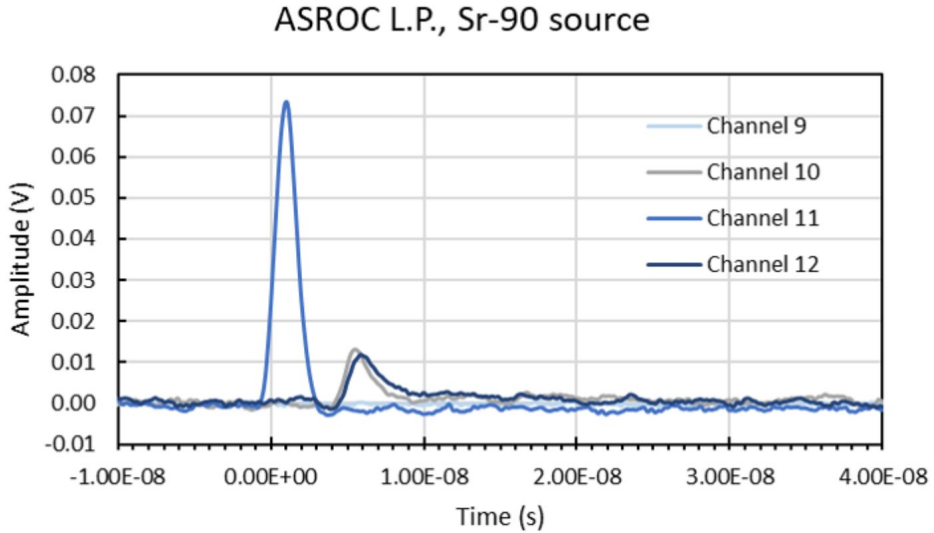
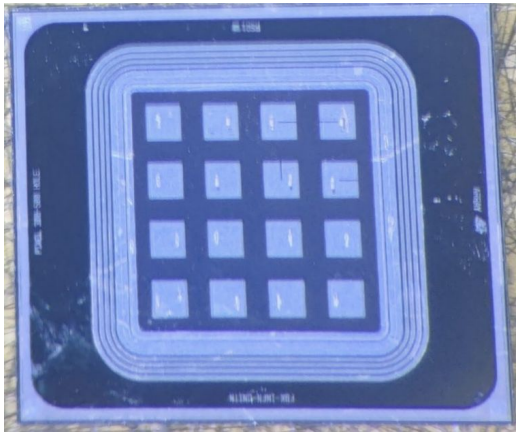
- Chip was connected to several pads of an AC-LGAD from an FBK RSD1 sensor
- Noise level around 700 uV
  - Agrees well with simulations for sensor input capacitance of 500 fF.
- Sensor was tested with a beta-source (figure below)
  - Excellent S/N, and charge sharing between channels observed!





AS-ROC: Laser TCT beta-testing

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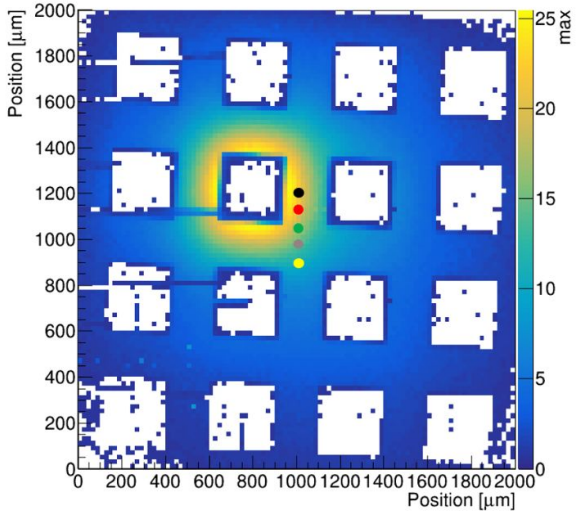
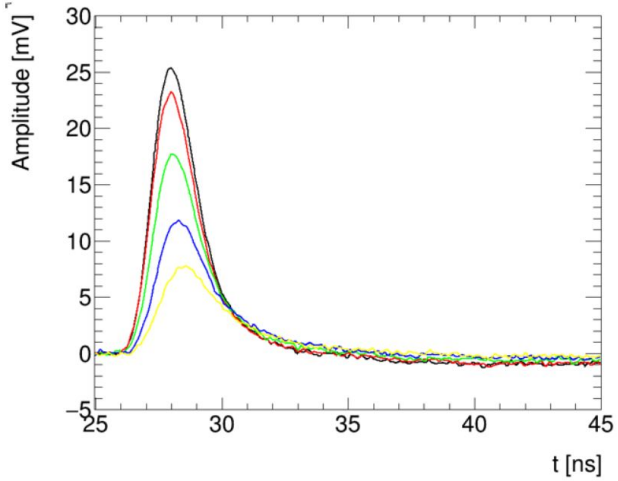
- Chip was connected to several pads of an AC-LGAD from an FBK RSD1 sensor
- Laser TCT scan performed, initial results shown below
  - Colors on 2D plot correspond to signal location in the waveform on the right. Closer proximity, larger signal as expected.
  - Data analysis ongoing to further characterize performance.





AS-ROC: Observations & next steps

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- The prototype chip fabricated at Tower Semiconductor performs well, but the initial characterization shows slightly inferior pulse amplitude and rise time compared to what we expected in the simulation
- Originally we wanted 10ps jitter at 8 fC, instead, we see it at 20fC (at the moment the signal is reduced by 20% because of the external driver). The measured rise time is ~50% higher than in the simulation.
- We only tested one version of the chip and we had some technical difficulties on the boards. Needed to rework test boards, and we expect a full characterization in the next few months
- Planning to perform a measurement of power consumption when boards are finished, hopefully this week

HPSoC chip

HPSoC

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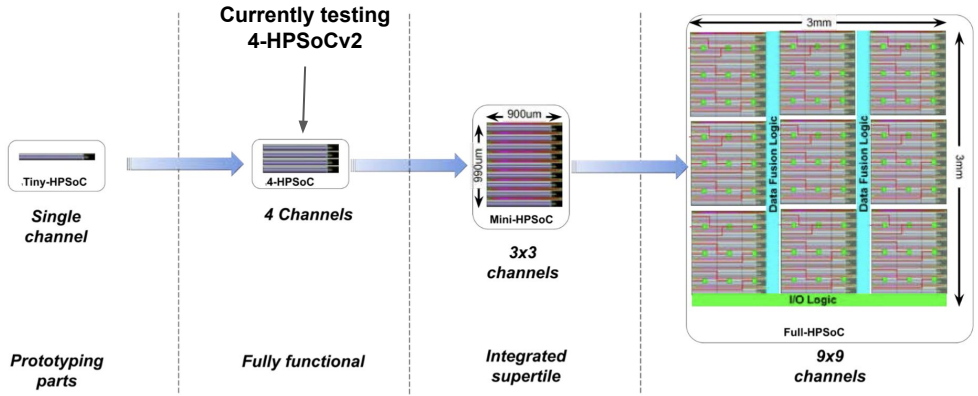
- The HPSoC design implements signal pre-amplification along with **full waveform sampling and digitization** in an ultra-small area package size compatible with small-pitch sensors
- Waveform digitization **promising technique** to reduce the noise from various sources of electronic noise to achieve timing resolution <10ps

Parameter	Specification
Channel no.	miniHPSoC chip (this proposal): 9 Full chip (post FY23): ~100 (pitch ~300µm)
Process	65nm CMOS
Sample rate	10 GSa/s
Bandwidth	2 GHz
No. bits	10
Supply Voltage	1.0V (2.5V for digital I/O)
Timing accuracy	5 ps
Front-End stage	Embedded TIA
Buffer length/channel	256 samples
Power/channel	<2mW



Waveform digitization

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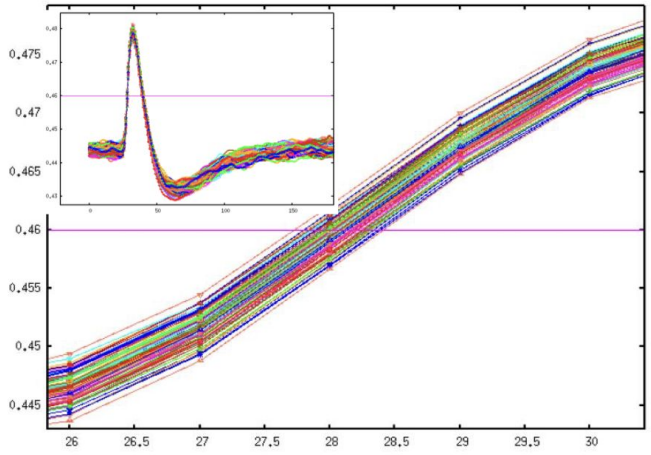
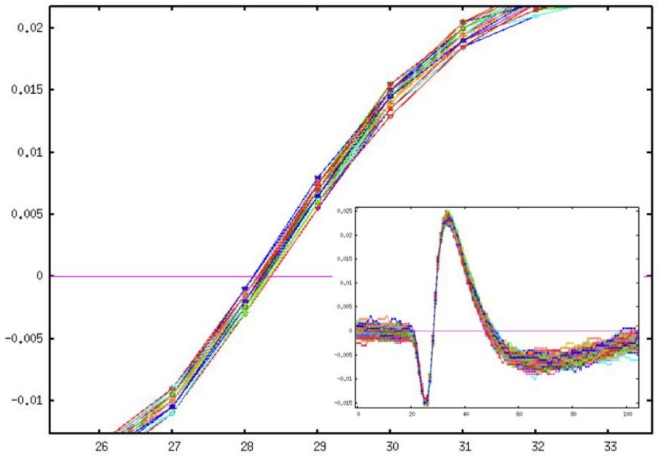
- Waveform digitization at 10 GS/s: allows digital baseline correction, constant fraction discrimination and other algorithms for improving jitter component of the timing resolution & feature extraction
- Simulated HP-SoC v2 output digitized waveforms with noise: estimated reduction from 13.7 ps (leading edge) to 5 ps





HPSoC: Overall status

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- HPSoC v2 chip fabricated & diced, and shipped to UCSC
- Readout board designed, fabricated, and mechanically loaded in collaboration with Nalu Scientific team
- Efforts spent on debugged powering issues:
  - Discovered chip wire bonding was shorting to the chip seal
  - Underlying issue was the extremely small bond-pads on chip
  - Develop procedure to overcome small bond-pads: moved to smaller wire size and corresponding wedge (in-house)
- Calibration pulses used to characterize the analog TIA, and first results when pairing with HPK AC-LGAD sensors

HPSoCv2 board design

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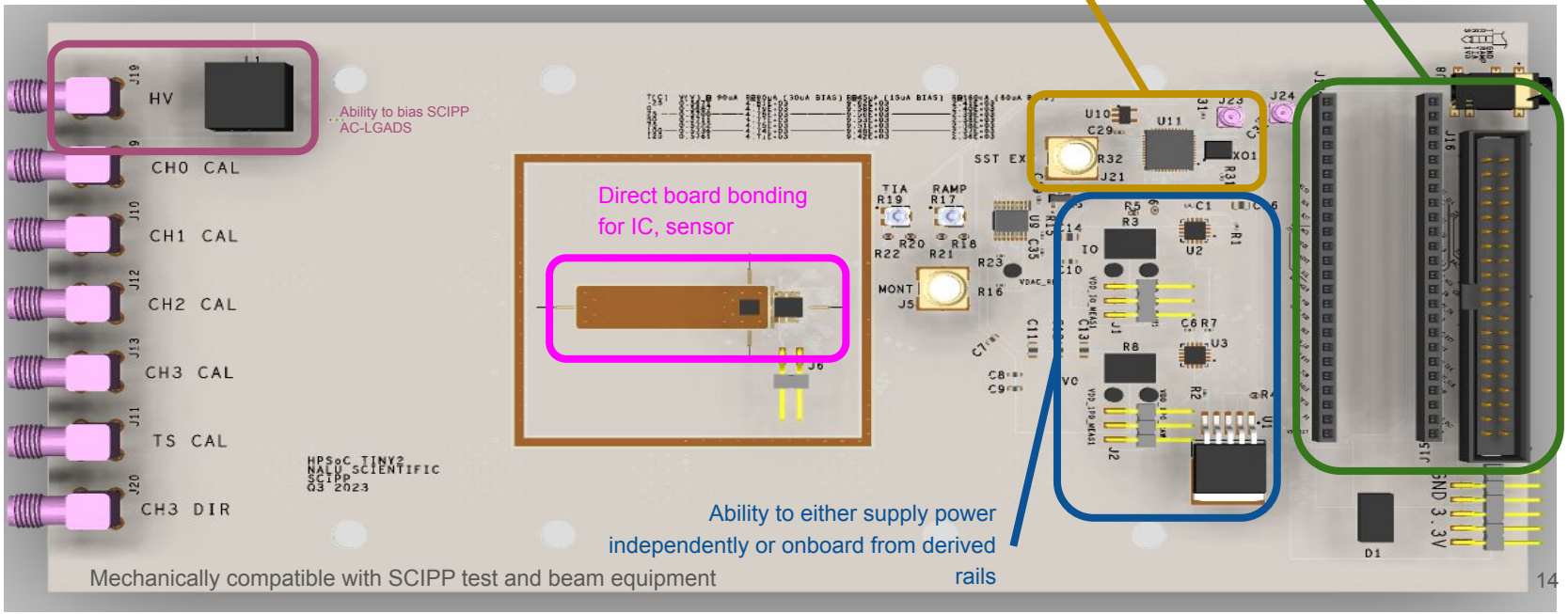

HPSoCv2 bonding

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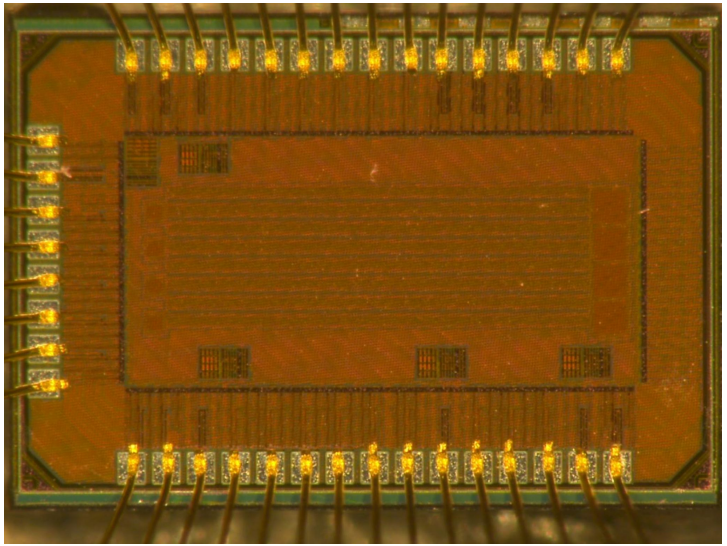
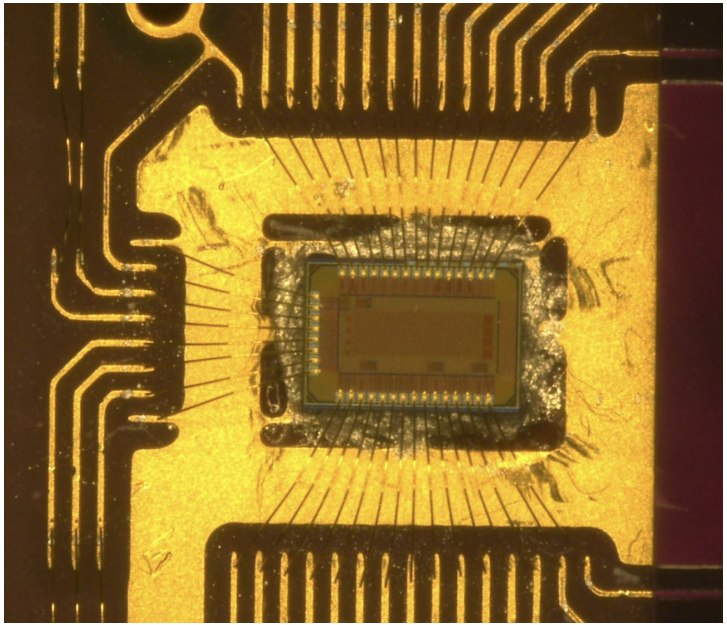
- Moved to smaller bond wire and dedicated wedge





HPSoCv2: Preliminary results

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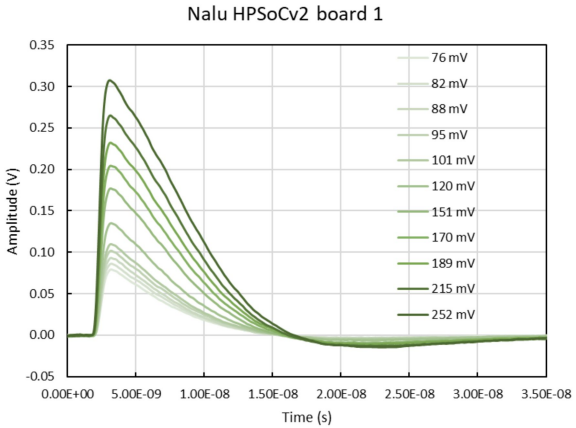
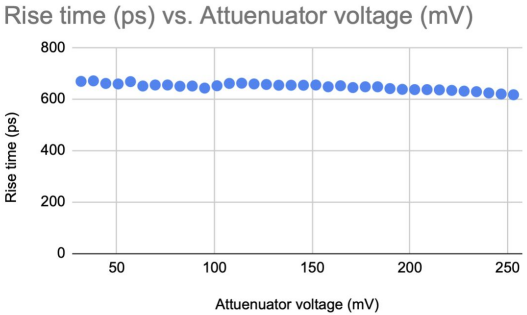
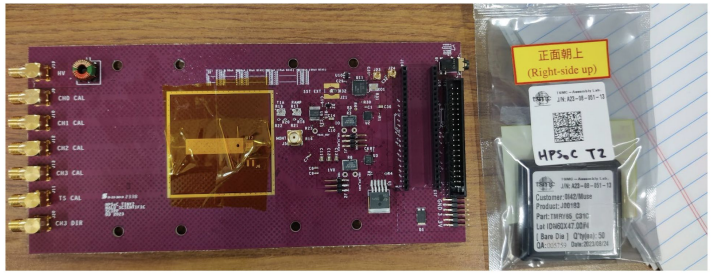
- Status: HPSoCv2 chips in hand, corresponding readout board designed & fabricated, and front-end characterization has started
- Calibration pulses injected to characterize the TIA
  - Observe rise time in the range of 600-700 ps
    - Sensitive to the TIA configuration. We have seen that this can be improved with improved configuration of the offset. Further exploration early next year.
  - Improved gain compared to v1 chip







HPSoC v2: ASIC + Sensor

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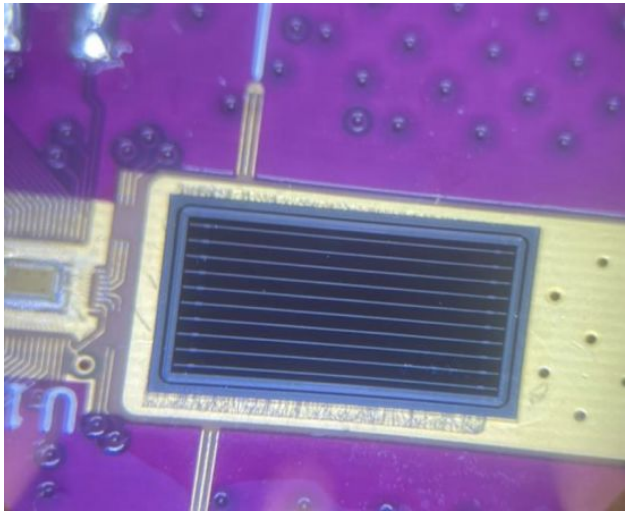
- Sensors from an HPK AC-LGADs runs with 500 µm pitch were tested with laser and a Sr-90 beta source
  - 4x4 pad array, type C600, 50 µm thick, 300 and 450-µm pad
  - 1 cm strip, 50 µm thickness, 50 µm metal width, type C600
- Data acquired using GHz probe and oscilloscope connected to standalone TIA output



HPSoC v2: ASIC + Sensor Results

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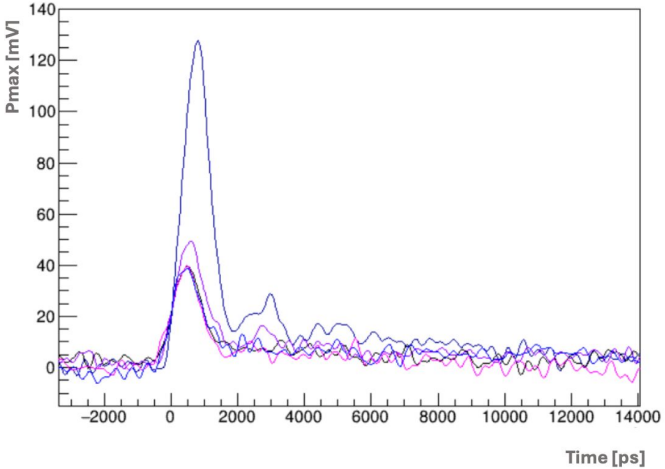
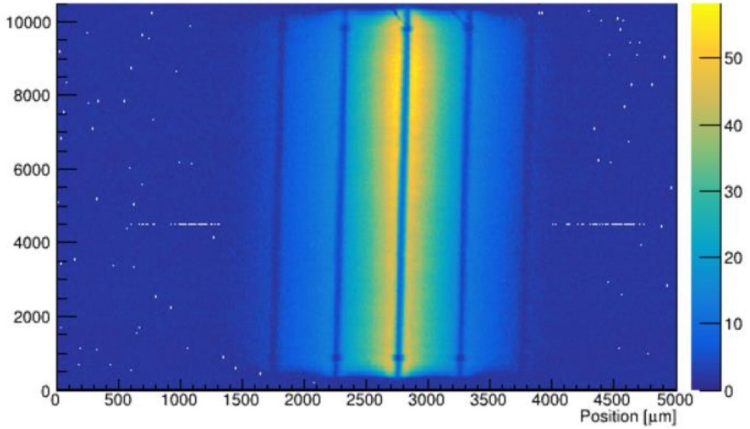
- Laser scans of pad and strip sensors were conducted, data still being analyzed
  - From a quick peek at the data, we see excellent performance of strip sensors with **observed rise time 600-750 ps, jitter ~35 ps**
- Beta source exposure of pad sensors using self-triggered data
  - From a quick peek at the data: **rise time 550 ps, noise rms 1.8 mV**
- Detailed analysis of the data ongoing over the next 1-2 months





HPSoC v2: Initial Digitizer testing

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- So far operated only at Nalu with calibration input and/or supplied waveform
- Firmware development finished recently
  a. Arrived to SCIPP December 8th, initial testing started. Can load firmware.
- Initial testing of internal delay line, internal conversion clock generation and counter, comparator, ramp has been conducted
  - Functional bug found by Nalu staff, in joint control of ramp and counter prevents full internal conversion
  - Nalu has submitted a corrected version of the chip, expected back early 2024

Next steps for HPSoC

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- **Continued funding for HPSoC chip** through the *JLab EIC-related generic detector R&D program*: *Design, Fabrication and testing of a multi-channel System on a chip for Low-Power High-Density High Timing Precision Readout ASIC for AC-LGADs (HPSoCv3) [Oct/23 review meeting, proposal]*
  - Single largest award in FY24, targeting an integrated supertile in a 3x3 channel array
- Also partly funded through FY23 eRD109, but these efforts were dropped from FY24 eRD109 → this does negatively affects the scope of our testing program at UCSC
- For HPSoC v3, need to improve the communication between EIC DAQ & electronics group and Nalu chip designers

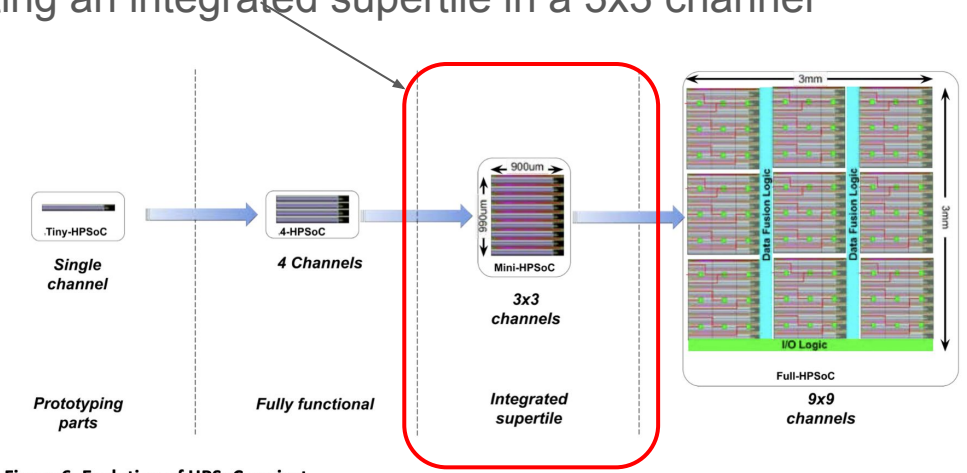

Figure 6. Evolution of HPSoC project

Conclusions

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- The UC Santa Cruz group has been investigating three third party ASICs for time of flight applications at the EIC
- Characterization of the AC-ROC and HPSoC v2 chips have shown good performance, but with a few areas of improvement
- Testing will continue throughout early next year on both chips. Expect a new version of the HPSoC v2 chip and a version of FAST3 early next year
- The HPSoC v3 chip will be continued to be funded and explored by the UC Santa Cruz team in FY24