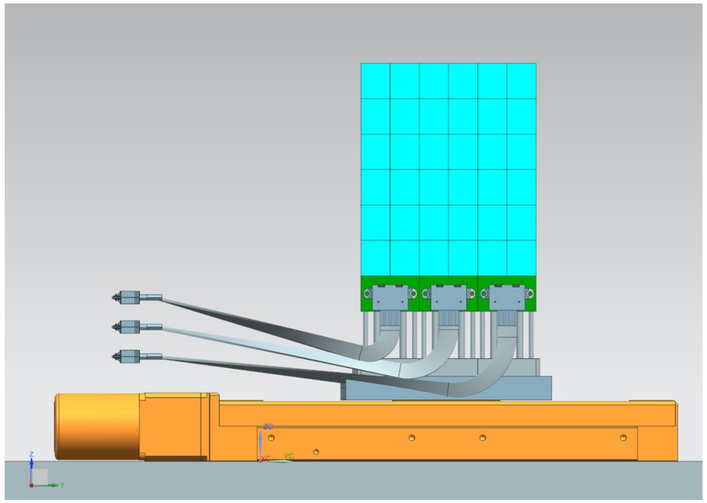
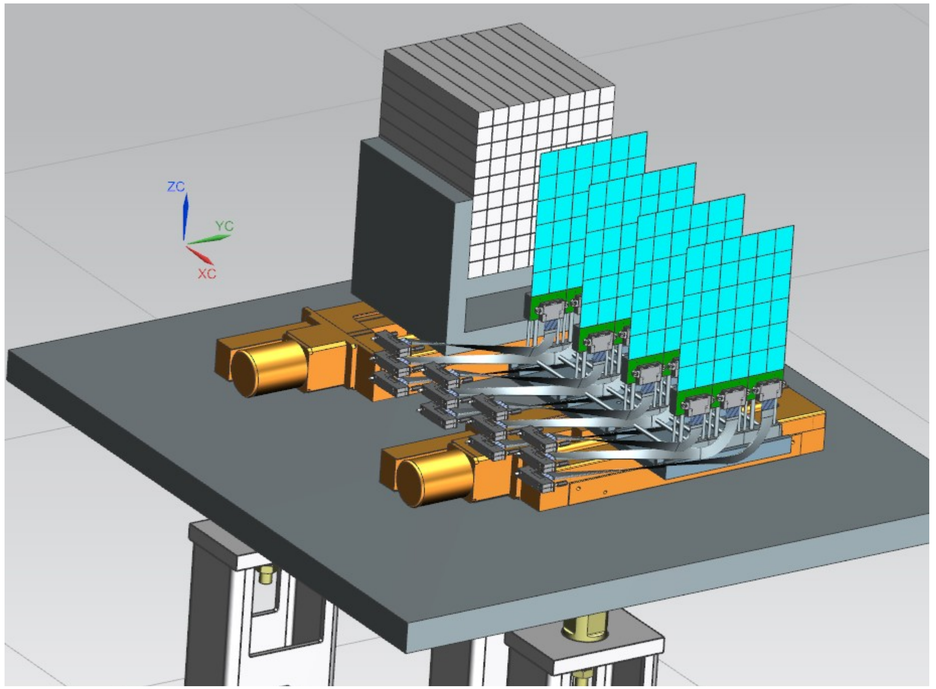
LOW-Q2 SETUP

Tracker

4 tracking layers per Tagger station (30 cm apart – still being optimised)





Pixel-based tracking detectors for a Low Q2 Tagger at EIC – status report:
https://arxiv.org/pdf/2305.02079.pdf

Sensor: Timepix4 + Si Hybrids.

Pixel size: 55x55 um. 448 x 512 pixels per sensor. Area = 6.94 cm^2
Timing resolution 2ns.

Singles rate capability high > 20kHz per 55um pixel

Low material budget in front of the setup
2 Si-stations (outside of the primary vacuum)
… but Timepix is designed to operate under 10^{-6} mbar vacuum

Location: Tagger 1 23.7 - 24.7 m
Tagger 2 35.7 - 36.7 m

Calorimeter

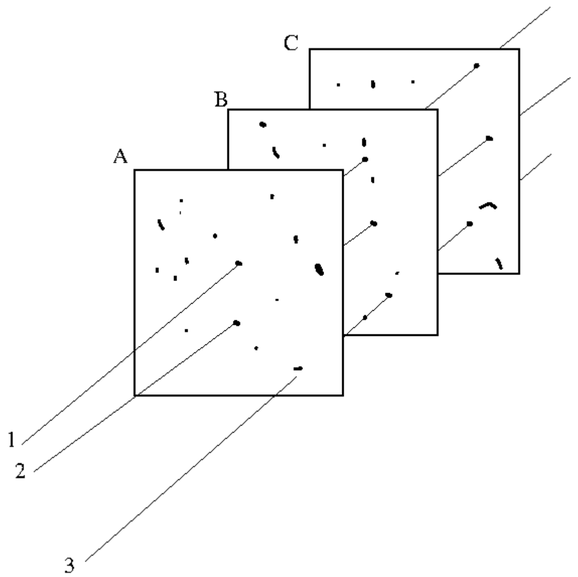
PbWO4 (?) towers 2x2x20 cm
Total size 26x24cm

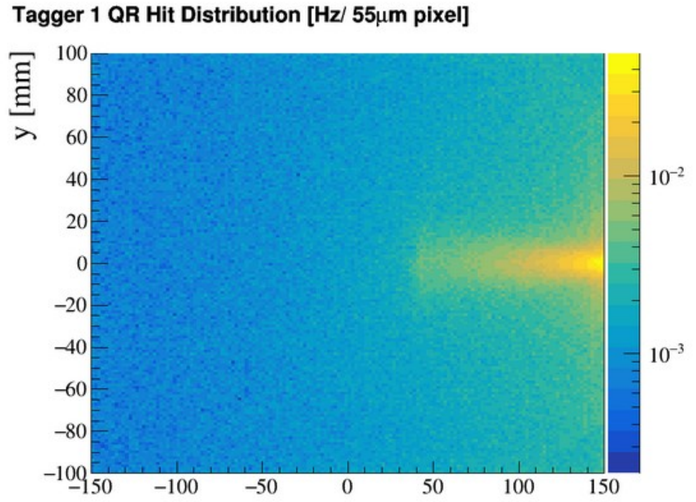
Timepix4 tracker rates from Geant4

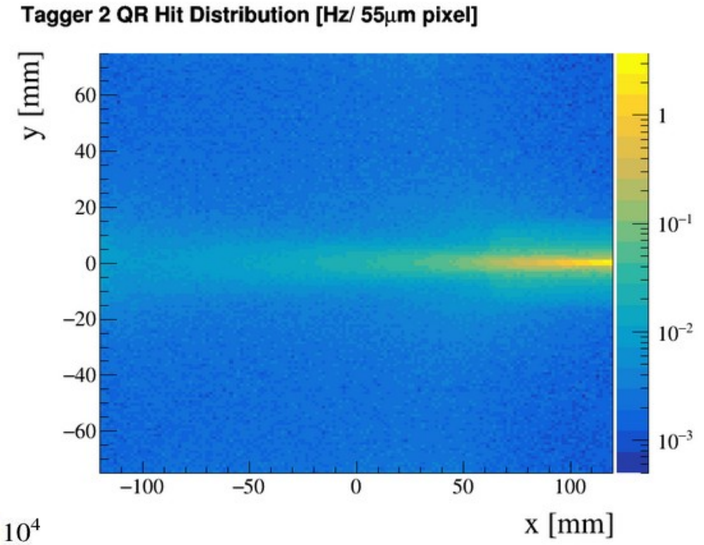
Timepix4 tracking layer design

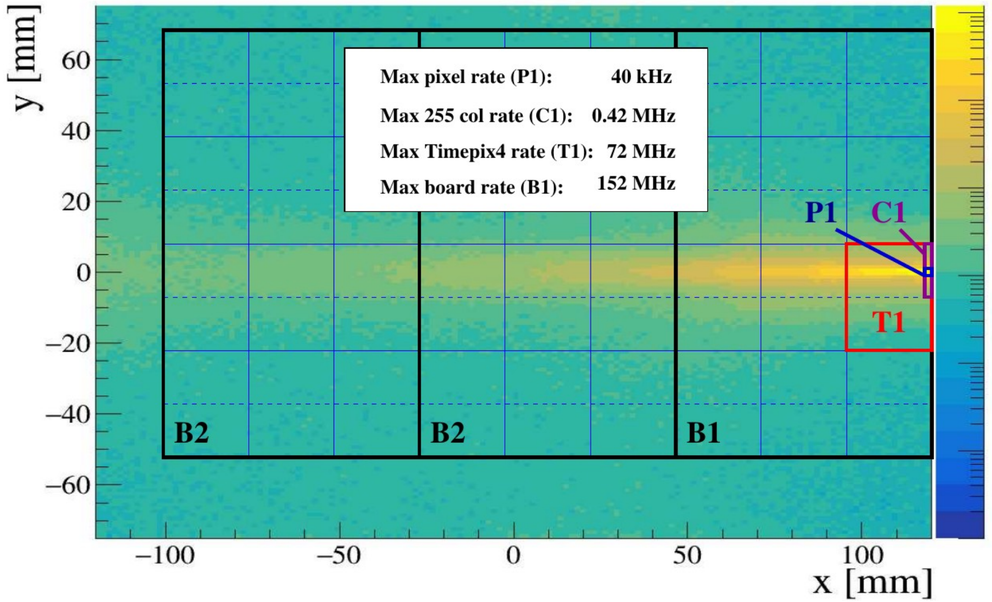
4 layers per tagger (2 taggers)
3 boards per layer
12 Timepix4 per board

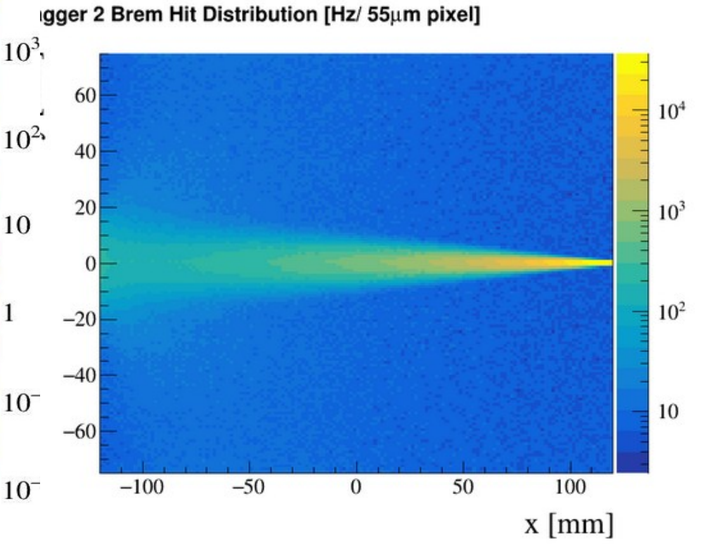
66M pixels
Max board bit rate: 115 Gb/s
Reduced DAQ rate: 20Gb/s











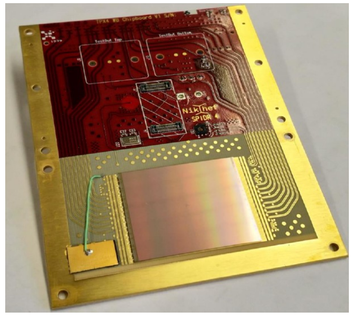
Timepix4 + SPIDR4 Design and prototype

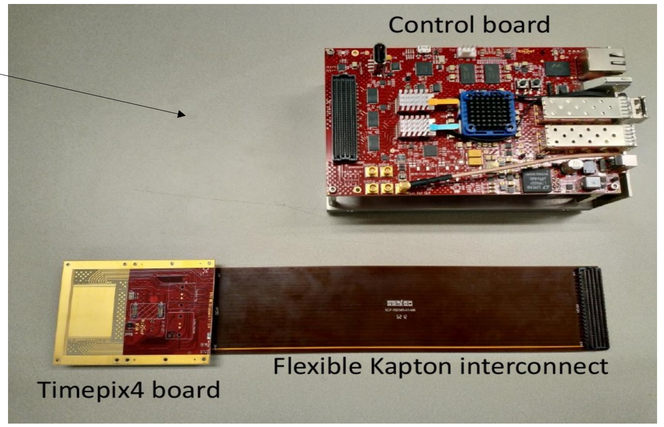
Timepix4 tracking layer design

4 layers per tagger (2 taggers)
3 boards per layer
12 Timepix4 per board

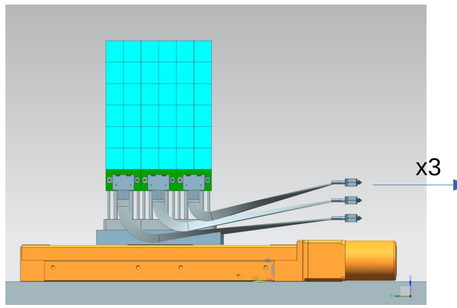
66M pixels
Max board bit rate: 115 Gb/s
Reduced DAQ rate: 20Gb/s

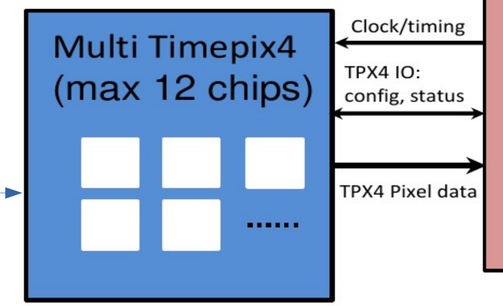
Prototype tracker based on:
2 x Timepix4 + SPIDR4
(Expected from Sept 2023)



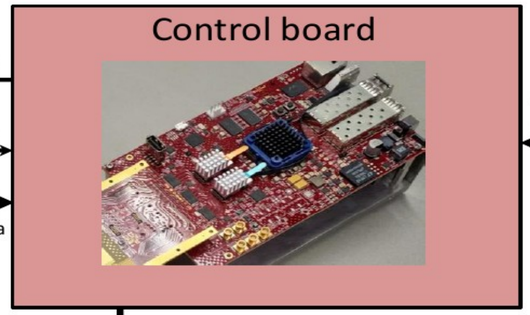


SPIDR4: Multi chip, 2 x 10 Gb/s per TPX4 chip

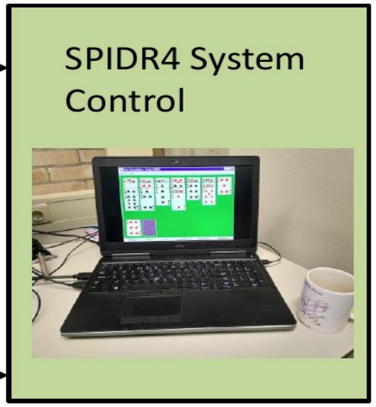




Clock/timing
TPX4 IO:
config, status
TPX4 Pixel data



Control, gRPC
(1Gb/s ethernet)



TPX4 Pixel data
24 x 10Gb/s = 240 Gb/s

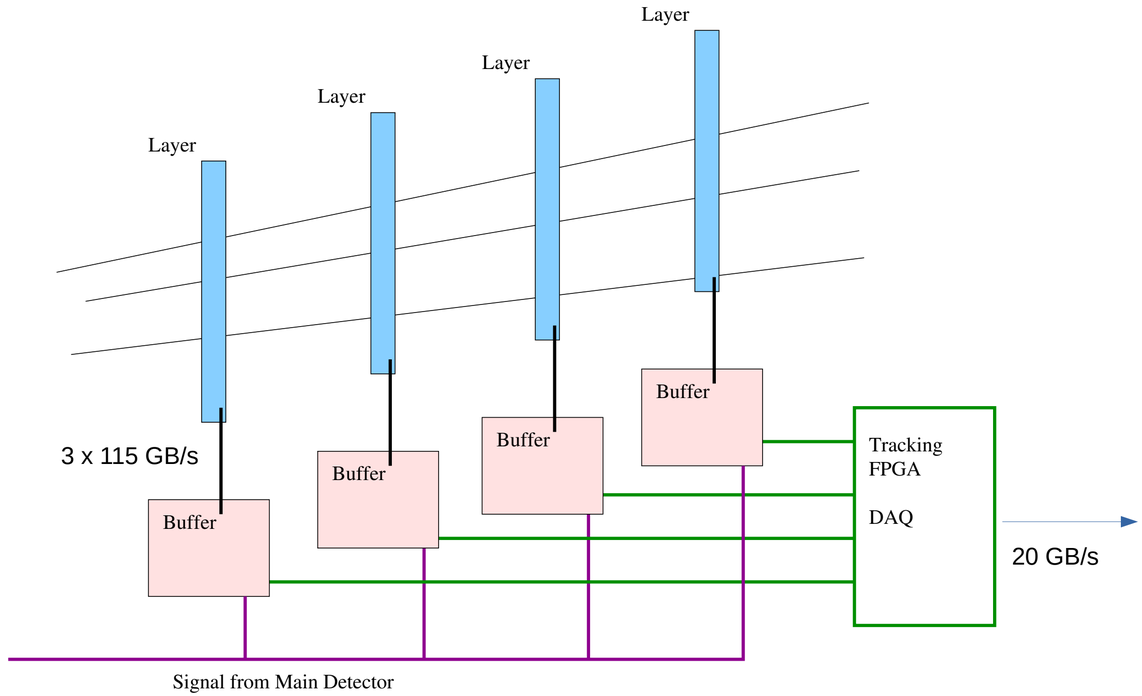
Data access

Full tracker board
Schematic

Timepix4 and SPIDR4 images from
Marten Fransen
https://www.nikhef.nl/~s01/SPIDR4-MF-GP-apr2020.pdf

Xilinx Virtex UltraScale, FPGAs in PCI slots

Timepix4 + SPIDR4 Readout



Only pass data which has coincidence with hadron to DAQ / Tracking / Store

Average number of electrons through tracker per bunch crossing	10	electrons
Total number of tracker layers (2 x 4)	8	layers
Total number of hits per bunch crossing (10 x 8)	80	hits
Bits per cluster (x, y, time, energy, width: 5x2 bytes)	80	bits
Total bits per bunch crossing (80 x 80)	6400	bits
Hardon trigger rate	500	kHz
Total bit rate for hadron triggers (6400 x 500 kHz)	**3.2**	**Gb/s**
Total bit rate, including random sample for BG	**20**	**Gb/s**

Maximum pixel rate	120	kHz
Maximum 255 column rate	121	MHz
Maximum Timepix4 rate	214	MHz
Maximum board (12 timepix4 sensors) rate	460	MHz
Maximum board (12 timepix4 sensors) rate, including synchrotron BG	1.8	GHz
Data readout per pixel	64	bits
Maximum board bit rate (64 x 1.8 GHz)	**115**	**Gb/s**