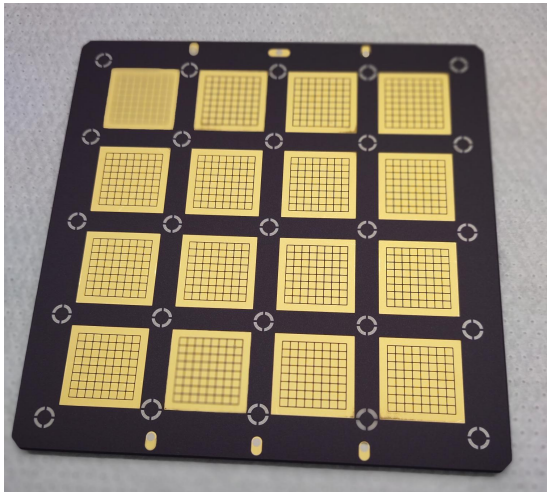
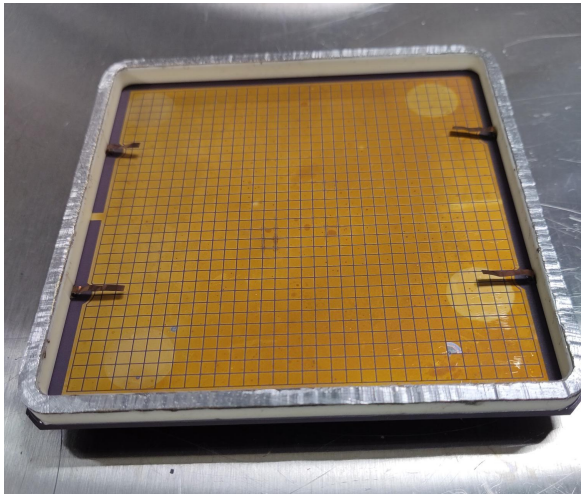
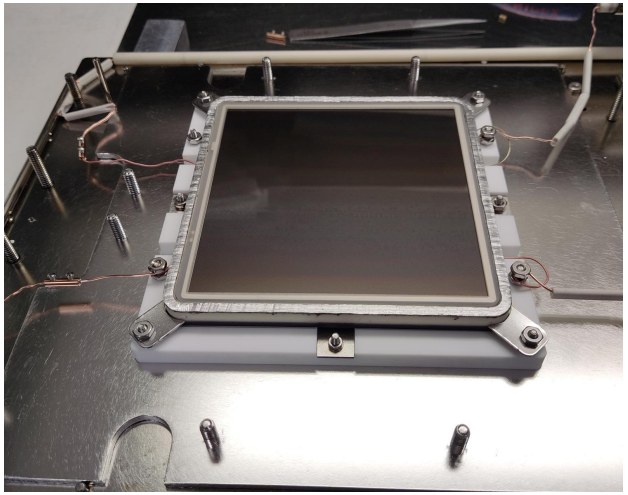
HRPPD manufacturing



Screw markings

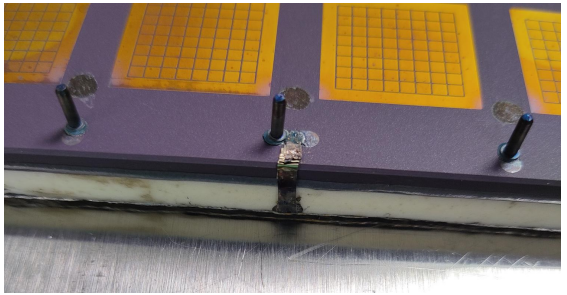


Side walls; indium alloy; HV springs



With MCPs; placed in a sealing tank

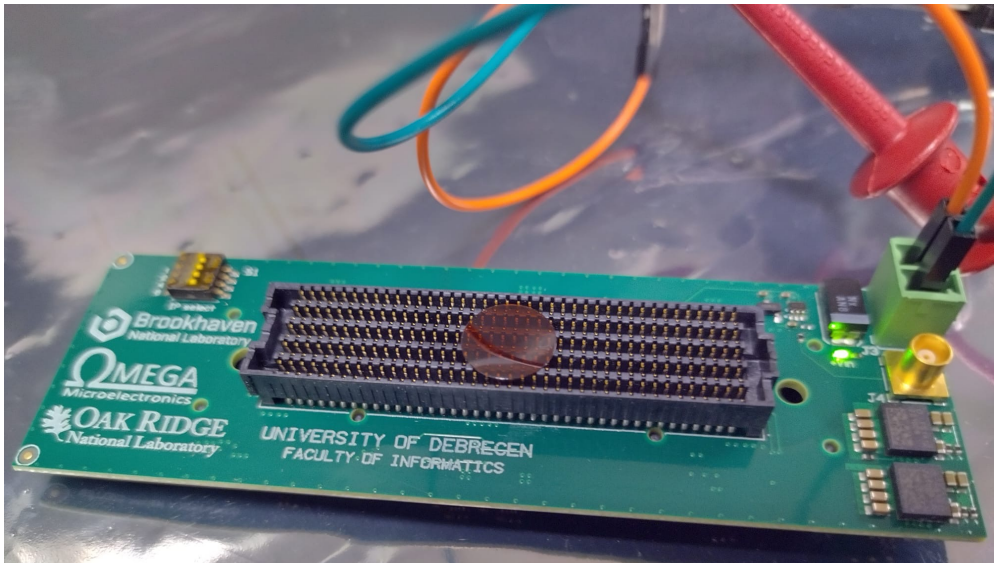
- Baking out starting today or tomorrow
- Then a winter break at Incom starts
- If everything goes smoothly, this HRPPD#15 should go into a QA process at Incom on January 5th
- Second sealing tank fully functional by January 15th

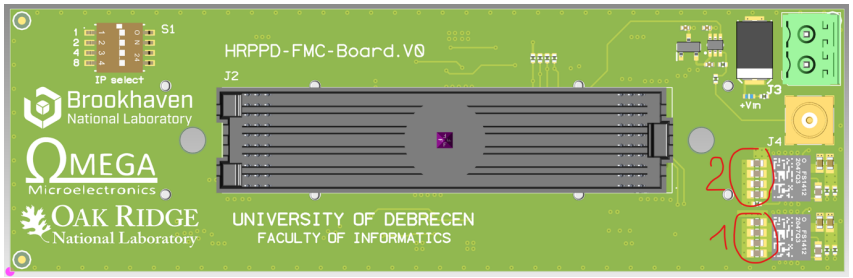


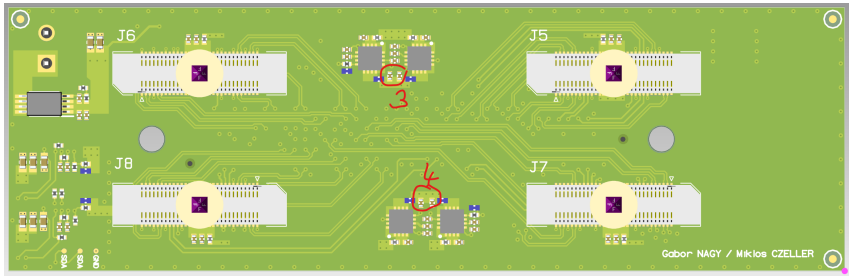
HV pins; photocathode contact

HGCROC3 ASIC / FPGA backplane

IN2P3 [OMEGA] (Pierrick, Damien), Uni Debrecen (Gabor, Miklos)
BNL (Daniel), Oak Ridge (Norbert)



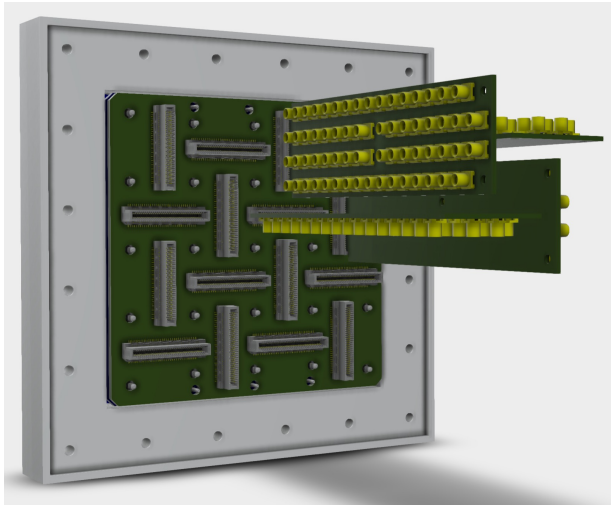




- FMC (passive) board is in a debugging stage at Orsay
- ASIC board is expected by Christmas time
- FPGA board PO: dispatched today, ~3 weeks lead time (well, over Christmas & New Year -> mid January)

Other news

- HRPPD anode base plate electrical measurements at BNL
  - Trace resistivity <1 Ohm, capacitance 4-7 pF



- Passive interface #2 board (Q00a): PO dispatched today
  - Still need to finalize and submit 3D printed parts for production

- HRPPD evaluation procedure
  - Document is being circulated in eRD110; to be sent to the EIC project management next week
  - A meeting between BNL / JLab / Yale colleagues Friday last week
  - HRPPDs will be first shipped to JLab, express-tested there, then sent to BNL, then elsewhere