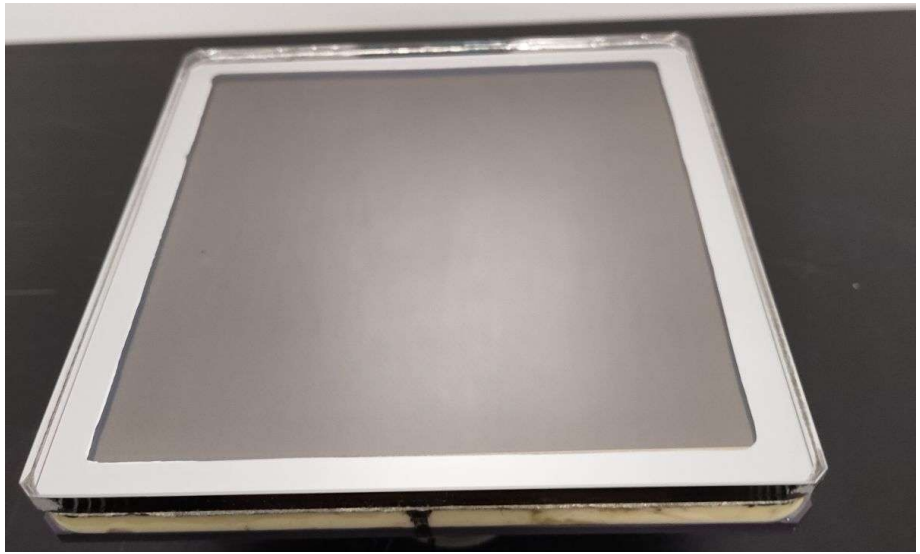
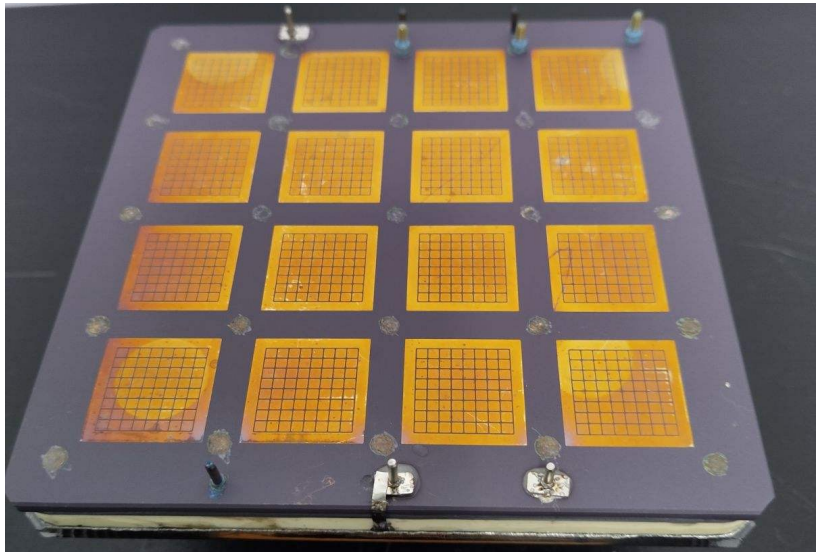
HRPPD manufacturing



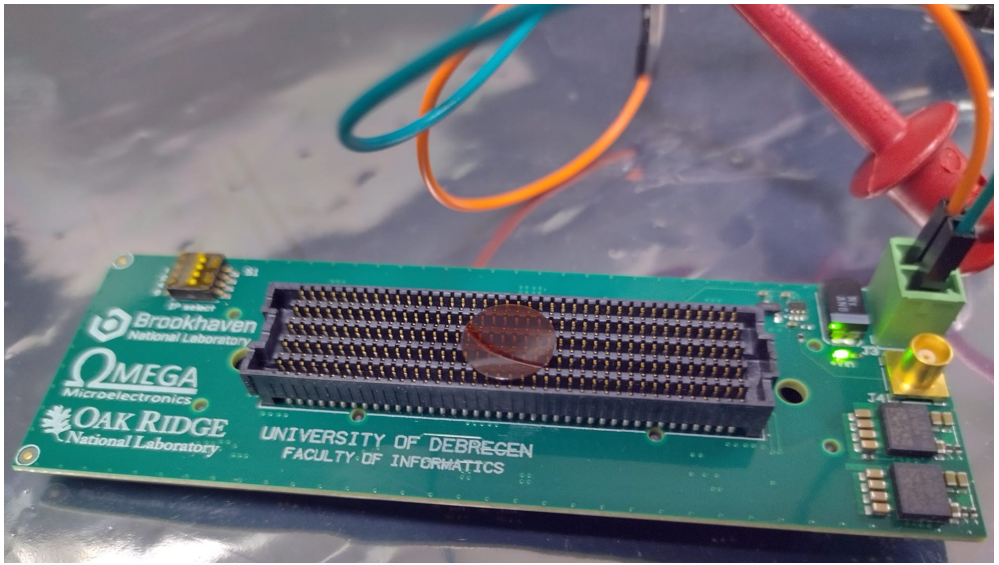


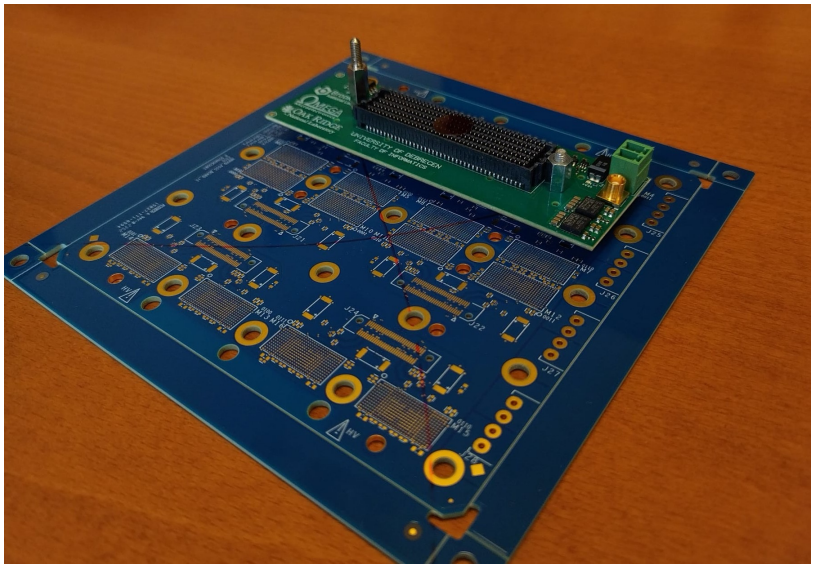
HRPPD #15 (EIC HRPPD trial #1)

- Should have gone into a QA process at Incom today
- A “decent” QE measured already

HGCROC3 ASIC / FPGA backplane

IN2P3 [OMEGA] (Pierrick, Damien), Uni Debrecen (Gabor, Miklos)
BNL (Daniel), Oak Ridge (Norbert)





- FMC (passive) board is in a debugging stage at Orsay
- ASIC bare boards were received today (add ~ten days for assembly)
- FPGA board PO: dispatched three weeks ago, then put on hold, re-design finished yesterday