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U.S. DEPARTMENT OF ENERGY

Progress of FELIX Hardware Development at BNL

E. Buschmann, G. Chatzianastasiou, H. Chen, A. Liu, D. Matakias,

M. Silva-Oliveira, S. Tang, H. Xu

BNL

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Outline

- Status of FLX-182B for small production
- Design of FLX-155

Reminder: Requirements from ATLAS for HL-LHC

- FELIX will be used for ATLAS detector Readout system in Phase-II
  - To receive event data from detector front-end links
  - To relay Timing, Trigger and Control (TTC) information from the Phase-II TTC system to on-detector electronics
- Requirements for FELIX
  - ~12 k uplinks for Phase-II Readout system
  - Link speeds: from 2.5 Gb/s to 25 Gb/s
  - 24 channels for majority application, 48 channels are preferred for LAr LTDB and some NSW sectors
  - PCIe Gen4 (at least) for data output
  - Electrical connection for trigger signal
- A new FELIX with advanced FPGA is being developed to meet high throughput requirements
  - FLX-182 with Xilinx Versal FPGA production device

Table 2.4: Summary of Phase-II Detector Readout Link and Bandwidth Requirements. Downlink refers to data travelling toward the front-end electronics, and uplink to data travelling from the front-end toward the rest of the DAQ system. Detectors with existing FELIX installations from Phase-I will be updated with new hardware as required. Where no split between downlink and uplink is presented, it is assumed that the number of downlinks will at most match the number of uplinks, with a downlink bandwidth of 2.5 Gb/s for lpGBT and 5 Gb/s for GBT mode (and implicitly FULL mode). For 25 Gb/s uplinks the corresponding downlink speed has yet to be specified, but will likely be 5 or 10 Gb/s.

Detector	Number of FELIX boards	Number of Links	Bandwidth (Gb/s)	Top-level Link Protocol
ITk Pixel downlink	220	1564	2.5	lpGBT
ITk Pixel uplink		4684	10	
ITk Strips downlink	76	1552	2.5	lpGBT
ITk Strips uplink		1824	10	
LAr LASP downlink	5	200	5	GBT
LAr LASP uplink	48	1136	10	FULL
LAr LDPB downlink	8	31	5	FULL
LAr LDPB uplink		155	10	
LAr LATS downlinks	6	26	5	lpGBT
LAr LTDB downlinks	16	620	5	GBT
L0Calo downlink	8	16	5	FULL
L0Calo uplink		120	10	
NSW downlink	96	1728	5	GBT
NSW uplink		2880	5	
NSW Trigger Processor	4	96	5	GBT
RPC downlink (incl BI)	4	32	5	FULL
RPC uplink (incl BI)		96	10	
CTP downlink	1	0	5	FULL
CTP uplink		12	10	
MUCTPI downlink	1	2	5	FULL
MUCTPI uplink		8	10	
MDT Trigger Processor	32	64	2.5	lpGBT
MDT Trigger Processor		768	10	
Global Trigger GEP	7	50	25	Interlaken
Global Trigger MUX & gCTPi	4	74	25	lpGBT
Tile	8	161	10	FULL
TGC Endcap Sector Logic	8	192	10	FULL
HGTD DAQ Path	48	1152	10	lpGBT
PLR	4	32	10	lpGBT
BCM'	2	12	10	lpGBT
LUCID	1	4	10	lpGBT
ZDC	1	9	10	lpGBT
AFP	2	32	10	lpGBT

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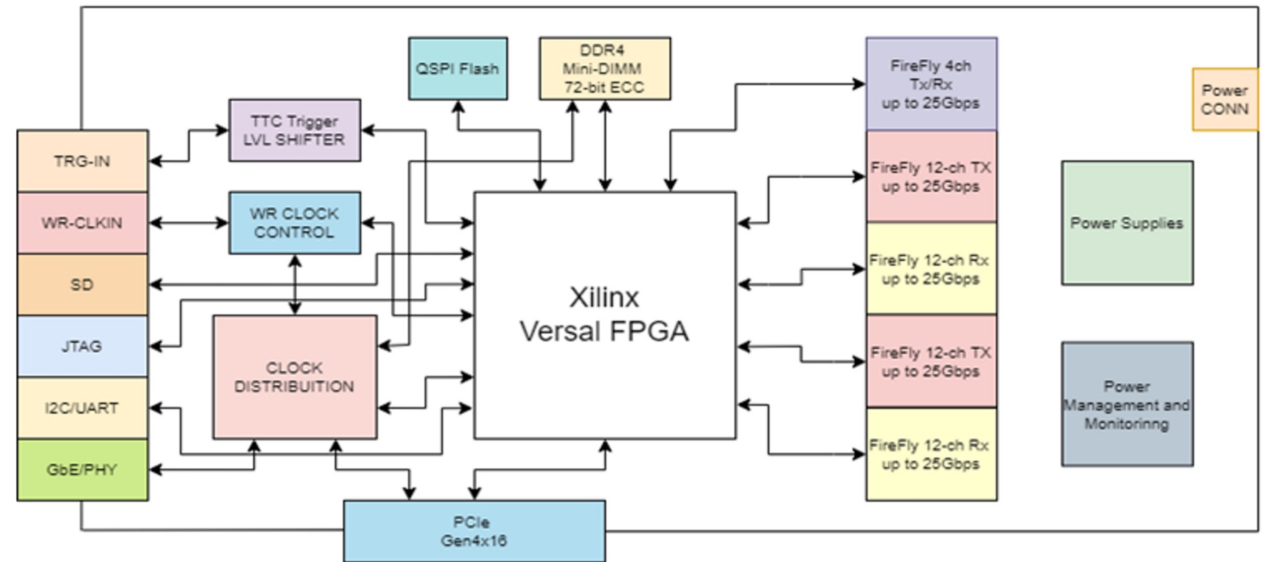
FLX-182 Features

Main features of FLX-182

- XCVM1802 production chip
- PCIe Gen4 x16: PL and CPM compatible
  - PL: Hard PCIe endpoint like in earlier FPGA series
  - CPM: Hard PCIe endpoint integrated in SoC, data transferred over NoC
- 24 FireFly links with 3 possible configurations
  - 24 links up to 25 Gb/s
  - 24 links up to 10 Gb/s (CERN-B FireFly)
  - 12 links up to 25 Gb/s + 12 links up to 10 Gb/s
- 4 FireFly links with 2 possible configurations with 14 or 25 Gb/s FireFly TRx
  - LTI interface
  - 100 GbE
- 1 DDR4 Mini-UDIMM
- USB-JTAG/USB-UART
- SD3.0/QSPI
- GbE



Block diagram of FLX-182

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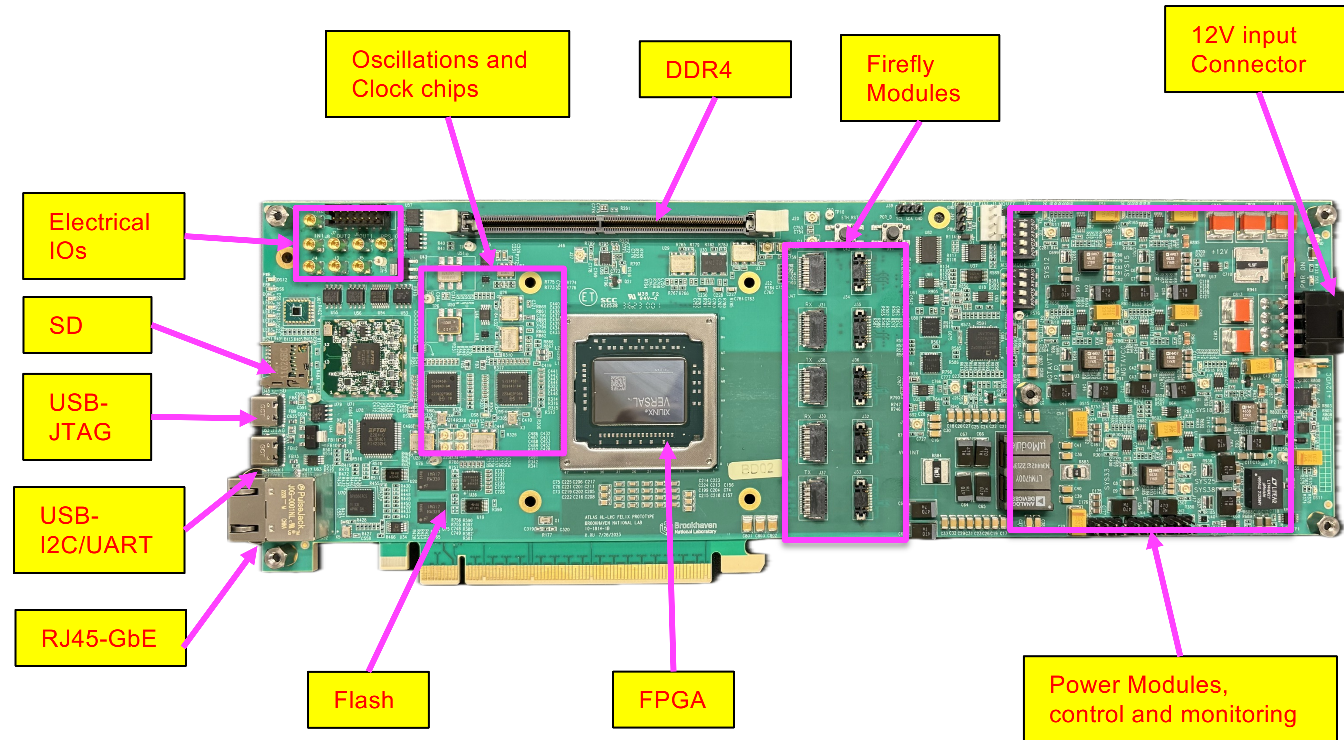
FLX-182B

- ~10 FLX-182 were produced for different applications. Some minor changes are needed to make small production in 2024.
- Minor changes of FLX-182
  - Replace the -5V power module
  - Change the position of MMCX connector
  - ADM1266 is used for power monitoring and control
- 3 assembled PCBs delivered end of Dec. 2023
- Functionalities and performance can meet the requirements.
- Started 46 boards production



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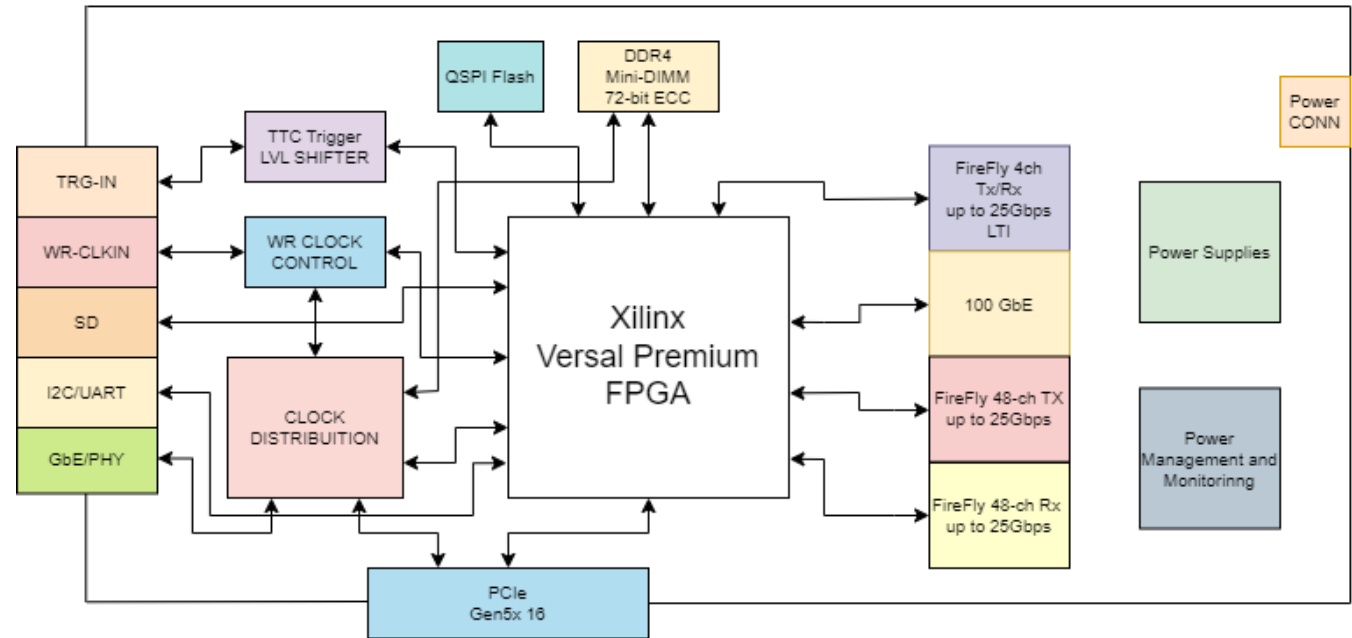
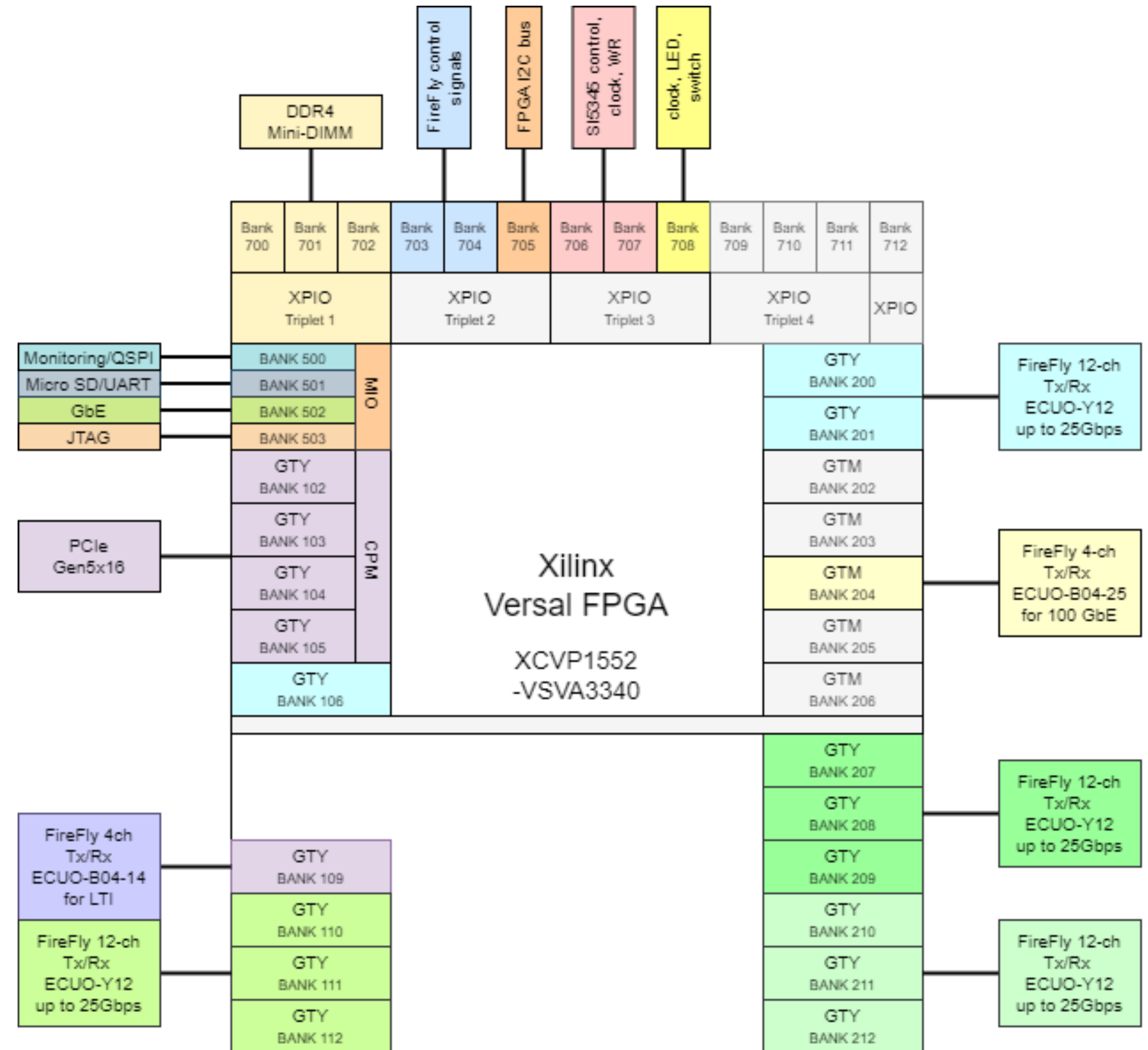
FLX-155

- Versal Premium: XCVP1552-VSVA3340
- Support PCIe Gen4 x16, 2 Gen5 x8
- 48 FireFly data links (10/25 Gb/s)
- 4 LTI links (10/25 Gb/s)
- 100GbE (4*25Gb/s)
- DDR4
- GbE
- White Rabbit
- Electrical IOs (single-ended)



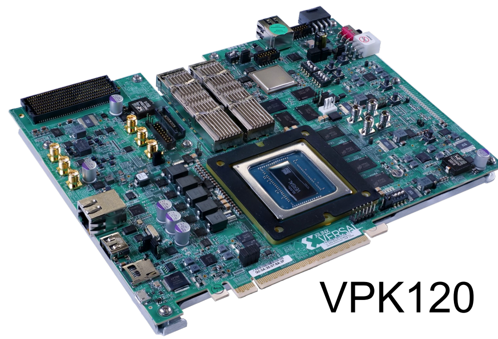
GTYP/GTM Mapping

- **Requirements**
  - TTC link: GTYP
  - Data links: 48 GTYP
  - 100GbE: 4 GTM
- **Resources**
  - GTYP: 68
    - CPM5 for PCIe: dedicated Banks 102-105
    - TTC link: Bank 109
    - Data links: GTYP Banks 106, 110-112, Banks 207-212, Banks 200-201
  - GTM: 20
    - 1 of Banks 202~206 is used for 100GbE
- **Hard IP**
  - CPM
  - PCIE
  - MRMAC: 100GbE, 4*25G



Block diagram of FLX-155 FPGA by Carlo

CPM5

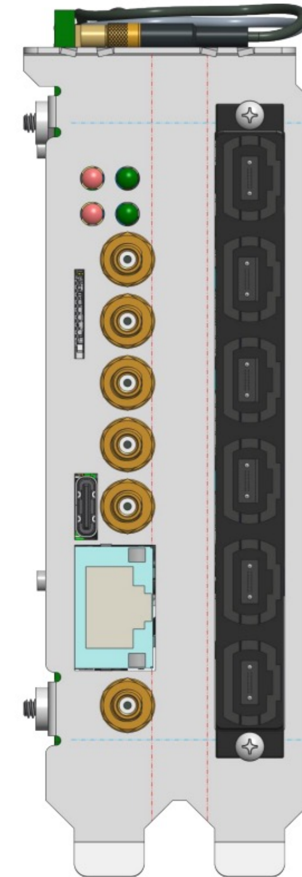

VPK120

- CPM5
  - GTYP Banks: 102~105
  - CPM5 has dedicated connectivity to a specific set of four GTYP quads which are adjacent to each other, and adjacent to CPM5
- Either PCIE PL or CPM5 has to be selected for PCIe
  - CPM5 is preferred
  - Loan VPK120 is being tested to evaluate CPM5
- Discuss with Xilinx/Avnet engineers to select which grade of FPGA could be better for ATLAS and other applications with PCIe Gen5.
  - -2MH is OK in principle, but -3H is recommended by AMD/Xilinx
  - Waiting for quotation of -3H devices. The price for -3H is probably ~15% higher than -2M.

```
root@felix-morty:/home/felix# lspci -vvd:b03f
01:00.0 Memory controller: Xilinx Corporation Device b03f
        Subsystem: Xilinx Corporation Device 0007
        Control: I/O- Mem+ BusMaster+ SpecCycle- MemWINV- VGASnoop- ParErr- Stepping- SERR- FastB2B- DisINTx-
        Status: Cap+ 66MHz- UDF- FastB2B- ParErr- DEVSEL=fast >TAbort- <TAbort- <MAbort- >SERR- <PERR- INTx-
        Latency: 0, Cache Line Size: 64 bytes
        NUMA node: 0
        Region 0: Memory at f6480000 (64-bit, non-prefetchable) [size=512K]
        Region 2: Memory at f6560000 (64-bit, non-prefetchable) [size=128K]
        Capabilities: [40] Power Management version 3
                Flags: PMEClk- DSI- D1+ D2- AuxCurrent=0mA PME(D0+,D1+,D2-,D3hot+,D3cold+)
                Status: D0 NoSoftRst+ PME-Enable- DSel=0 DScale=0 PME-
        Capabilities: [60] MSI-X: Enable- Count=8 Masked-
                Vector table: BAR=0 offset=00050000
                PBA: BAR=0 offset=00054000
        Capabilities: [70] Express (v2) Endpoint, MSI 00
                DevCap: MaxPayload 512 bytes, PhantFunc 0, Latency L0s <64ns, L1 <1us
                        ExtTag+ AttnBtn- AttnInd- PwrInd- RBE+ FLReset+ SlotPowerLimit 75.000W
                DevCtl: CorrErr+ NonFatalErr+ FatalErr+ UnsupReq-
                        RlxdOrd+ ExtTag+ PhantFunc- AuxPwr- NoSnoop+ FLReset-
                        MaxPayload 512 bytes, MaxReadReq 512 bytes
                DevSta: CorrErr+ NonFatalErr- FatalErr- UnsupReq+ AuxPwr- TransPend-
                LnkCap: Port #0, Speed 32GT/s, Width x8, ASPM not supported
                        ClockPM- Surprise- LLActRep- BwNot- ASPMOptComp+
                LnkCtl: ASPM Disabled; RCB 64 bytes Disabled- CommClk+
                        ExtSynch- ClockPM- AutWidDis- BWInt- AutBWInt-
                LnkSta: Speed 32GT/s (ok), Width x8 (ok)
                        [illegible] BWMgmt- ABWMgmt-
                DevCap2: Completion Timeout: Range BC, TimeoutDis+, NROPrPrP-, LTR+
                         10BitTagComp+, 10BitTagReq+, OBFF Not Supported, ExtFmt-, EETLPPrefix-
                         EmergencyPowerReduction Not Supported, EmergencyPowerReductionInit-
                         FRS-, TPHComp-, ExtTPHComp-
                         AtomicOpsCap: 32bit+ 64bit+ 128bitCAS+
                DevCtl2: Completion Timeout: 50us to 50ms, TimeoutDis-, LTR+, OBFF Disabled
                         AtomicOpsCtl: ReqEn-
                LnkCtl2: Target Link Speed: 32GT/s, EnterCompliance- SpeedDis-
                         Transmit Margin: Normal Operating Range, EnterModifiedCompliance- ComplianceSOS-
                         Compliance De-emphasis: -6dB
                LnkSta2: Current De-emphasis Level: -6dB, EqualizationComplete+, EqualizationPhase1+
                         EqualizationPhase2+, EqualizationPhase3+, LinkEqualizationRequest-
        Capabilities: [100 v1] Advanced Error Reporting
                UESta:  DLP- SDES- TLP- FCP- CmpltTO- CmpltAbrt- UnxCmplt- RxOF- MalfTLP- ECRC- UnsupReq+ ACSViol-
                UEMsk:  DLP- SDES- TLP- FCP- CmpltTO- CmpltAbrt- UnxCmplt- RxOF- MalfTLP- ECRC- UnsupReq+ ACSViol-
                UESvrt: DLP+ SDES+ TLP- FCP+ CmpltTO+ CmpltAbrt- UnxCmplt+ RxOF+ MalfTLP+ ECRC- UnsupReq- ACSViol-
                CESta:  RxErr- BadTLP- BadDLLP- Rollover- Timeout- AdvNonFatalErr+
                CEMsk:  RxErr- BadTLP- BadDLLP- Rollover- Timeout- AdvNonFatalErr-
                AERCap: First Error Pointer: 00, ECRCGenCap- ECRCGenEn- ECRCChkCap- ECRCChkEn-
                        MultHdrRecCap- MultHdrRecEn- TLPPfxPres- HdrLogCap-
                HeaderLog: 00000000 00000000 00000000 00000000
        Capabilities: [148 v1] Single Root I/O Virtualization (SR-IOV)
                IOVCap: Migration-, Interrupt Message Number: 000
                IOVCtl: Enable- Migration- Interrupt- MSE- ARIHierarchy+
```

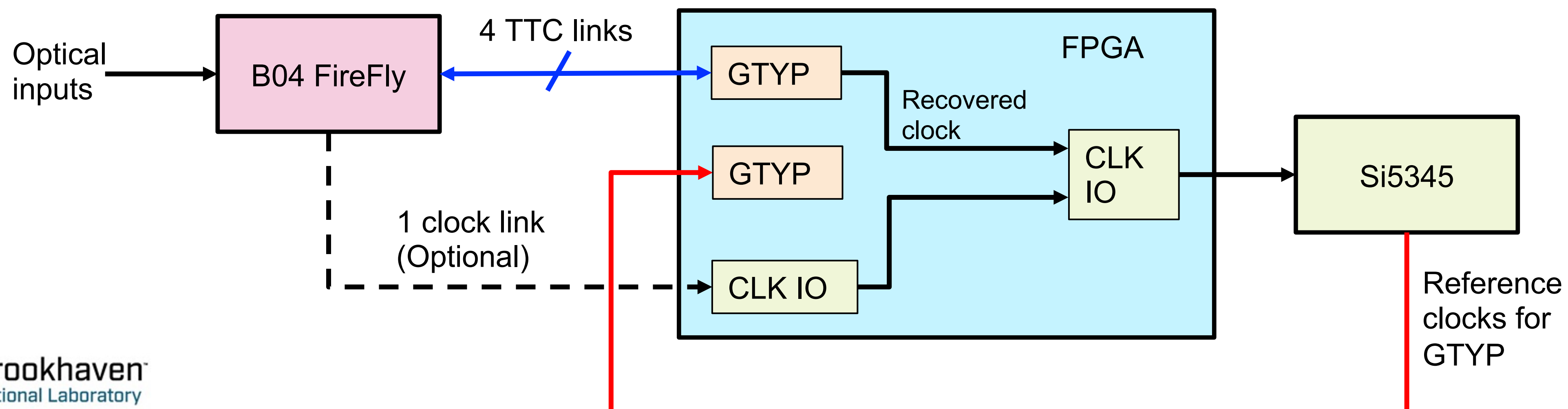
Electrical IOs on Front Panel

- Connectors on Front Panel
  - MMCX is preferred
  - SMA is OK, but may only be partially installed
- Input
  - One NIM input NIM -> LVDS to FPGA
  - Two 3.3V LVTTL/LVCMOS-> LVDS to FPGA
- Output
  - One FPGA LVDS -> 3.3V LVTTL/LVCOMS
- Input/Output
  - Four 3.3V LVTTL/LVCMOS -> FPGA grouped in two parts. Each group can be set as input or output



TTC Clock Scheme

- Either recovered clock from TTC link, or clock from optical directly. Selected by jumper resistors.
- Recovered clock from TTC link
  - Connected to GTYP to get recovered clock as system clock
  - 4 TTC links on one B04
- Optional optical clock
  - To use the optical clock as system clock directly
  - One RX of B04 is connected to FPGA clock input. In this case, only 3 RX links left are connected to GTYP



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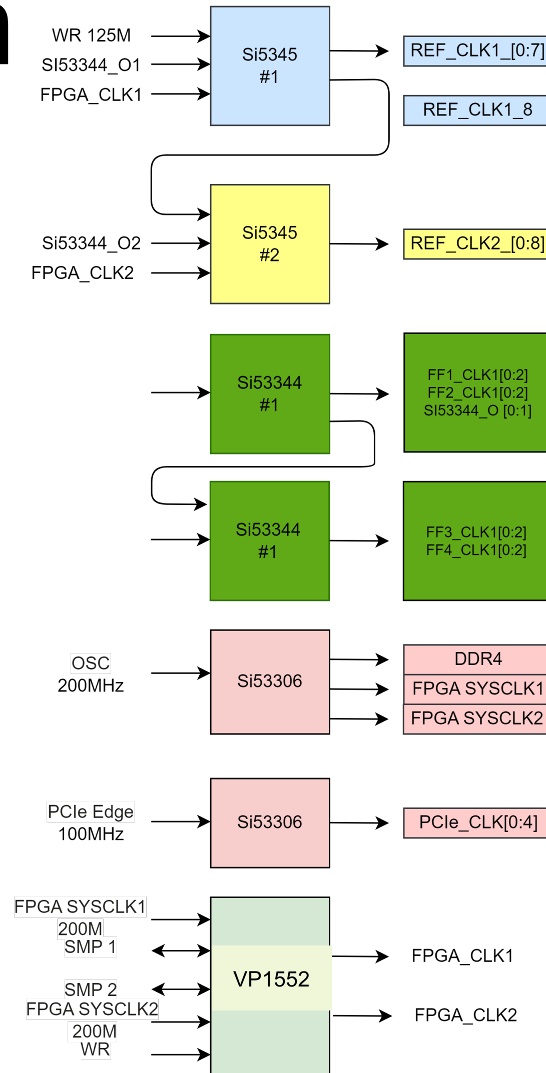
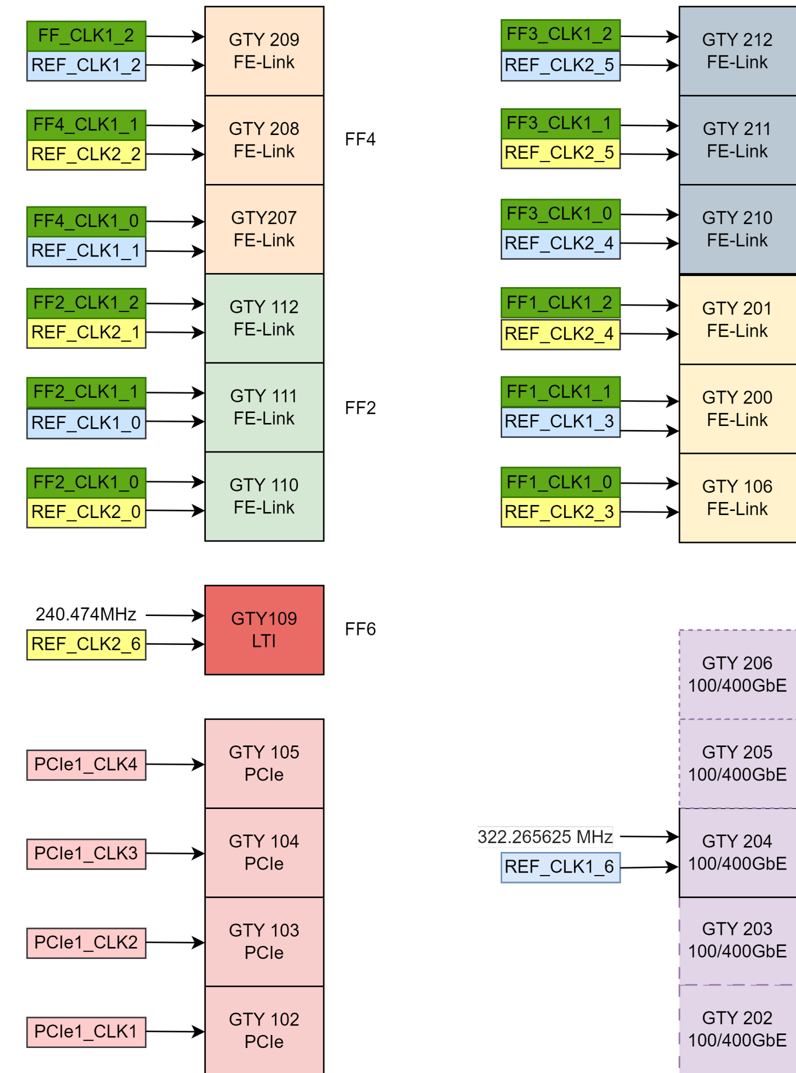
Clock Distribution

1. Two Si5345 for clock generating and distribution
2. 156.25MHz as main source of Si5345 for on board clock
   a. Interlaken
   b. Link test
3. 240.474MHz for LTI
4. 322.265625MHz for 100GbE





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FPGA Power Estimate

Flavour	Channels	Remark	LUT	FF	BRAM	URAM	On chip Power estimation
GBT	24	Dynamic	65.06%	44.60%	36.40%	45.35%	50.981W
GBT	24	semistatic	44.16%	27.01%	43.01%	51.35%	45.668W
FULL	24		44.28%	30.16%	39.39%	49.81%	50.216W
LPGBT	24	Dynamic	55.41%	27%	49.78%	49.81%	47.971W
STRIPS	24		53.39%	31.61%	59.74%	57.14%	49.885W
PIXEL	24		37.05%	33.48%	36.11%	49.81%	50.639W
INTERLAKEN	24		10.62%	9.2%	19.87%	44.27%	49.390W
GBT	36	semistatic, **failed routes**	64.24%	38.02%	63.79%	67.95%	51.649W
PIXEL	36		54.74%	38.58%	61.14%	66.41%	54.276W
PIXEL	48	placement failed	69.85%	66.19%	60.67%	71.48%	61.466W
LTDB	48		30.69%	21.62%	35.93%	83.94%	52.183W

Power Estimate (W)	VP1552-VSVA3340-2MP-E-S	VP1552-VSVA3340-2LP-E-S
Generic 2	91.946	77.912
48-ch GBT	73.753	64.556
48-ch LPGBT	72.682	63.792
48-ch STRIP	71.005	62.603
48-ch Interlaken	85.122	72.919

- Generic app: Resources: 70%; Clock: 100MHz (80%) + 250MHz (20%)
- Others: simply double resources of 24-ch mode on FLX182
- Take max. power consumption, as shown in generic 2 for power design

Power Consumption

POWER RAIL	VOLTAGE(V)	FPGA	Y12_25G (4 PAIRS)	B04_25G (2PCS)	SI5345 (2 PCS)	DDR4	QSPI (2 PCS)	DP83867	MISC	TOTAL(A)	PWR(W)	NOTE
VCCINT_0V8	0.8	75.496								75.496	60.3968	
VCCINT_0V88	0.88	7.933								7.933	6.98104	
PHY_VDD1PV0	1							0.11		0.11	0.11	FROM 2.5
VCC1V2	1.2	0.466				2				2.466	2.9592	
VCC1V5	1.5	0.418							0.5	0.918	1.377	combine with vccaux 1.5
VCCAUX1V5	1.5	6.932								6.932	10.398	combine with VCC1V5
VCC1V8	1.8	0.903		1.4	0.37			0.1	0.5	3.273	5.8914	
VCC2V5	2.5					0.35		0.14		0.49	1.225	
VCC3V3	3.3		10	0.7	0.25		0.2		0.5	11.65	38.445	
VCC3V8	3.8		2							2	7.6	
MGTAVCC	0.92	7.87								7.87	7.2404	
MGTAVTT	1.2	13.393								13.393	16.0716	
MGTYVCCAUX	1.5	0.339								0.339	0.5085	
DDR4_VTT	0.6					1.5				1.5	0.9	
		total: FPGA 104.41W								Total	160.10394	

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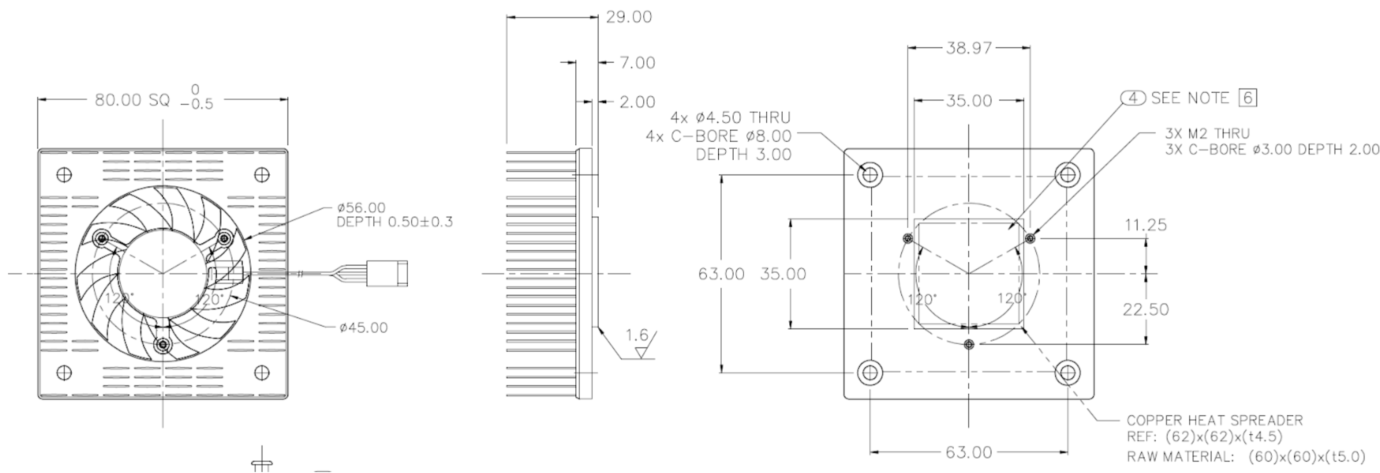
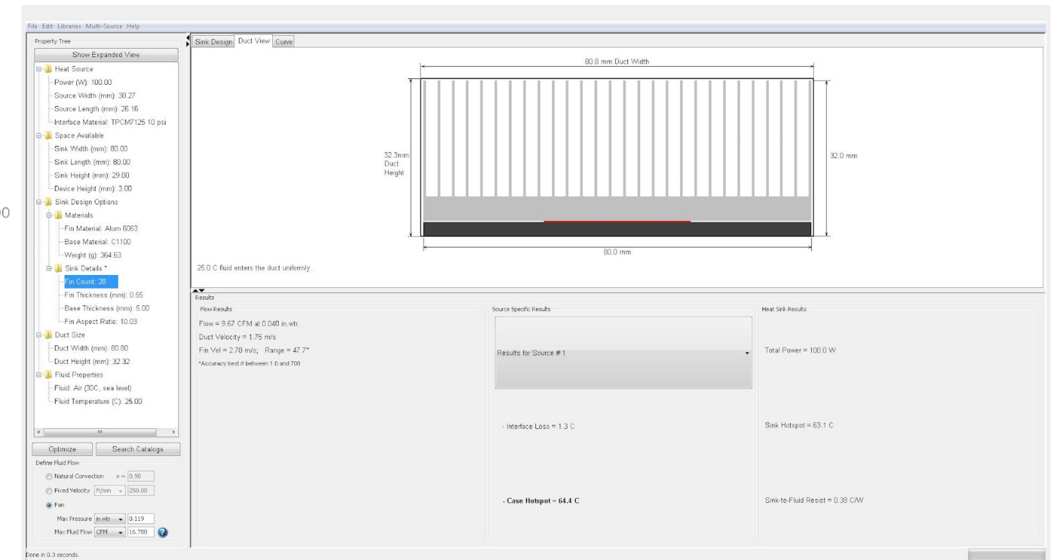
Power Scheme

#	Module	Module Rail	Nominal Voltage/V	Power Rail	PMBUS	Board Power Rails	Current Rating/A	Current Consumption/A	Sequence	Efficiency	Power/W	NOTE
1	LTM4700	1&2	0.8	VCCINT	Y	VCC_INT, VCC_RAM,VCC_SOC, VCC_IO,	100	75.496	2	0.85	71.1	
2	LTM4638	1	0.88	VCC0V88	N	VCC_PSLP, VCC_PSFP, VCC_PMC, VCC_CPM5	15	7.933	2	0.87	8	
3	LTM4638	1	1.2	MGTAVTT	N	MGTYAVTT,MGTAVTTRCAL	15	13.393	6	0.91	17.7	
4	LTM4638	1	1.2	VCC1V2	N	VCC1V2, VCCIO_1V2	15	2.466	1	0.91	3.3	reference for DDR4_VTT
5	LTM4638	1	0.92	MGTAVCC	N	MGTY_AVCC	15	7.87	4	0.87	8.3	
6	LTM4638	1	1.8	VCC1V8	N	VCC1V8	15	3.273	1	0.8	7.4	
7	LTM4638	1	1.5	VCC1V5	N	VCCAUX, VCCAUX_PMC, VCCAUX_SMON	15	7.85	3	0.83	14.2	
8	LTM4638	1	3.3	VCC3V3	N	VCC3V3	15	11.65	NA, SET TO 0	0.91	42.2	
	LTM4642	1	3.8	VCC3V8	N	VCC3V8	4	2	NA, SET TO 0	0.8	9.5	
9		2	2.5	VCC2V5	N	VCC2V5	4	2.5	NA, SET TO 0	0.8	7.8	generate mgtvccaux 0.5A generate ddr4_vtt 1.5
10	ADP124	1	1.5	MGTY_VCCAUX	N	MGTY_VCCAUX	0.5	0.339	5	0.8	0	from VCC2V5
11	TPS51200	1	0.6	DDR4_VTT_PL	N	DDR4_VTT_PL	3	1.5	2	0.85	0	FROM VCC2V5
12	TPSM5601	1	5	VCC5V	N	VCC5V	1.5	0.5	NA, SET TO 0	0.92	2.7	
13	LMR70503	1	-5	VCC5VM	N	VCC5VM	0.27	-0.1	NA, SET TO 0	0.75	0.7	
										total	192.8	

FLX-155 Heatsink Design - ULP80-29 Active





- Heatsink 29 mm, Fan is embedded in the heatsink, total 29 mm.
- Screw based assembly
- Thermal resistance is 0.38 C/W. So with 25 °C airflow, the die temperature is about 63.1 °C at 100 Watts.

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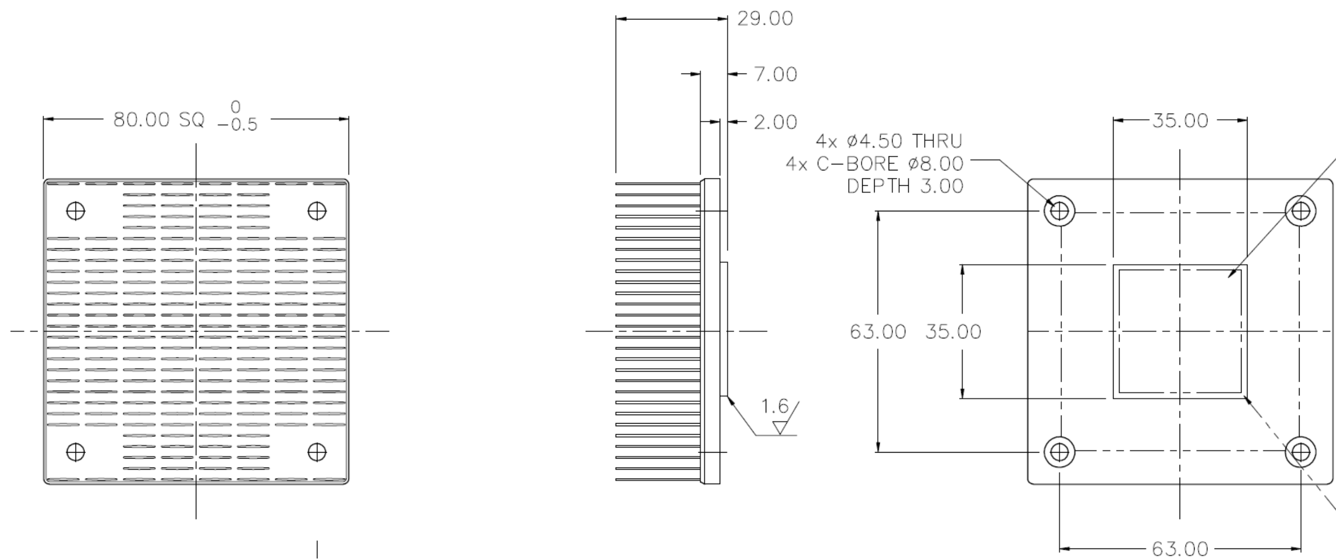
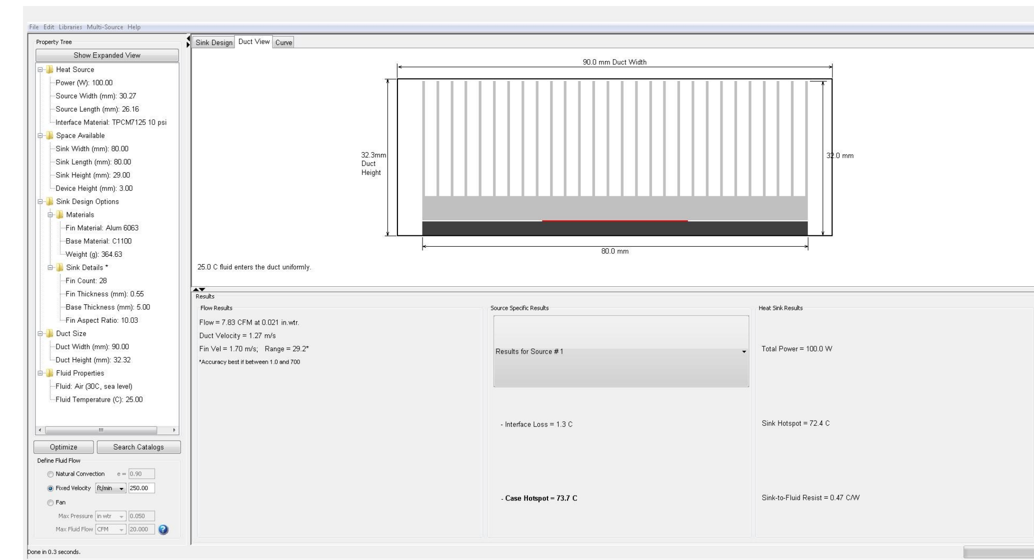
FLX-155 Heatsink Design - ULP80-29 Passive





- Heatsink total height is 29 mm, no Fan.
- Screw based assembly
- Thermal resistance is 0.47 C/W at 250 LFM air flow. So with 25 °C air flow, the die temperature is about 73.7 °C at 100 Watts.

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Stack-up

The stack-up is the same as what has been used for FLX-182B

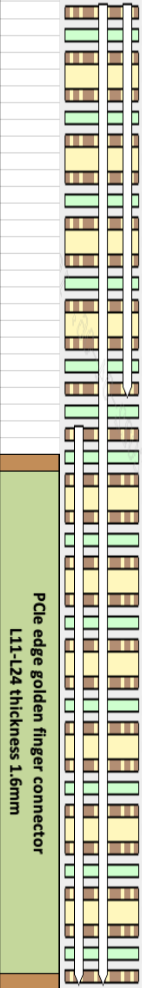
Stackup Report

Job Name:000-W24-TJ-101306824-IO-1814-1A-220418TL-230805

Finish Board Thickness(mm):3+/-0.28

Stackup Control Required:

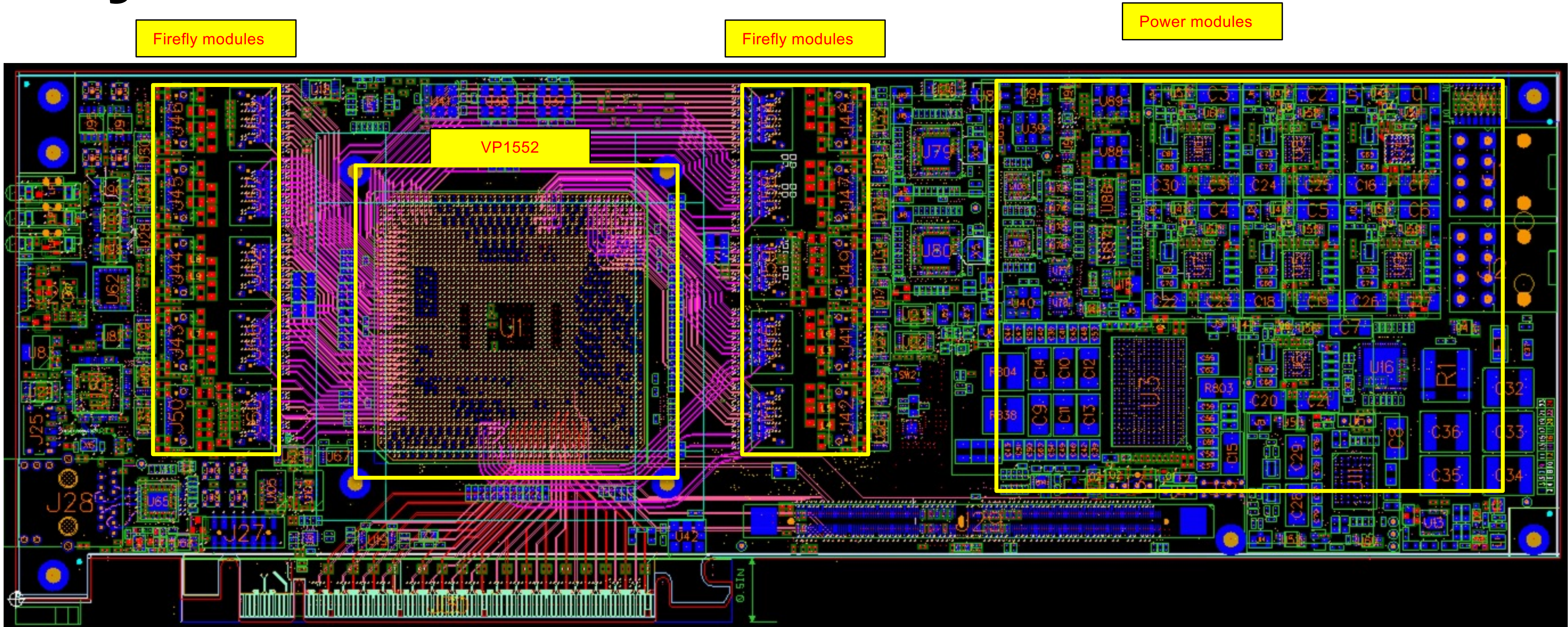
Layer Index	Stackup Buildup	PP Name And RC	Finished Thickness(mm)	Dielectric Thickness(mm)	Dielectric Thickness(Mil/mm)	Finish Cu Thk(oz)	DK(1GHz)	Material Family	Copper Rate(%)
L1	Foil(HTE)		0.04			0.5oz+Plating			31.00
	PP	PP(1080)RC68	0.07	0.073	2.861(0.073)		2.91	EM890K	
L2 Core L3	HVLP Core HVLP	1*1078	0.03 0.076 0.031	0.076	2.992(0.076)	1oz 1oz	2.93	EM890K	86.00 79
	PP PP	PP(1035)RC77 PP(1035)RC77	0.12	0.123	4.848(0.123)		2.82	EM890K EM890K	
L4 Core L5	HVLP Core HVLP	1*1078	0.03 0.076 0.015	0.076	2.992(0.076)	1oz 0.5oz	2.93	EM890K	86.00 54
	PP PP	PP(1035)RC77 PP(1035)RC77	0.13	0.125	4.921(0.125)		2.82	EM890K EM890K	
L6 Core L7	HVLP Core HVLP	1*1078	0.02 0.076 0.015	0.076	2.992(0.076)	0.5oz 0.5oz	2.93	EM890K	86.00 13
	PP PP	PP(1035)RC77 PP(1035)RC77	0.12	0.119	4.679(0.119)		2.82	EM890K EM890K	
L8 Core L9	HVLP Core HVLP	1*1078	0.02 0.076 0.015	0.076	2.992(0.076)	0.5oz 0.5oz	2.93	EM890K	86.00 43
	PP PP	PP(1035)RC77 PP(1035)RC77	0.13	0.125	4.939(0.125)		2.82	EM890K EM890K	
L10	Foil(HTE)		0.04			0.5oz+Plating			86.00
	PP PP PP	PP(1080)RC68 PP(1035)RC77 PP(1080)RC68	0.18	0.184	7.240(0.184)		2.88	EM890K EM890K EM890K	
L11	Foil(HTE)		0.04			0.5oz+Plating			8.00
	PP	PP(1080)RC68	0.07	0.073	2.873(0.073)		2.91	EM890K	
L12 Core L13	HVLP Core HVLP	2X1035	0.03 0.102 0.031	0.102	4.016(0.102)	1oz 1oz	2.91	EM890K	87.00 79
	PP PP	PP(1035)RC77 PP(1035)RC77	0.12	0.121	4.751(0.121)		2.82	EM890K EM890K	
L14 Core L15	HVLP Core HVLP	1*1078	0.03 0.076 0.031	0.076	2.992(0.076)	1oz 1oz	2.93	EM890K	78.00 86
	PP PP	PP(1035)RC77 PP(1035)RC77	0.12	0.118	4.650(0.118)		2.82	EM890K EM890K	
L16 Core L17	HVLP Core HVLP	1*1078	0.015 0.076 0.015	0.076	2.992(0.076)	0.5oz 0.5oz	2.93	EM890K	23.00 86
	PP PP	PP(1035)RC77 PP(1035)RC77	0.12	0.122	4.815(0.122)		2.82	EM890K EM890K	
L18 Core L19	HVLP Core HVLP	1*1078	0.015 0.076 0.015	0.076	2.992(0.076)	0.5oz 0.5oz	2.93	EM890K	36.00 86
	PP PP	PP(1035)RC77 PP(1035)RC77	0.12	0.118	4.644(0.118)		2.82	EM890K EM890K	
L20 Core L21	HVLP Core HVLP	1*1078	0.015 0.076 0.015	0.076	2.992(0.076)	0.5oz 0.5oz	2.93	EM890K	7.00 87
	PP PP	PP(1035)RC77 PP(1035)RC77	0.12	0.121	4.774(0.121)		2.82	EM890K EM890K	
L22 Core L23	HVLP Core HVLP	2X1035	0.015 0.102 0.015	0.102	4.016(0.102)	0.5oz 0.5oz	2.91	EM890K	28.00 86
	PP	PP(1080)RC68	0.08	0.075	2.949(0.075)		2.91	EM890K	
L24	Foil(HTE)		0.04			0.5oz+Plating			39.00



Impedance Control Required:

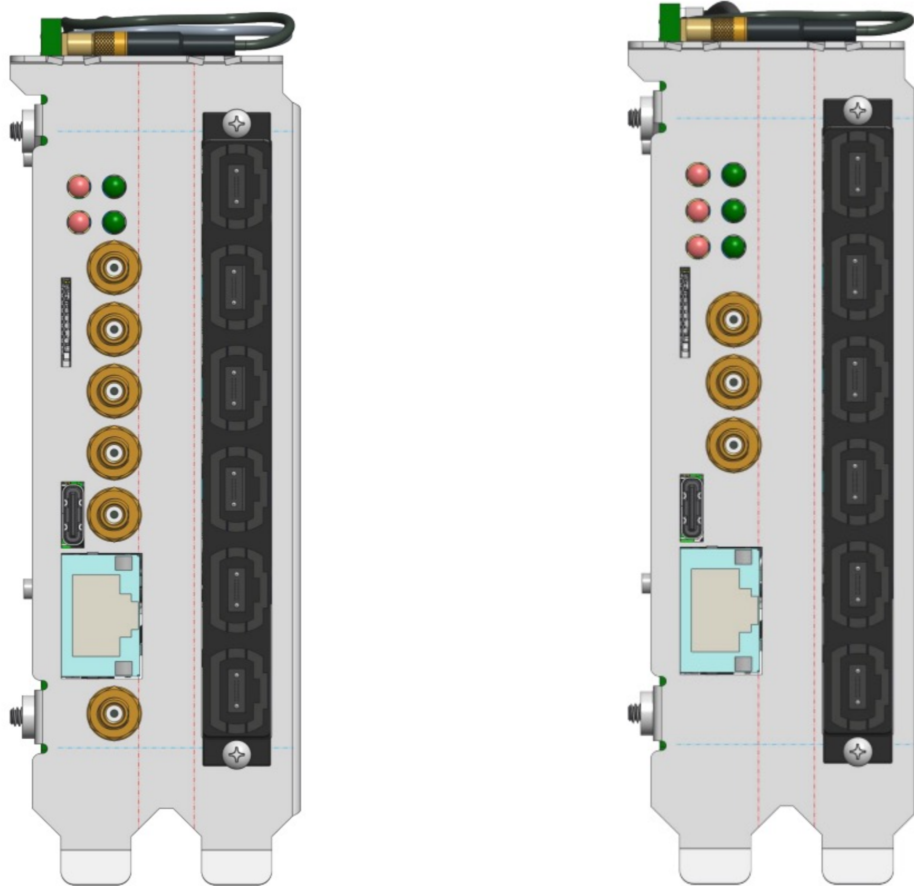
Impedance Layer	Impedance Model	Reference Layer	Required Line Width/Spacing(Mil)	Finish Line Width/Spacing(Mil)	Calculated Impedance(Ω)
L1	se_coated_microstrip	L2	7	5.6	50+/-10%
L5	se_stripline	L4/L6	4.3	4.3	50+/-10%
L7	se_stripline	L6/L8	4.3	4.2	50+/-10%
L9	se_stripline	L8/L10	4.3	4.3	50+/-10%
L11	se_stripline	L12/L10	4.3	4	50+/-10%
L16	se_stripline	L17/L15	4.3	4.2	50+/-10%
L18	se_stripline	L19/L17	4.3	4.3	50+/-10%
L20	se_stripline	L21/L19	4.3	4.2	50+/-10%
L22	se_stripline	L23/L21	4.3	5.2	50+/-10%
L24	se_coated_microstrip	L23	7	5.8	50+/-10%
L1	se_coated_microstrip	L2	6	8.9	39+/-5Ω
L5	se_stripline	L4/L6	3.5	6.6	39+/-5Ω
L7	se_stripline	L6/L8	3.5	6.5	39+/-5Ω
L9	se_stripline	L8/L10	3.5	6.6	39+/-5Ω
L11	se_stripline	L12/L10	3.5	6.5	39+/-5Ω
L16	se_stripline	L17/L15	3.5	6.5	39+/-5Ω
L18	se_stripline	L19/L17	3.5	6.6	39+/-5Ω
L20	se_stripline	L21/L19	3.5	6.5	39+/-5Ω
L22	se_stripline	L23/L21	3.5	7.9	39+/-5Ω
L24	se_coated_microstrip	L23	6	9.2	39+/-5Ω
L5	diff_stripline	L4/L6	3.500/3.500	3.700/3.300	95+/-10%
L7	diff_stripline	L6/L8	3.500/3.500	3.700/3.300	95+/-10%
L9	diff_stripline	L8/L10	3.500/3.500	3.700/3.300	95+/-10%
L11	diff_stripline	L12/L10	3.500/3.500	3.000/4.000	95+/-10%
L16	diff_stripline	L17/L15	3.500/3.500	3.700/3.300	95+/-10%
L18	diff_stripline	L19/L17	3.500/3.500	3.700/3.300	95+/-10%
L20	diff_stripline	L21/L19	3.500/3.500	3.700/3.300	95+/-10%
L22	diff_stripline	L23/L21	3.500/3.500	4.100/2.900	95+/-10%
L5	diff_stripline	L4/L6	5.500/4.000	5.100/4.400	85+/-10%
L7	diff_stripline	L6/L8	5.500/4.000	5.100/4.400	85+/-10%
L9	diff_stripline	L8/L10	5.500/4.000	5.100/4.400	85+/-10%
L11	diff_stripline	L12/L10	5.500/4.000	4.500/5.000	85+/-10%
L16	diff_stripline	L17/L15	5.500/4.000	5.100/4.400	85+/-10%
L18	diff_stripline	L19/L17	5.500/4.000	5.100/4.400	85+/-10%
L20	diff_stripline	L21/L19	5.500/4.000	5.100/4.400	85+/-10%
L22	diff_stripline	L23/L21	5.500/4.000	5.700/3.800	85+/-10%
L24	diff_coated_microstrip	L23	5.400/4.000	5.300/4.100	85+/-10%
L5	diff_stripline	L4/L6	3.700/4.300	3.700/4.300	100+/-10%
L7	diff_stripline	L6/L8	3.700/4.300	3.700/4.300	100+/-10%
L9	diff_stripline	L8/L10	3.700/4.300	3.700/4.300	100+/-10%
L11	diff_stripline	L12/L10	3.700/4.300	3.000/5.000	100+/-10%
L16	diff_stripline	L17/L15	3.700/4.300	3.600/4.400	100+/-10%
L18	diff_stripline	L19/L17	3.700/4.300	3.700/4.300	100+/-10%
L20	diff_stripline	L21/L19	3.700/4.300	3.600/4.400	100+/-10%
L22	diff_stripline	L23/L21	3.700/4.300	4.100/3.900	100+/-10%

Layout of FLX-155



3D Modeling

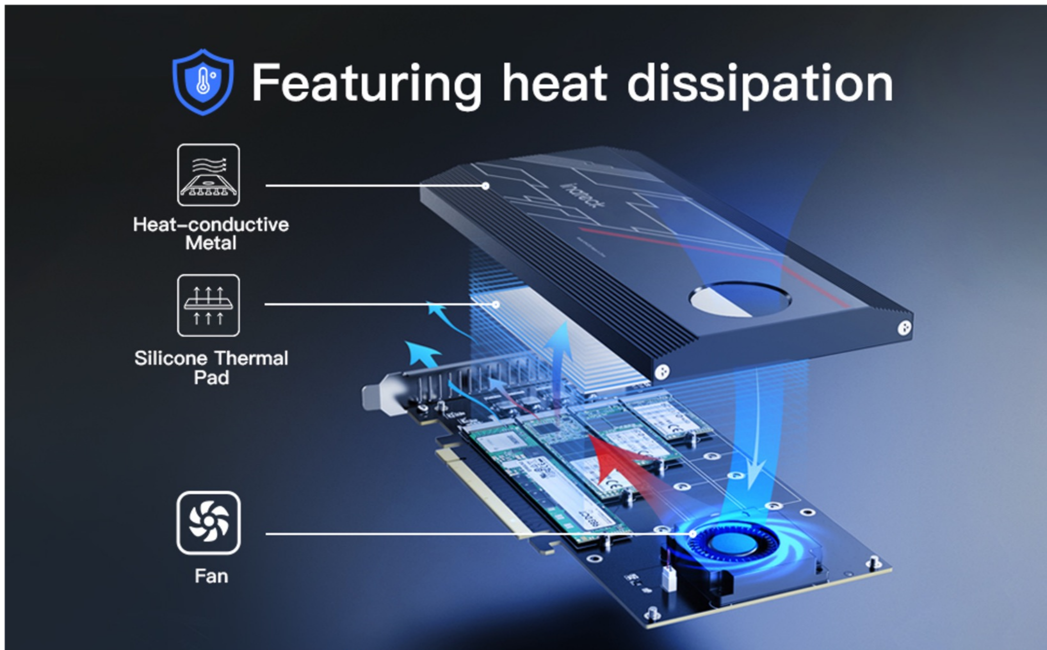
Front Panel for Different Requirements



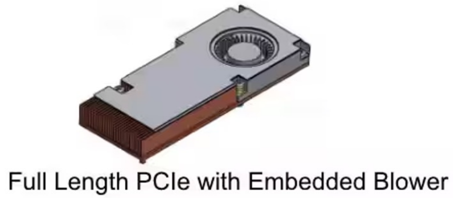
Summary

- Test results of the first FLX-182B show the hardware functionalities are all good. 46 boards production started.
- FLX-155 design is processing well.
  - Schematics is finished, power supplies could be further optimized.
  - Layout is ongoing, will be finished by end of February.
  - ATLAS PDR will be held on Feb. 1st. Then we will start fabrication, assembly. First board is expected to be tested before summer.

Backup slides

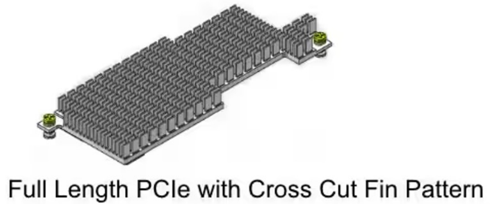


ATS PCIe Heat Sink Design Examples

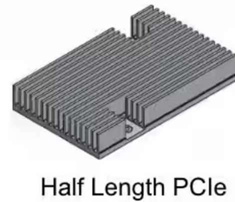


Full Length PCIe with Embedded Blower

Half Length PCIe, Black Anodized, with Embedded Blower



Full Length PCIe with Cross Cut Fin Pattern



Half Length PCIe