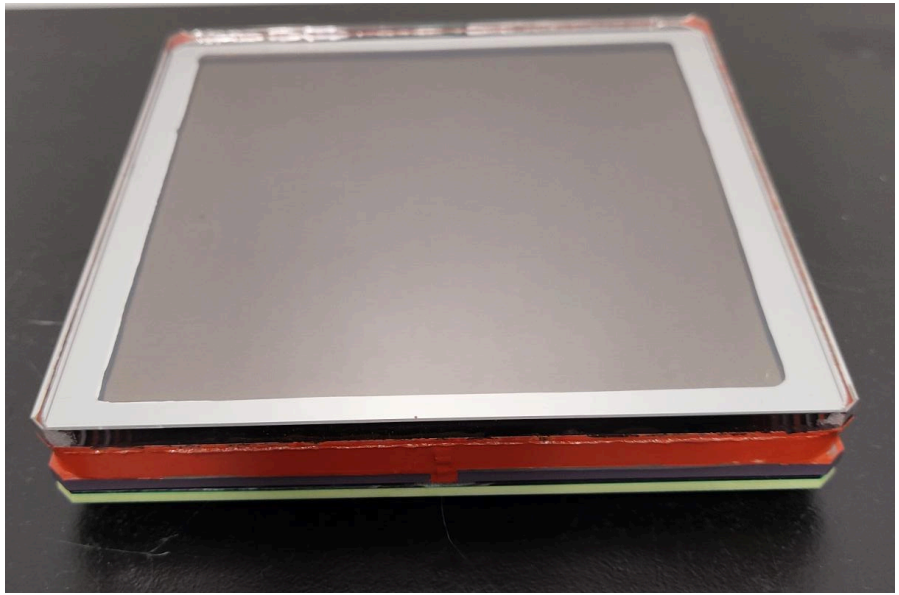
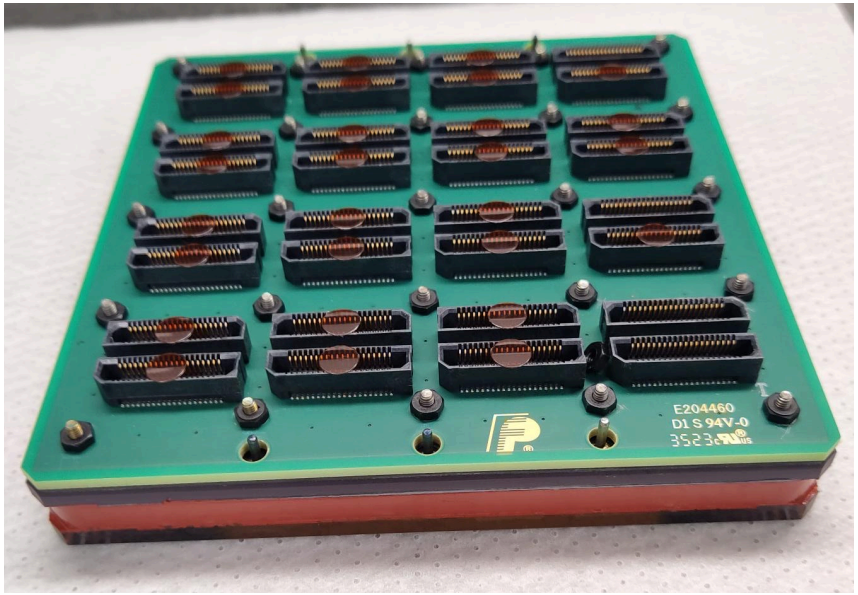
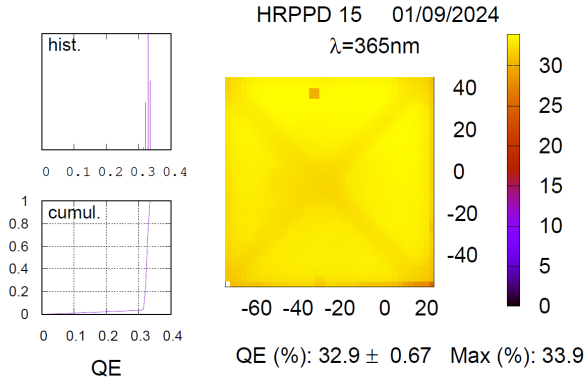
HRPPD #15 (EIC HRPPD #1)

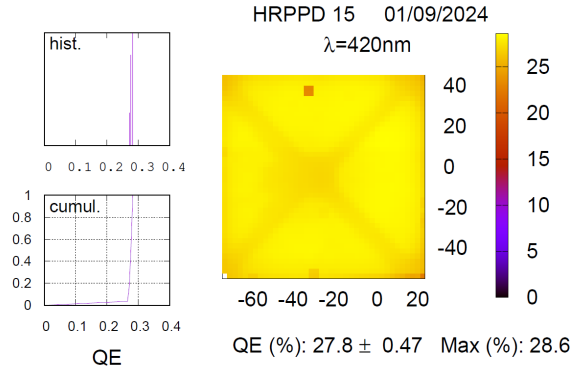


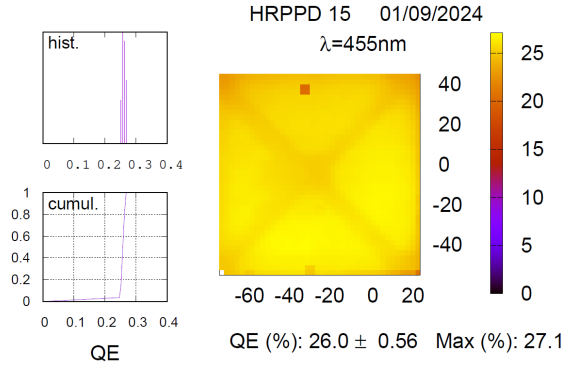


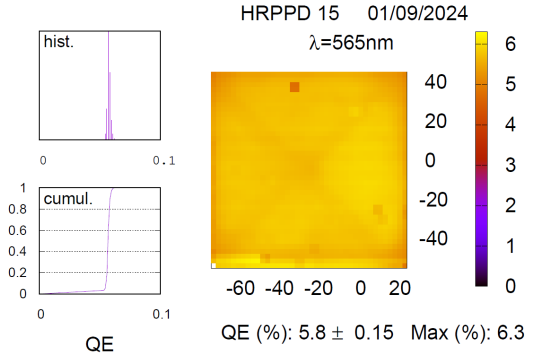
- Passed internal QA procedure at Incom
- Was shipped to JLab yesterday
  - Initial assessment will take up to one month
  - Then will be sent to BNL for systematic scans

HRPPD #15 (EIC HRPPD #1)



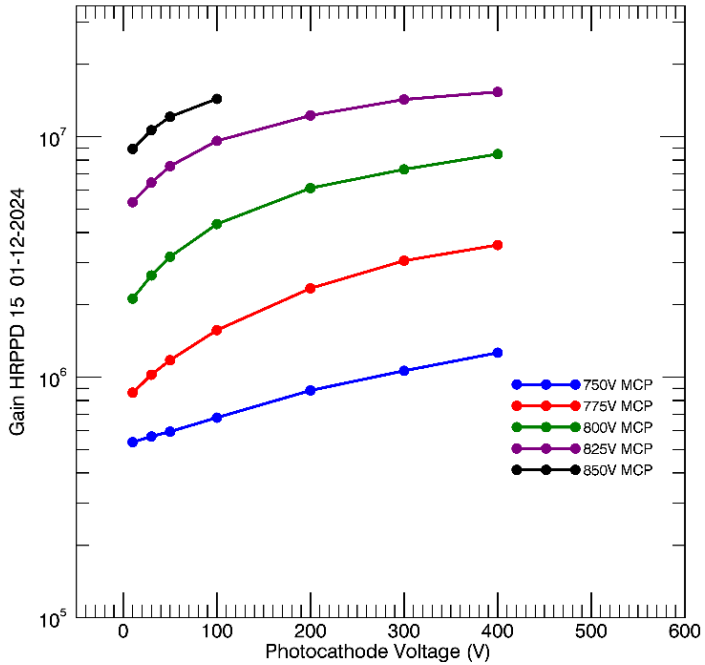


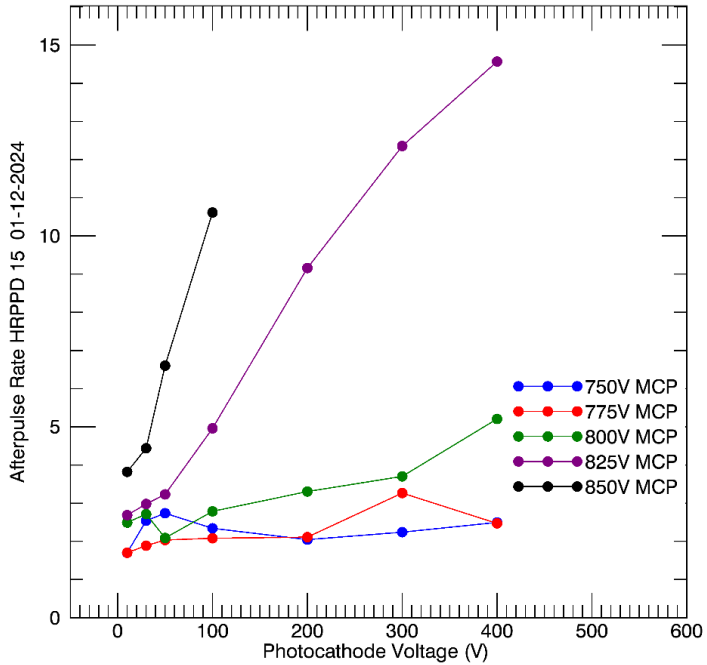




The QE scan looks very promising: ~33% @ 365nm

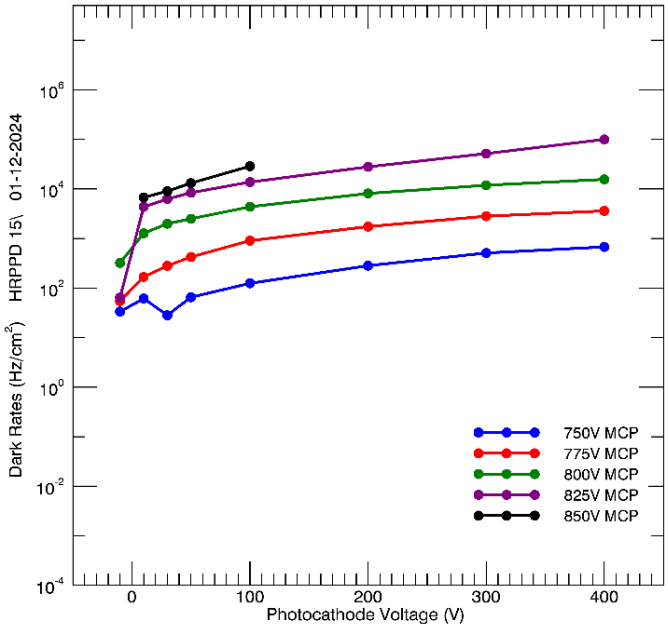
HRPPD #15 (EIC HRPPD #1)

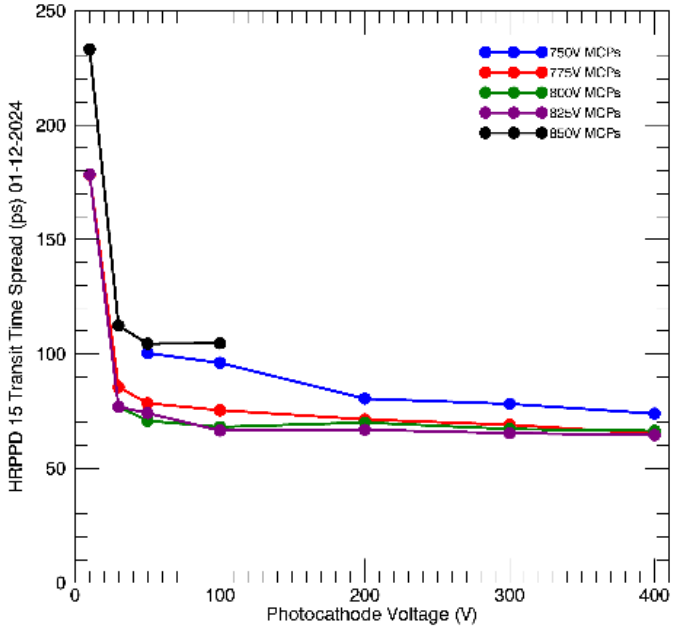




Gain few times 10^6; afterpulsing seems to be small

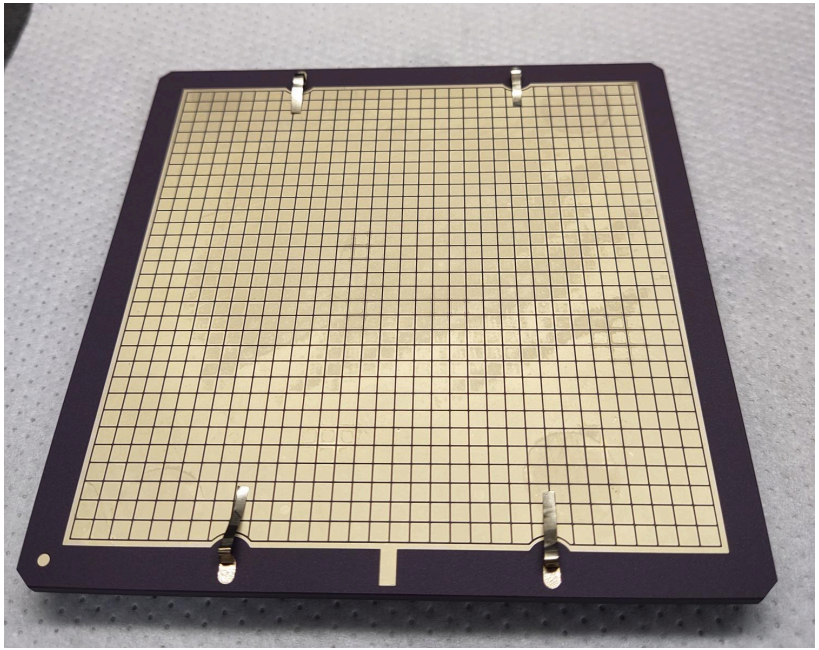
HRPPD #15 (EIC HRPPD #1)

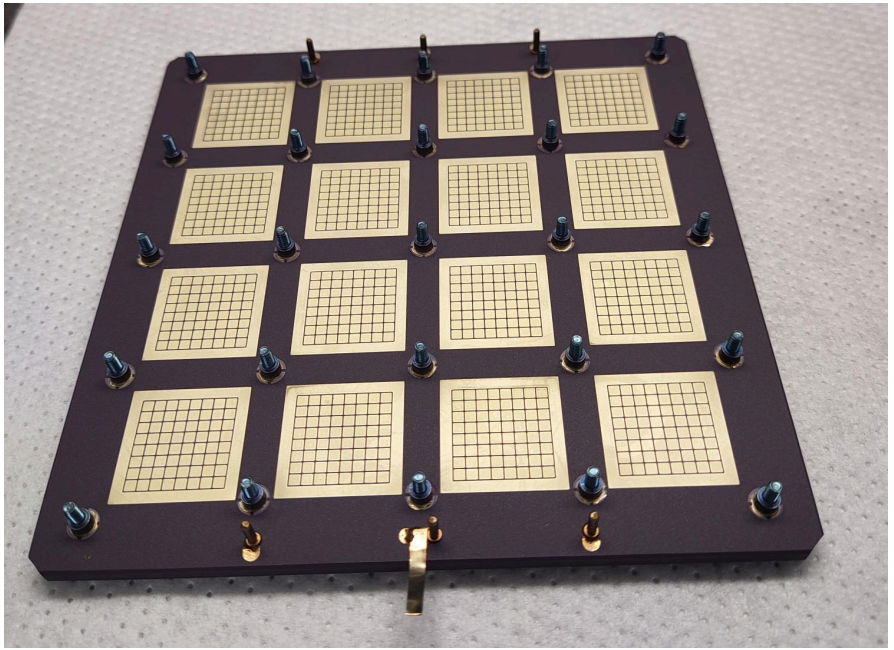




DCR few kHz/cm^2; SPE timing ~60ps

HRPPD #16 (EIC HRPPD #2 ?)

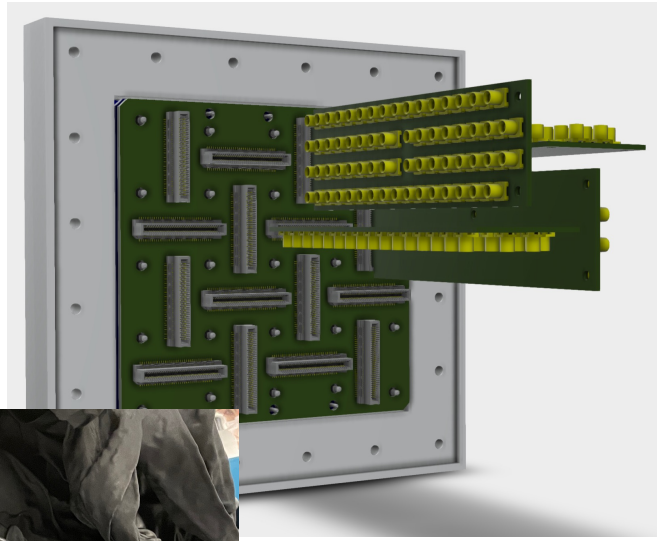


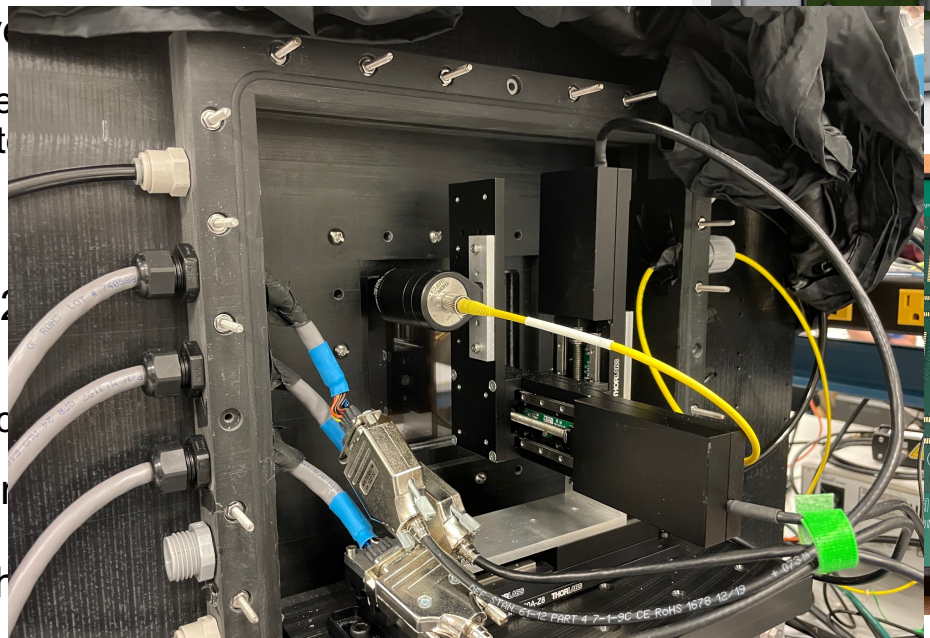


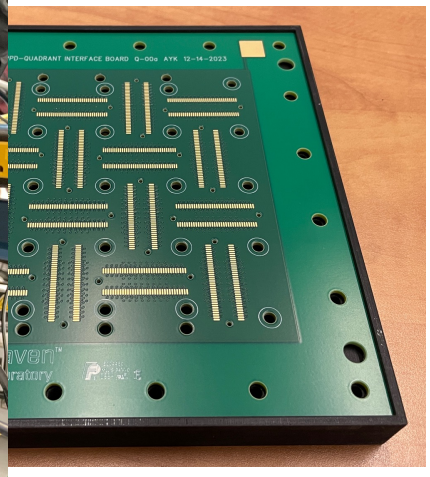
- If everything goes well, will be ready for shipment by the end of January

HRPPD evaluation procedure

- First shipped to JLab & express-tested there
  - Procedure yet to be worked out
- Then sent to BNL for systematic scans
  - A comprehensive document exists
- Then distributed ov
  - First with a passive
    the pfRICH beam t
    backplane
- Passive interface #2
  assembly process
  - Required for surfac
- Other small adapter
  dispatched, and all
  connectors are at th

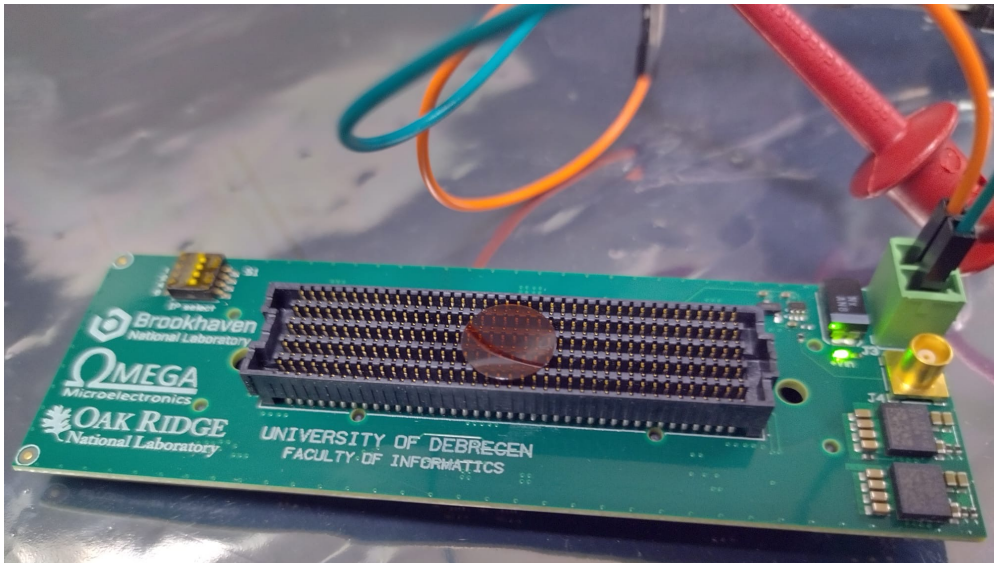


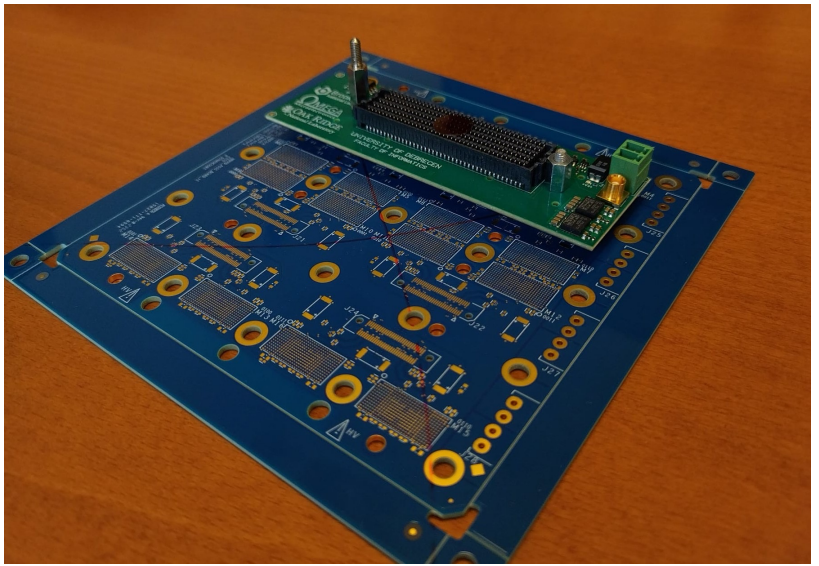




HGCROC3 ASIC / FPGA backplane

IN2P3 [OMEGA] (Pierrick, Damien), Uni Debrecen (Gabor, Miklos)
BNL (Daniel), Oak Ridge (Norbert)





- Assembled ASIC boards expected to be ready by the end of this week
- ASIC board + FMC (passive) board + KCU105 FPGA kit debugging @ Debrecen will take ~two weeks
- FPGA bare board production launched yesterday