

R&D on AC-LGAD Time-of-Flight for ePIC



Project Goal: Completing the readout chain for an AC-LGAD based TOF

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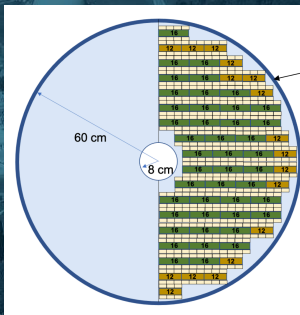
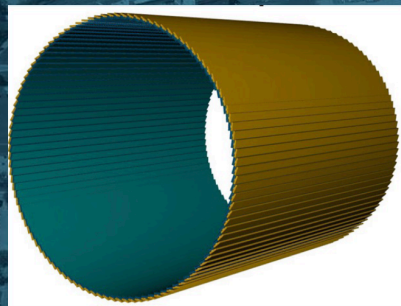
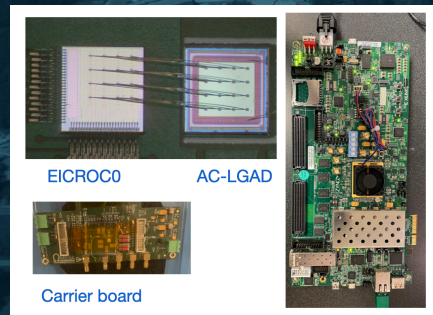
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External Collaborators:

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Wei Li (Rice)

Zhenyu Ye (UIC/LBNL)

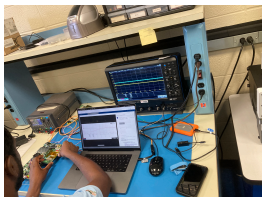


Funding: eRD109 (prototyping the RDO), Physics Department

Possible BNL group commitment: Understand the sensor + ASIC response & FPGA project: develop the RDO, make it compatible with ePIC DAQ protocol, implement the simulation

Commitments/activities/challenges (mid 2022-now)

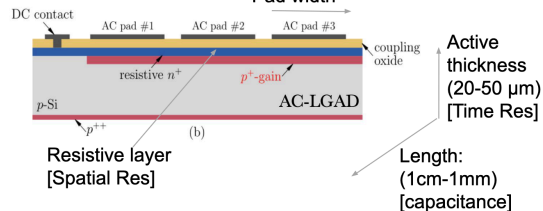
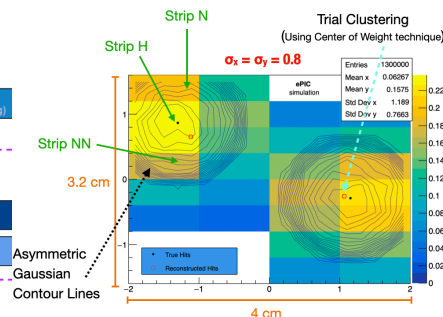
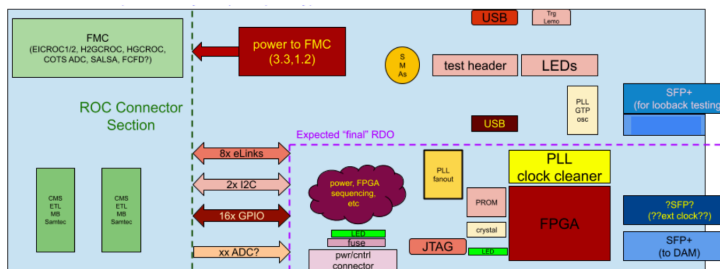
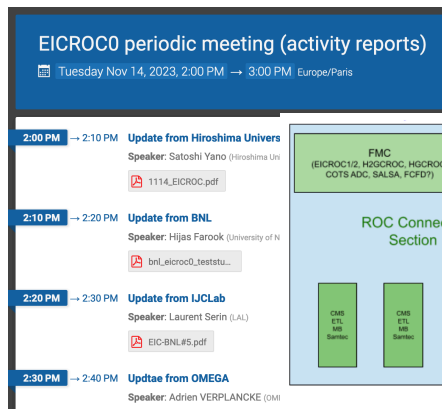
Test lab setup: BNL instrumentation



Periodic (bi-weekly) meeting on development of EICROC0 with French and Japanese group

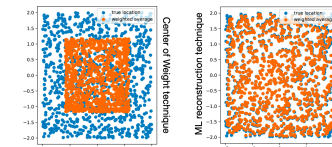
Development of prototype RDO with Rice and UIC/ LBNL

- Implement Sensor+ASIC response to ePIC simulation
- AI/ML technique to improve space/time performance



Milestones:	Milestones:
Jitter reduction,	PCB layout
cross-talk reduction	firmware
Working ADC module	EICRC
Compatibility with strip sensor	

Milestones:
PCB layout, FPGA
firmware, compatibility with
EICROC



Milestones:
Input from hardware, implement full digitization model implemented in ePIC simulation, reduce data throughput & noise reduction

Milestones: Modify sensor geometry for sensor-ASIC compatibility & TOF requirement

Pros and cons: ACLGAD based TOF (bTOF/FTOF)

	Pros	Cons	Remedy
Interest in TOF	Historically BNL heavy ion group started with interest in low-pT PID, semi-inclusive physics (STAR TOF bkg.)	Some members are moving, not enough people currently working	Need more people/support who will be interested in TOF
Opportunities in ePIC	Many lead opportunities still available with core part of project, other national labs are not taking lead roles	Recent BTOF leader has stepped down, cannot be done without strong electrical engineers, FPGA experts	Engineering FTE needed
Sensor Technology	AC-LGAD is premier tech, many future applications, BNL only fab capable US lab	No previous AC-LGAD detector, no expert in the EIC group	EIC group needs to hire or partially support AC-LGAD expert, or Inst-HEP-NP collab.
ASIC	EICROC is already available, pixel compatibility, possibly same ASIC for HRPPD (pFRICH), expertise will help	Need candidate for strip sensor: No expertise for design. Pixel ADC need work, cross talk, no streaming yet	HGCROC & FCFD could be a candidate for strip-sensor. EIC group can work closely with Inst. to modify the sensor
Readout	Couple be the major role from BNL group closely tied to DAQ group	Not possible without and FPGA expert/EE. EICROC not ready for fully functional dev.	Any TDC capable ASIC can be used to dev. ppRDO