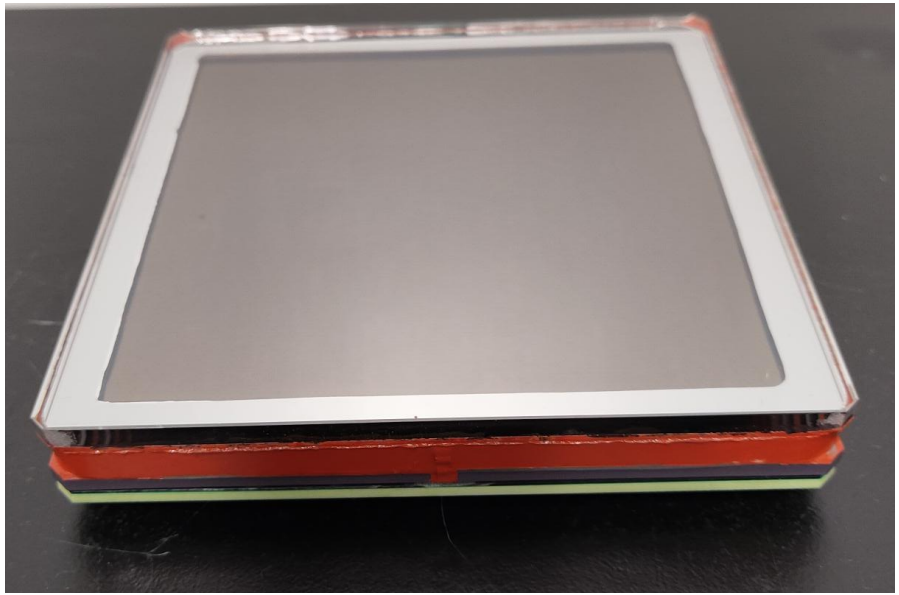
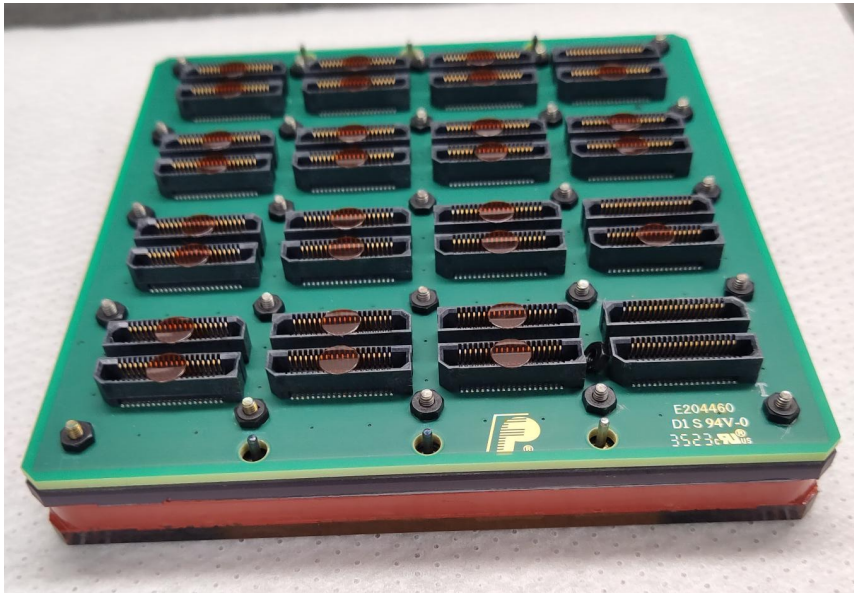
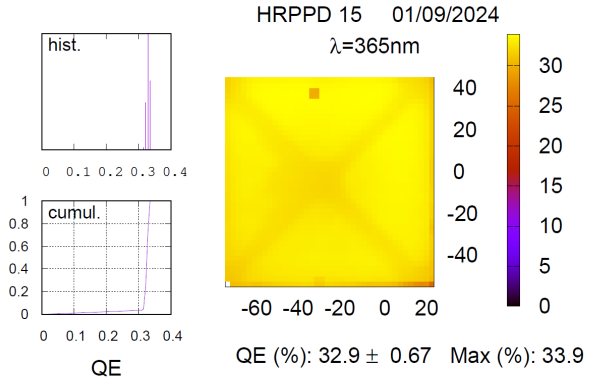
HRPPD #15 (EIC HRPPD #1)

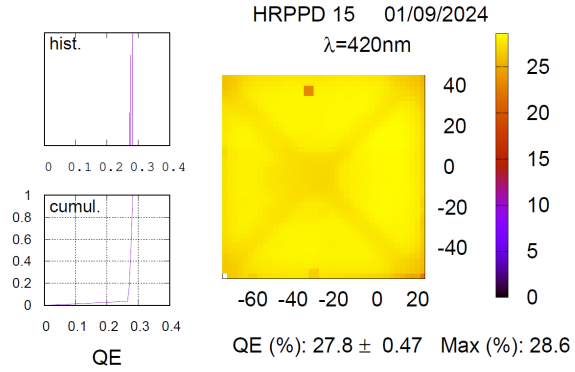


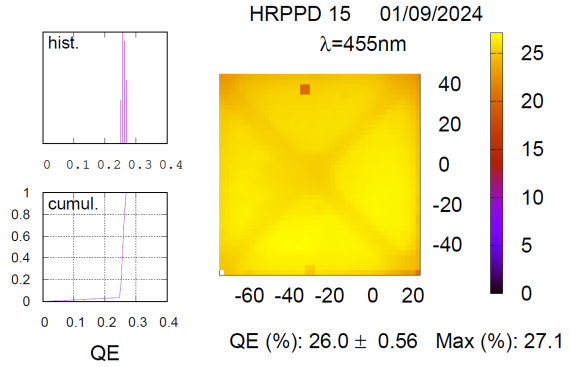


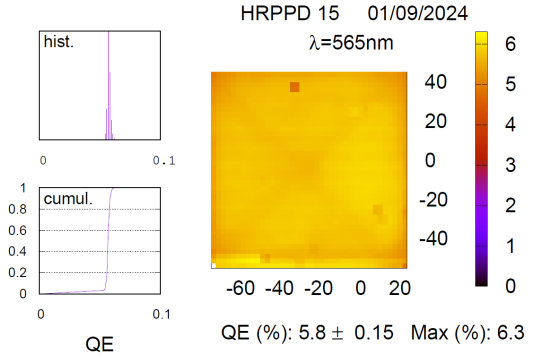
- Passed internal QA procedure at Incom
- Was shipped to JLab last week
  - Initial assessment will take up to one month
  - Then will be sent to BNL for systematic scans

HRPPD #15 (EIC HRPPD #1)



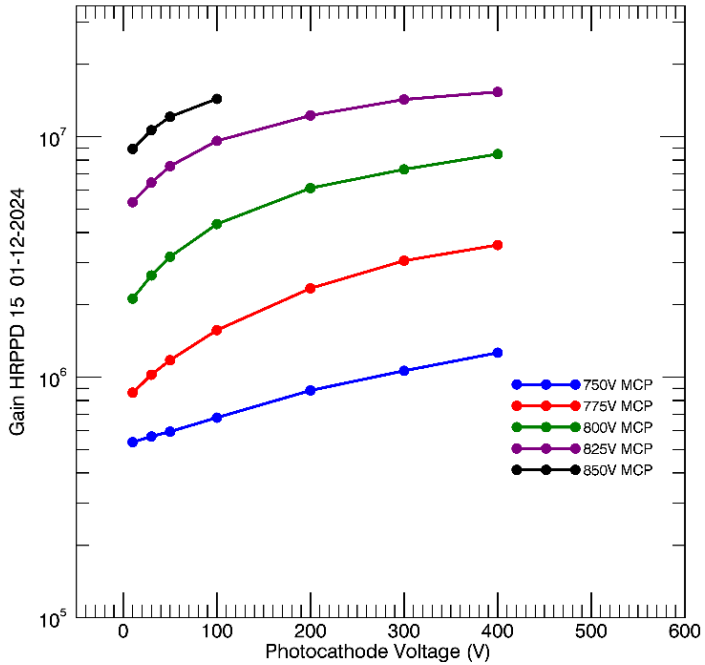


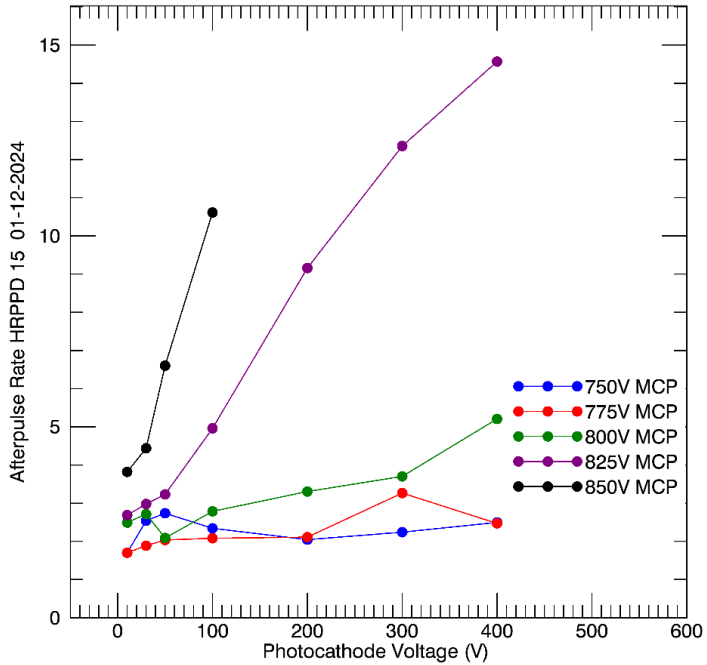




The QE scan looks very promising: ~33% @ 365nm

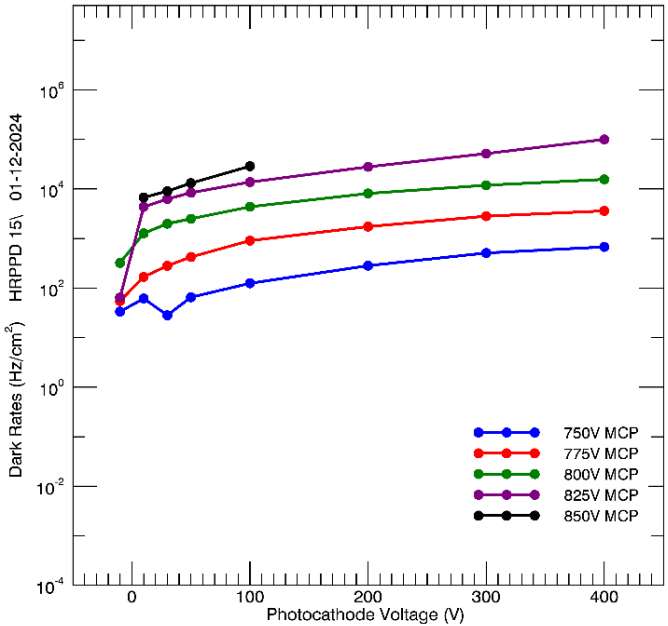
HRPPD #15 (EIC HRPPD #1)

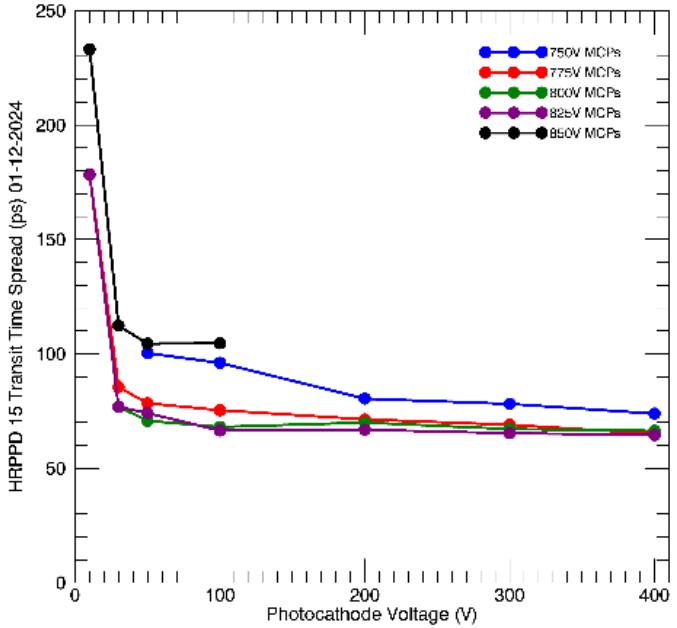




Gain few times 10^6; afterpulsing seems to be small

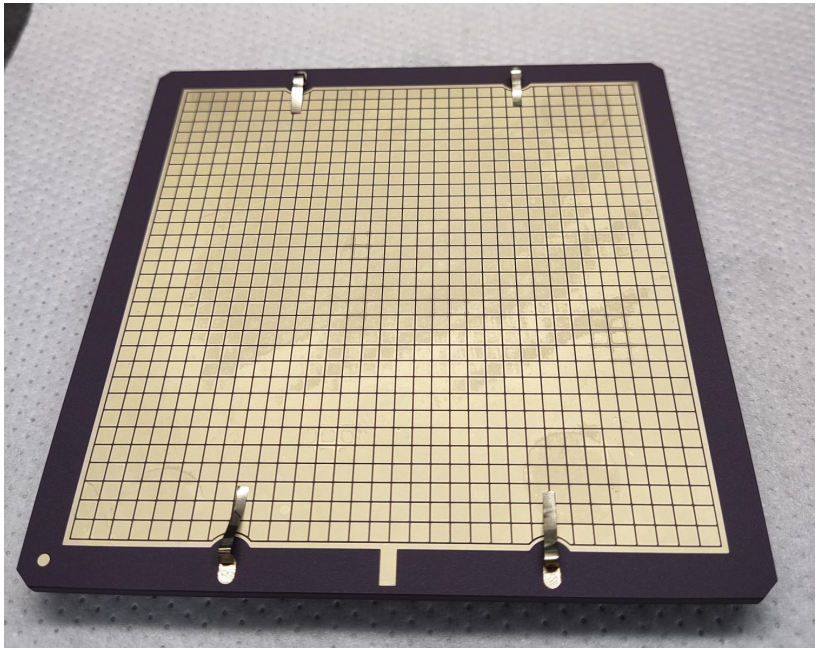
HRPPD #15 (EIC HRPPD #1)

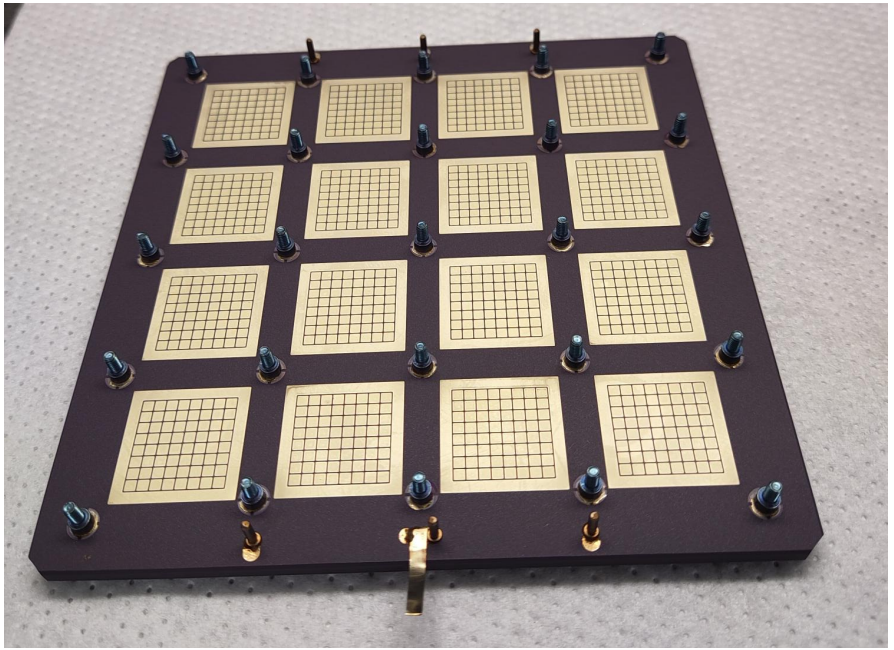




DCR few kHz/cm^2; SPE timing ~60ps

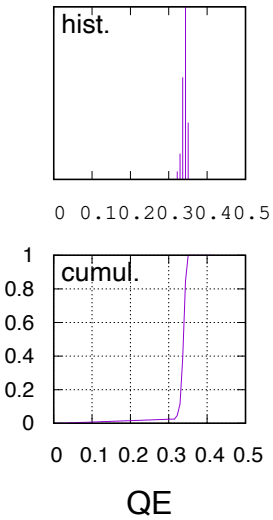
HRPPD #16 (EIC HRPPD #2)

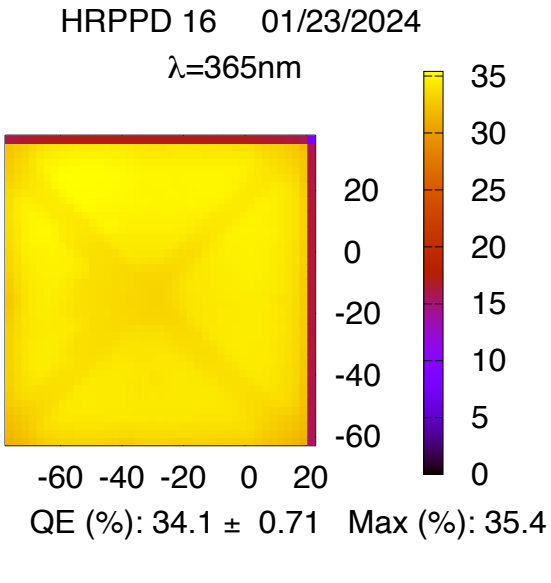


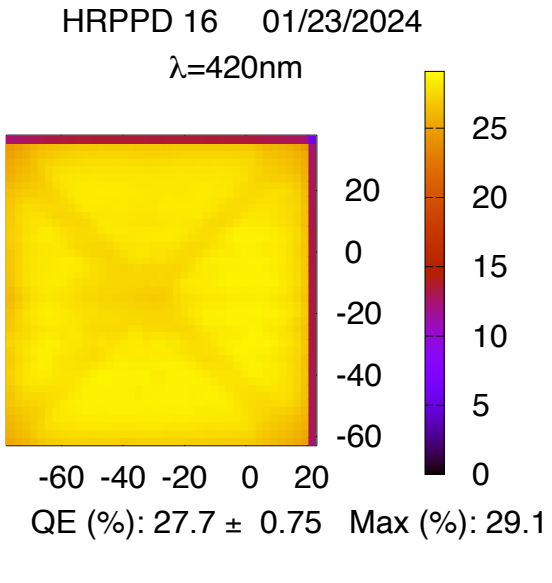


- A number of production bugs fixed, as compared to #15
- If everything goes well, will be ready for shipment next week

HRPPD #16 (EIC HRPPD #2)



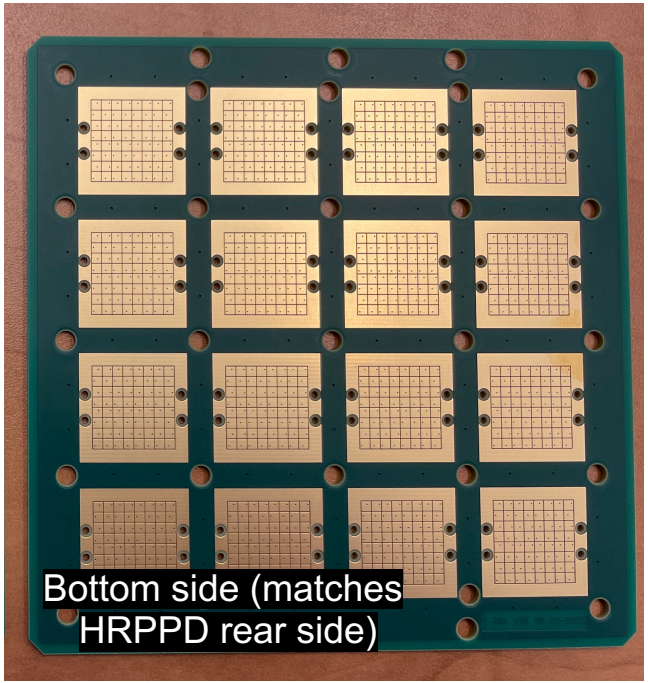


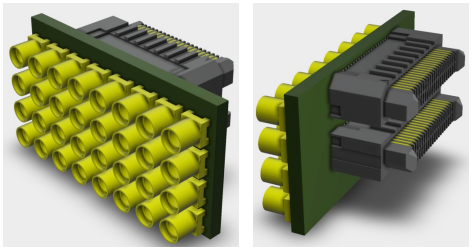


The QE scan looks even better than for #15: ~34% @ 365nm

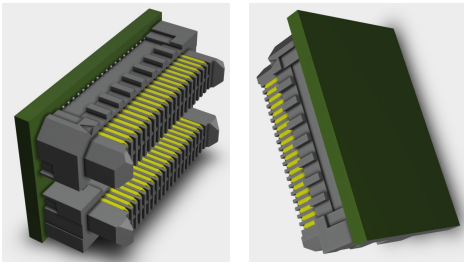
- If everything goes well, will be ready for shipment by the end of January

HRPPD passive interface #1(an update)





1x MMCX adapter



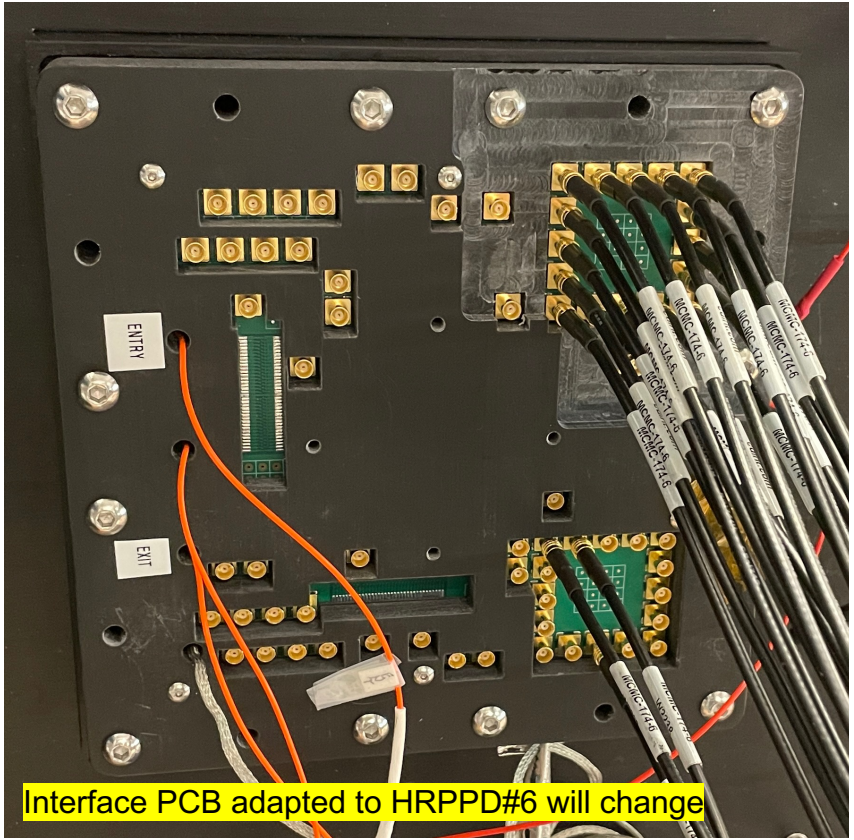
15x grounding caps

- All bare boards produced weeks ago; delays with assembly on a PCB shop side
- Assembled small boards are expected by January 31st
  - Including a Photek MCP-PMT interface board

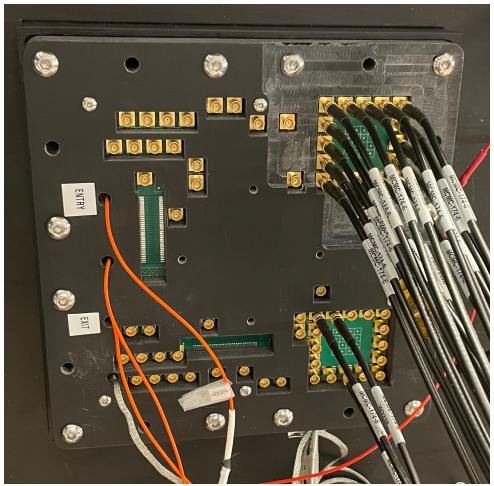
For Incom, JLab & Co

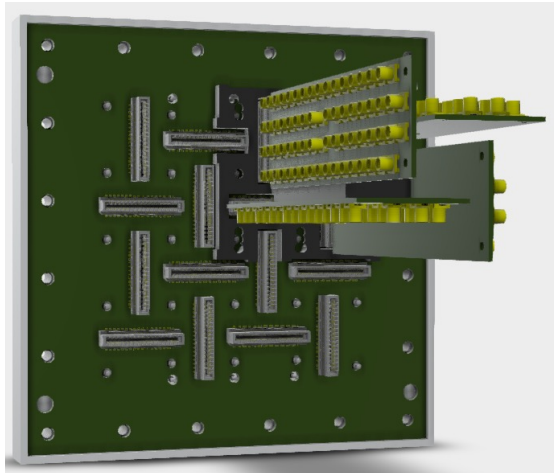
HRPPD QA station @ BNL (an update)

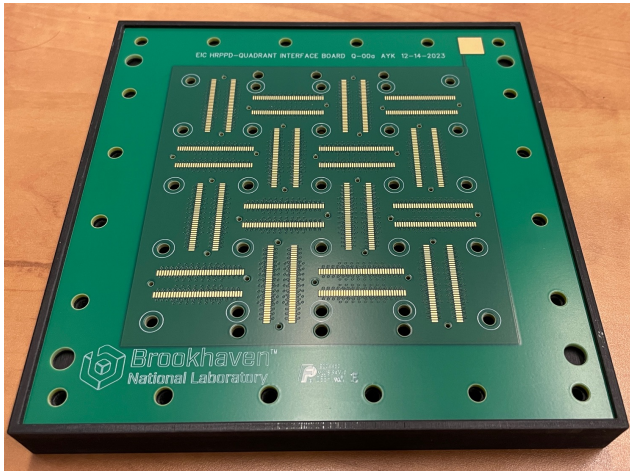
- Optimize data taking procedure
  - Synchronize DRS4 configuration with the XY-stage positioning (we are interested only in the illuminated pad data for these scans)
  - Read out only one of the 8x4 DRS4 chips and only the first 136 out of 1024 samples at 5GS/s (event size reduction from ~50kB to <2kB)
  - Then both the data volume and the CPU needs are manageable (at most 10^5 events per pixel @ ~9kHz, percentage of SPE events yet TBD)
- Plan to perform per pixel surface scans:
  - PDE (*in a counting mode*) & gain uniformity, timing
  - DCR (a self-triggering mode or a random trigger)
  - QE via a direct photocathode current measurement
    - Two pairs of Hamamatsu photodiodes ordered



HRPPD passive interface #2 (an update)







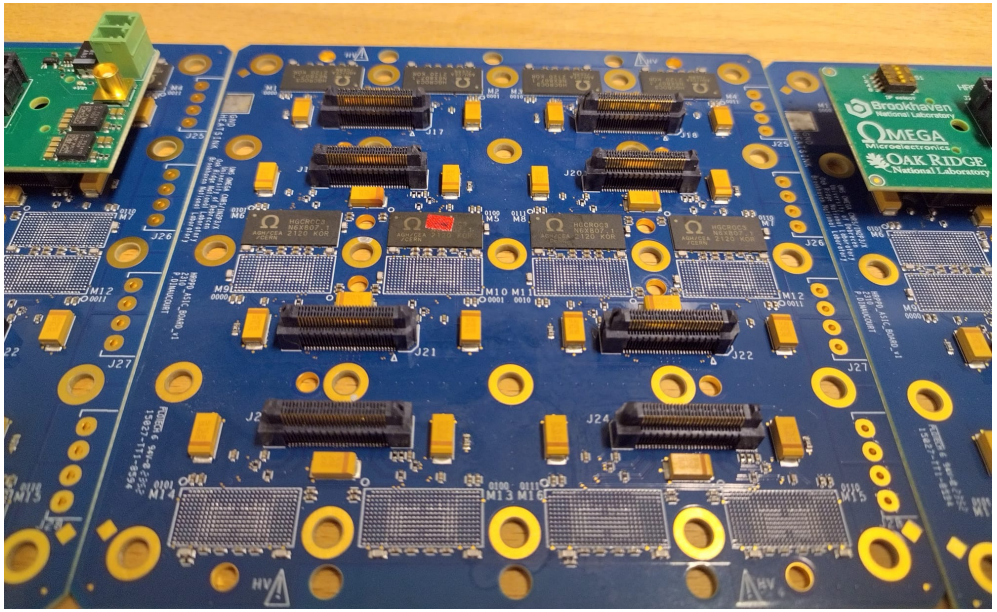
- Recycle existing 64-channel MCX adapters, 3D printed clam shell enclosure, etc
- Equip one HRPPD quadrant at a time for a scan and shorten to ground all other connectors

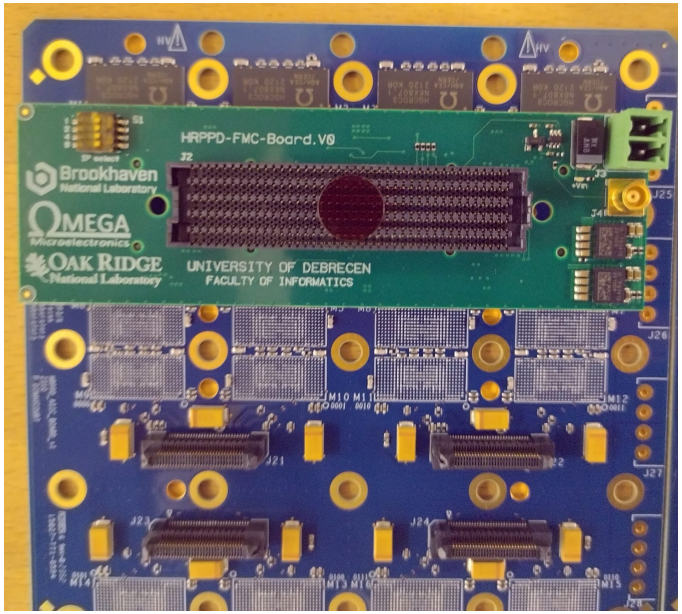
- Bare boards produced, as well as a 3D printed enclosure pieces
- Assembled board will hopefully become available also by January 31st

For BNL

HGCROC3 ASIC / FPGA backplane

IN2P3 [OMEGA] (Pierrick, Damien), Uni Debrecen (Gabor, Miklos)
BNL (Daniel), Oak Ridge (Norbert)





- Four partly assembled ASIC boards are produced and shipped to Debrecen and BNL
- ASIC board + FMC (passive) board + KCU105 FPGA kit debugging @ Debrecen will take ~two weeks
- FPGA bare board production is delayed substantially; expected by March 1st

AOB

- LAPPD Workshop #4 in April 2024
  - Please provide your blackout days
- FY24 progress reports are requested by February 15th
  - Should be given against the milestones
  - Contracts in place?
- At some point we need to re-focus on Photek & Photonis MCP-PMTs
  - Passive interface for Photek will be ready by January 31st
  - MCP-PMT itself is supposed to be received in January, correct?
  - Passive interface for Planacon is a low priority topic, yet needs to be made at some point
  - What else is missing?