dRICH DAQ
Short summary for SRO meeting

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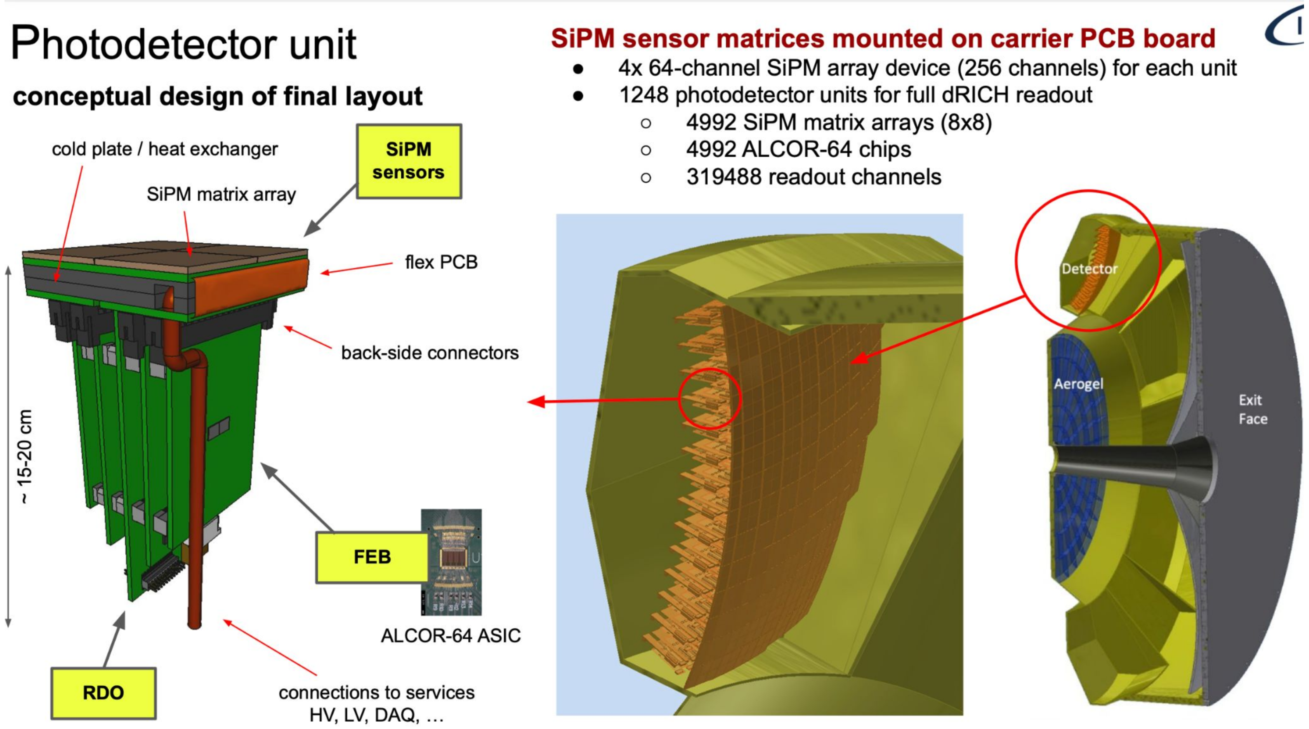
Reference: DAQ update at dRICH meeting was last 15 Nov

Outline

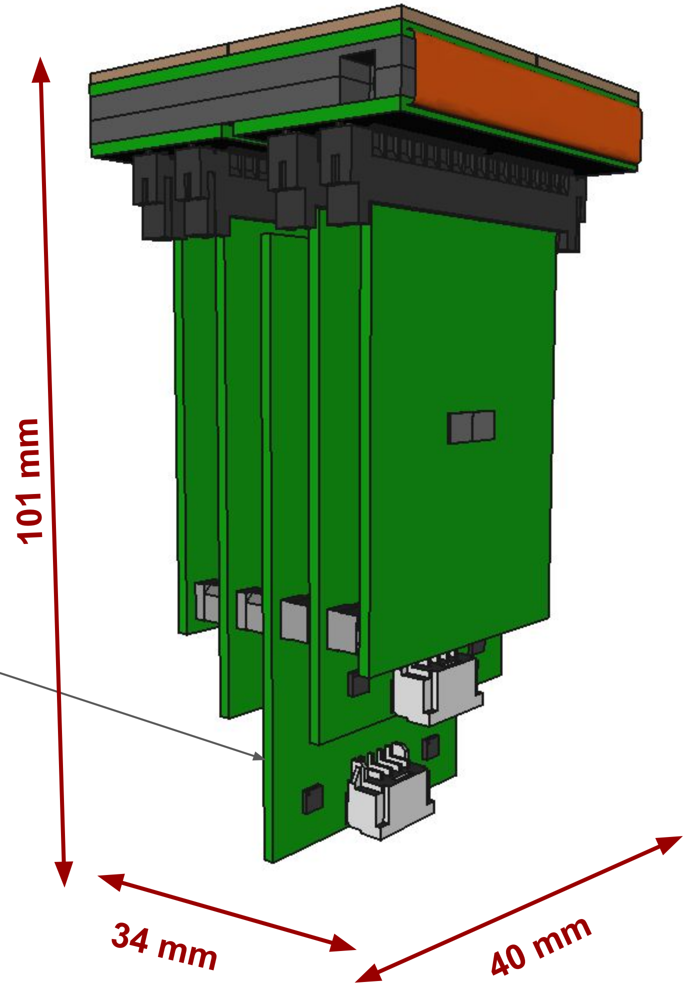
- Brief dRICH RDO overview in dRICH PDU
- Baseline RDO design
- DAQ throughput modelling

Trying to give some additional input/info following discussions @ANL



dRICH RDO Overview

RDO is as a *component* of dRICH PDU

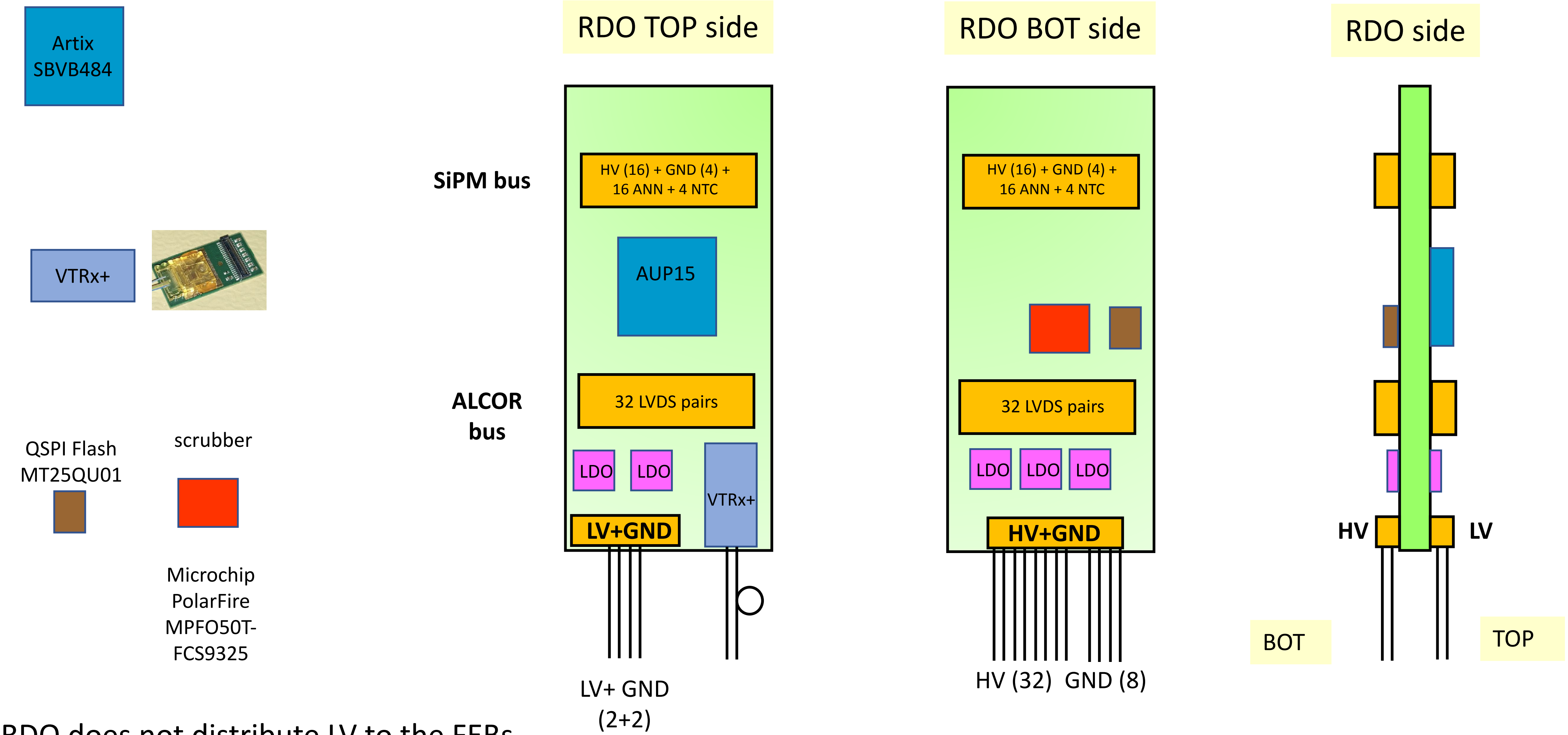


basic RDO specs/numbers:

- provide interface to ePIC DAQ
- provide readout/config to 4 ALCOR64
- route HV to SiPM via FEB
- 1 optical link (TX/RX)
- “control” annealing (MOSFET setup)
- services (T sensors, current monitor, …)
- 4x9 cm^2 surface available

Need of high integration with challenging space constraints→ “custom” RDO

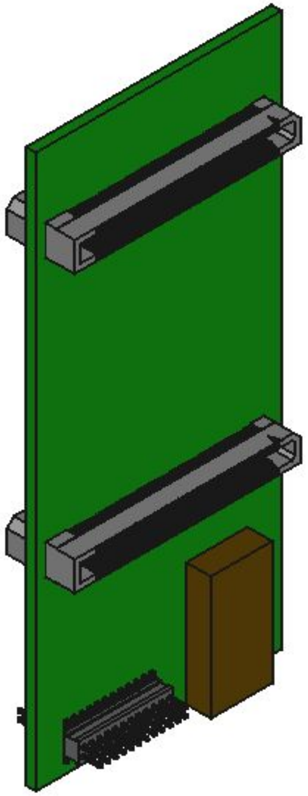
RDO Baseline (I)



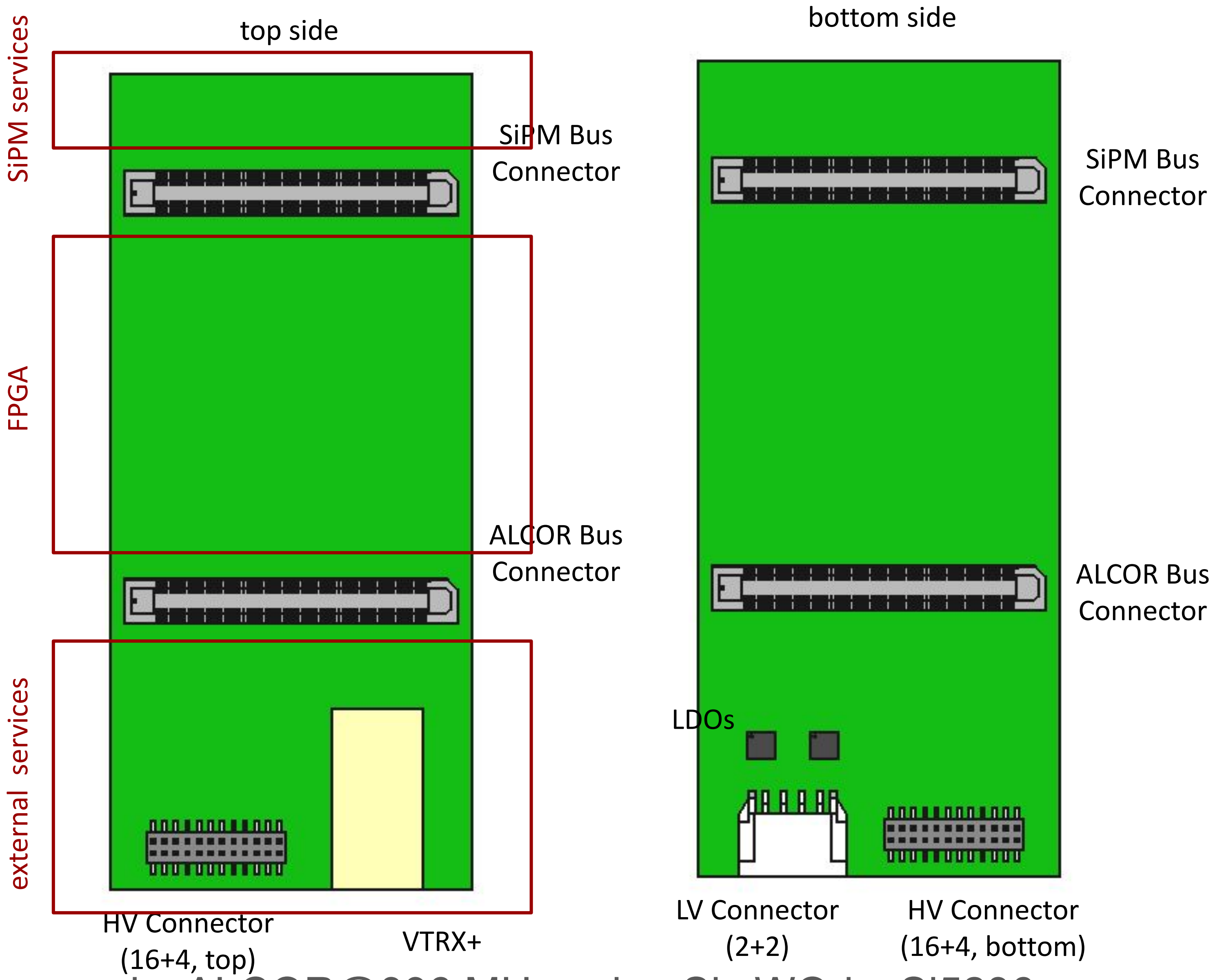
RDO does not distribute LV to the FEBs

components on scale excluding connectors

RDO baseline (II)

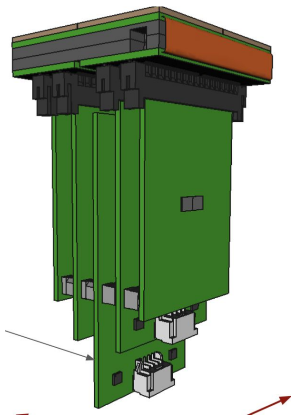


- 14-16 layers min
- HV in shielded middle-layer"!
- engineers at work on schematics



preferred clock to be received: 98.5 MHz, we aim ALCOR@396 MHz using SkyWOrks Si5236

RDO and ePIC DAQ



1248

1248

- PDU: 1248
- RDO: 1248
- FEB: 4992

I-level DAM (27)

FELIX

- 47 links to PDU
- 1 link to II-level DAM

27

in exp. hall, rack mounted

or PC with 4 FELIX each (??)

27

II-level DAM (1)

FELIX

- 27 links to I-level DAM
- link from central ePIC [clock/trigger]

ePIC interaction tagger
able to reach our DAMS in 10 μs!

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dRICH has largest number of RDOs in ePIC

EPIC Detector Scale and Technology Summary:

Detector System	Channels	RDO	Gb/s (RDO)	Gb/s (Tape)	DAM Boards	Readout Technology	Notes
Si Tracking: 3 vertex layers, 2 sagitta layers, 5 backward disks, 5 forward disks	7 m^2 36B pixels 5,200 MAPS sensors	400	26	26	17	MAPS: Several flavors: curved its-3 sensors for vertex Its-2 staves / w improvements	Fiber count limited by Artix Transceivers
MPGD tracking: Electron Endcap Hadron Endcap Inner Barrel Outer Barrel	16k 16k 30k 140k	8 8 30 72	1	.2	5	uRWELL / SALSA uRWELL / SALSA MicroMegas / SALSA uRWELL / SALSA	64 Channels/Salsa, up to 8 Salsa / FEB&RDO 256 ch/FEB for MM 512 ch/FEB for uRWELL
Forward Calorimeters: LFHCAL HCAL insert* ECAL W/SciFi Barrel Calorimeters: HCAL ECAL SciFi/PB ECAL ASTROPIX Backward Calorimeters: NHCAL ECAL (PWO)	63,280 8k 16,000 7680 5,760 500M pixels 3,256 2852	74 9 64 9 32 230 18 12	502	28	19	SiPM / HG2CROC SiPM / HG2CROC SiPM / Discrete SiPM / HG2CROC SiPM / HG2CROC Astropix SiPM / HG2CROC SiPM / Discrete	Assume HGCROC 56 ch * 16 ASIC/RDO = 896 ch/RDO 32 ch/FEB, 16 FEB/RDO estimate, 8 FEB/RDO conserve. HCAL 1536x5 *HCAL insert not in baseline Assume similar structure to its-2 but with sensors with 250k pixels for RDO calculation. 24 ch/feb, 8 RDO estimate, 23 RDO conservative
Far Forward: B0: 3 MAPS layers 1 or 2 AC-LGAD layer 2 Roman Pots 2 Off Momentum ZDC: Crystal Calorimeter 32 Silicon pad layer 4 silicon pixel layers 2 boxes scintillator	300M pixel 1M 1M (4 x 135k layers x 2 dets) 640k (4 x 80k layers x 2 dets) 400 11,520 160k 72	10 30 64 42 10 10 10 2	15	8	8	MAPS AC-LGAG / EICROC AC-LGAD / EICROC AC-LGAD / EICROC APD HGCROC as per ALICE FoCal-E	3x20cmx20cm 600^cm layers (1 or 2 layers) 13 x 26cm layers 9.6 x 22.4cm layers There are alternatives for AC-LGAD using MAPS and low channel count DC-LGAD timing layers
Far Backward: Low Q Tagger 1 Low Q Tagger 2 Low Q Tagger 1+2 Cal 2 x Lumi PS Calorimeter Lumi PS tracker	1.3M pixels 480k pixels 700 1425/75 80M pixels	12 12 1 1 24	150	1	4	[illegible] Timepix4 (SiPM/HG2CROC) / (PMT/FLASH) Timepix4	
PID-TOF: Barrel Endcap	2.2M 5.6 M	288 212	31	1	17	AC-LGAD / EICROC (strip) AC-LGAD / EICROC (pixel)	bTOF 128 ch/ASIC, 64 ASIC/RDO eTOF 1024 pixel/ASIC, 24-48 ASIC/RDO (41 ave)
PID-Cherenkov: dRICH	317,952	1242	1240	13.5	28	SiPM / ALCOR	Worse case after radiation. Includes 30% timing window. Requires further data volume reduction software trigger
pfRICH DIRC	69,632 69,632	17 24	24 11	12.5 6	1 1	HRPPD / EICROC (strip or pixel) HRPPD / EICROC (strip or pixel)	

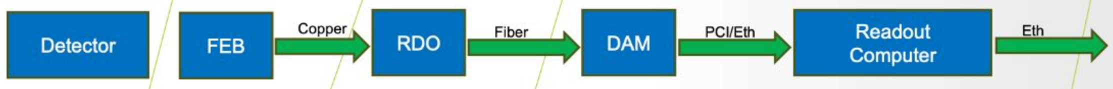
numerology in Sep2023 now 1248

Status@ANL meeting.. (Jeff)

Summary of Channel Counts and Data Flow

Detector Group	Channels					RDO	Fiber (single)	DAM	Data Volume (RDO) (Gb/s)	Data Volume (To Tape) (Gb/s)
	MAPS	AC-LGAD	SiPM/PMT	MPGD	HRPPD/ MCP-PMT					
Tracking (MAPS)	16B					n/a	3158	35	26	26
Tracking (MPGD)				202k		118	236	5	1	1
Calorimeters	500M		104k			451	902	14	502	28
Far Forward		1.4M	253k			247	624	10	15	8
Far Backward	66M	60k	2k			38	518	14	150	1
PID (TOF)		7.8M				500	1500	14	31	1
PID Cherenkov			320k		140k	1283	2583	32	1275	32
TOTAL	16.9B	10.4M	679k	202k	140k	2637	9521	124	2,000	96

Summary of Data Flow



100% Occupancy	27.5-1760 Pb/sec

Aggregate	**2.0 Tb/sec**
Noise	1.6 Tb /sec
Signal from Physics + Background	400 Gb / sec

Aggregate	**2.0 Tb/sec**
Per RDO (Avg)	0.7 Gb/sec

Aggregate	**96 Gb/sec**
Collision Signal	38 Gb/sec
Synchrotron Rad	.01 Gb/sec
Electron Beam	22 Gb/sec
Hadron Beam	4 Gb/sec
Noise	32 Gb/sec

1/10/2023 Electronics, DAQ & SRO Workfest

New numbers coming out with improvements:

- Correct Thresholds
- Simulation Properties
- Updated Collider Lattice
- Distributions of hits within detectors
- More realistic ASIC behavior
- Better understanding of software triggering scheme

See Elke's talk and ePIC background group wiki

For now, these are last summer's numbers

dRICH doesn't have largest number of DAMs..

Data throughput modeling (update)

dRICH DAQ parameters	
RDO boards	1248
ALCOR64 x RDO	4
dRICH channels (total)	319488
Number of DAM L1	27
Input link in DAM L1	47
Output links in DAM L1	1
Number of DAM L2	1
Input link to DAM L2	27
Link bandwidth [Gb/s] (assumes VTRX+)	10
Interaction tagger reduction factor	200
Interaction tagger latency [s]	2,00E-06
EIC parameters	
EIC Clock [MHz]	98,522
Orbit efficiency (takes into account gap)	0,92

ALCOR parameters		Notes
Front end limit [kHz]	4000	
ALCOR Clock [MHz]	394,08	It will be 394.08 MHz or 295.55 MHz
Channels/serializer	8	
Bits per hit	64	2 32-bit words per hit (also TOT)
Bits per hit encoding 8/10	80	
Serializer band limit [Mb/s]	788,16	
Theoretical Serializer limit/ channel [kHz]	1231,5	this would be with 0 control words
Serializer limit single ch [kHz]	800	this is expected to improve with ALCOR v3
Number of serializer per chip	8	
Channel/chip	64	
Shutter width (ns)	2	

	Bandwidth analysis		Limit	Comments
INPUT	Sensor rate per channel [kHz]	300,00	4.000,00	
	Rate post-shutter [kHz]	55,20	800,00	
	Throughput to serializer [Mb/s]	34,50	788,16	
	Throughput from ALCOR64 [Mb/s]	276,00		limit FPGA dependent: with RDO prototype we will have something
	Throughput from RDO [Gb/s]	1,08	10,00	based on VTRX+
	Input at each DAM I [Gbps]	50,67	470,00	
	Buffering capacity at DAM I [MB]	0,01		to be checked but seems manageable
	Throughput from DAM I to DAM II [Gbps]	0,25	10,00	this might be higher (from FELIX to FELIX)
	Output to each DAM II [Gbps]	6,84	270,00	

- numbers passed to ePIC
- interaction tagger critical (**several discussion at ANL**)
- some of the "pressure" transferred to budget

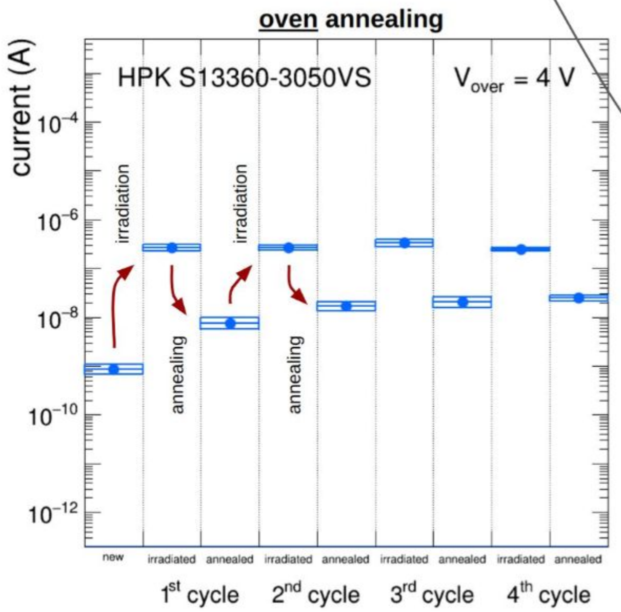
Note this is with 200 interaction tagger reduction factor

Aggregated dRICH data		Comments
Total input at DAM I [Gb/s]	1.368,14	This is only "inside" DAM, not to be transferred on PCI
Total input at DAM II [Gb/s]	6,84	This is based on aggregation above + reduction factor of the interaction tagger
Total output from DAM II [Gb/s]	6,84	Further reduction possible to be investigated (FPGA level?)

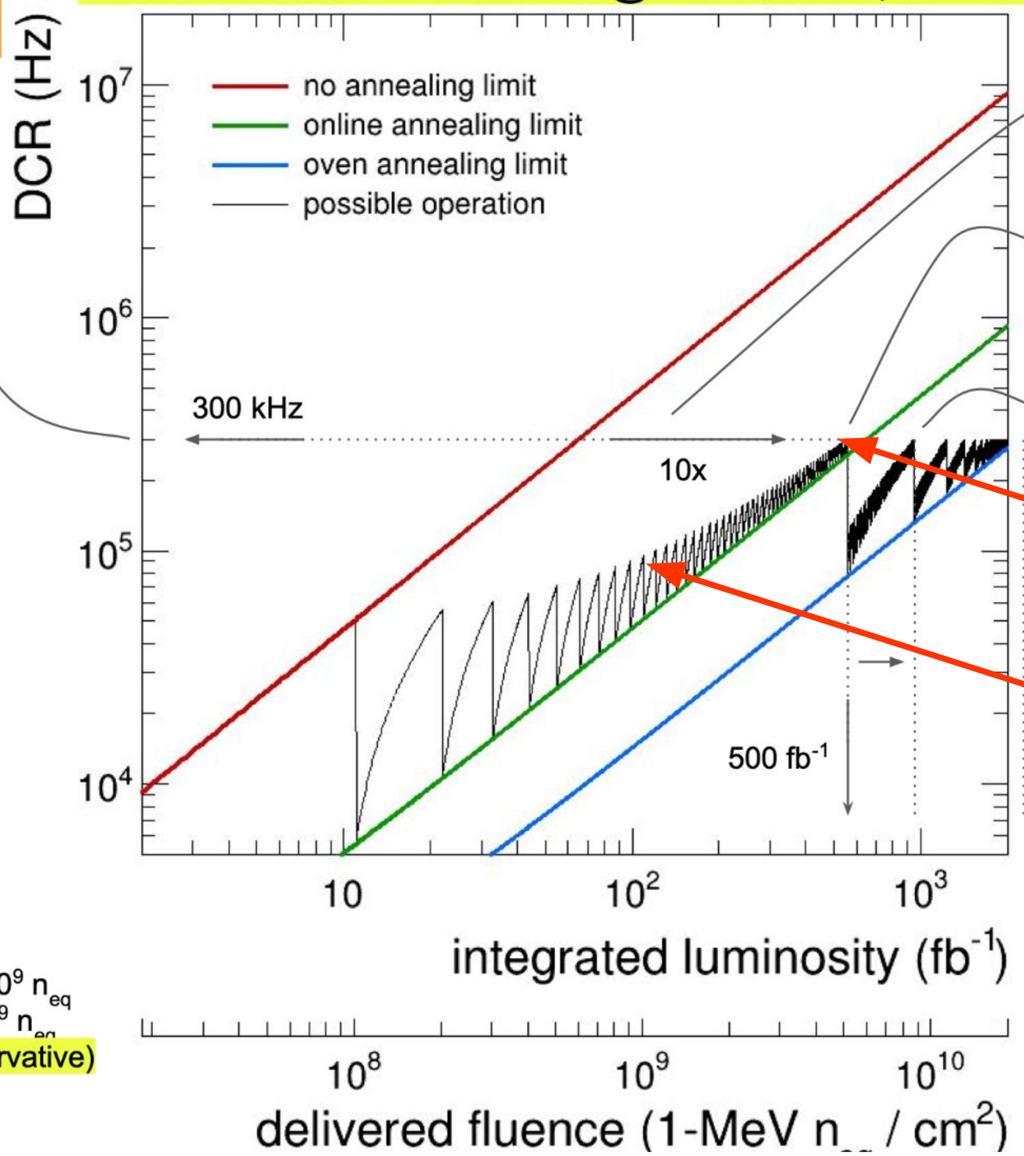
Ageing model and some DAQ consequences…

R. Preghenella at HEP-EPS 2023

max acceptable DCR for
Physics performance
~ 10 noise hits / sector within 500 ps



Hamamatsu S131360-3050 @ Vover = 4 V, T = -30 C



online annealing
extends SiPM
lifetime by ~ 10x

more aggressive
annealing needed here
might need to unmount SiPM (oven)

up to 1000 fb^{-1} with only
one oven annealing cycle
optimisation of online annealing
protocol could reach beyond that

model input from R&D measurements

- DCR increase: 500 kHz/10^9 n_{eq}
- residual DCR (online annealing): 50 kHz/10^9 n_{eq}
- residual DCR (oven annealing): 15 kHz/10^9 n_{eq}

1-MeV neq fluence from background group (conservative)

- 9 10^6 n_{eq} / fb^{-1}
- includes 10x safety factor

these predictions are according to
present knowledge / tested solutions
there are more handles to
further mitigate DCR
lower Vover, 3V
lover T operation -40 C or below

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dRICH throughput during EIC life…

When	DCR	Total throughput at DAM-I	Total throughput at DAM-II
starting	2	9.2 Gbps	< 1 Gbps
after 100 fb^{-1} (and several annealing cycles)	100	456 Gbps	2.28 Gbps
“at limit”	300	1.3 Tbps	6.84 Gbps

this is with factor 200 but…

https://docs.google.com/spreadsheets/d/1P3qoogFWuicXDgojwvhaFL2EnwQ7BEmGlITg1fwDUkE/edit#gid=0

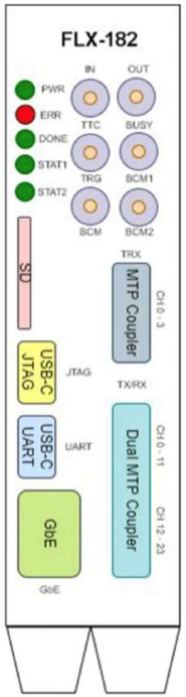
Questions:

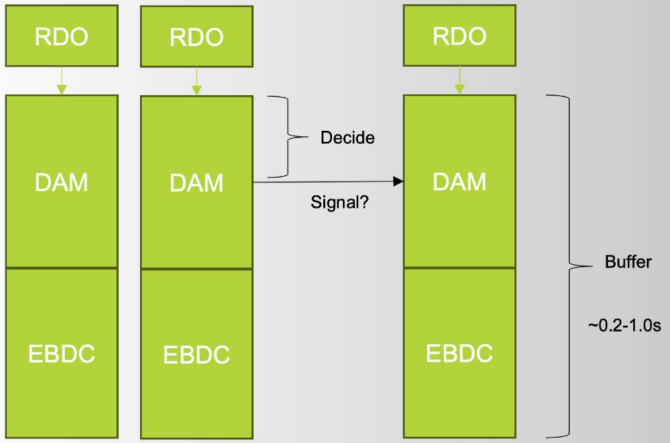
a) when the ePIC DAQ really starts having a problem? (max. throughput FELIX2-PCIe?) [it is also useful info for data reduction target inside DAM-II at FPGA]
b) any scenario about machine luminosity (and radiation) in 2031-2034?

Note on latency of interaction tagger

Triggering To Do

- Technical Issues
  - How is the communication handled?
- Trigger Issues
  - What are the algorithms, and what detectors go into the algorithms?
  - dRICH
    - ➢Does not need to be collision trigger. Trigger only needs to ensure that there is a real hit in the detector
  - Low Q Tracker
    - ➢Collision Trigger expected
    - ➢Could use prescale instead
- Collision detector detector?
  - Do we need one?
  - Can we construct one?
  - What would it look like?





Decision Signal not yet specified

- 100Gb Ethernet (switched)?
- Dedicated “Trigger” FELIX Boards?
- Hardware/Software Signals routed through GTU?

the model so far uses 2 µsec latency

Eth implementation on FLX-192 to distribute “interaction tagger”?

Note: 2 ms latency instead would require 12.8 MB buffering capacity (with 300 KHz DCR rate) in FLX-182

The dRICH big plan (just DAQ)

2024	2025	2026
• **hardware effort** • RDO prototype as close as possible to final • RDO readout of old FEB32 • initial ePIC link test with RDO (clock) • input to TDR • radiation tests	• integration with ALCOR64 in the PDU • **readout with VC709 & ePIC link (including clock)** • RDO rev. 2 final components • possibly test in detector box • (likely radiation tests again….)	• FELIX available in ePIC to groups • use of DAM (FELIX2) • **crucial firmware development L1-DAM / L2-DAM**

2027	2028	2029
production	assembly	assembly in-situ DAM deployment + commissioning

in parallel:

- someone has to think/build ePIC interaction tagger
- further data reduction/calibration through L2-DAM FPGA or SRO to be integrated

Conclusions

- ongoing effort toward specifications/requirements for RDO (at 60/70%)
- secured VTRx+ and almost defined FPGA baseline
- need of highly integrated development of RDO with other dRICH electronic components

- ePIC link protocol still not defined, we need to remain close to central ePIC DAQ
- at the forefront → designing first ePIC RDO (risk of later specs/surprises)
- ePIC interaction tagger is crucial to dRICH architecture → need to work with ePIC/EIC project