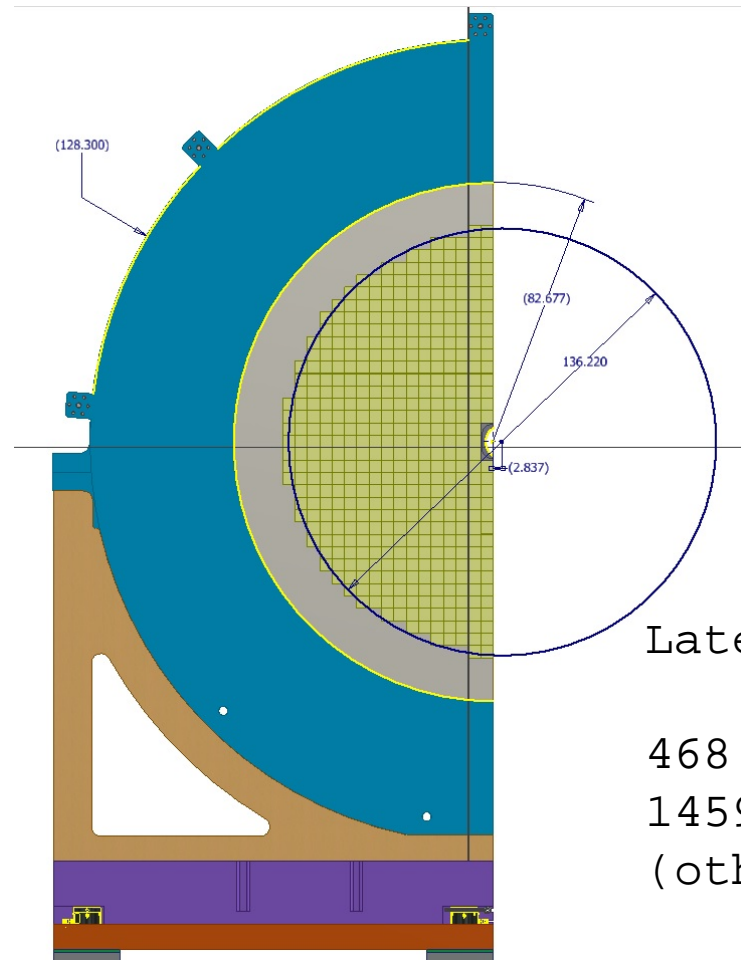


eRD109 COTS Waveform Readout FEB – update Feb. 1 2024

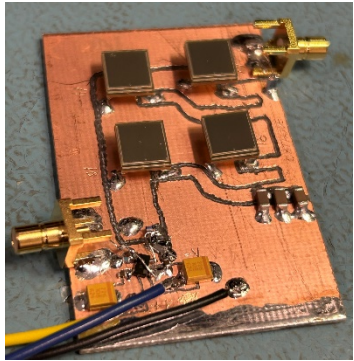
G. Visser, Indiana University



Latest update on fwd ECAL:

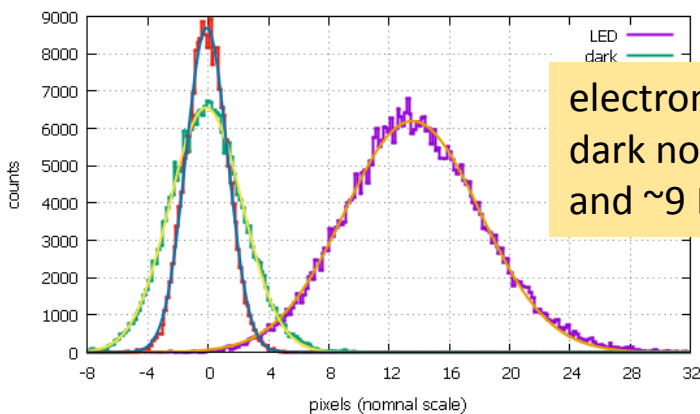
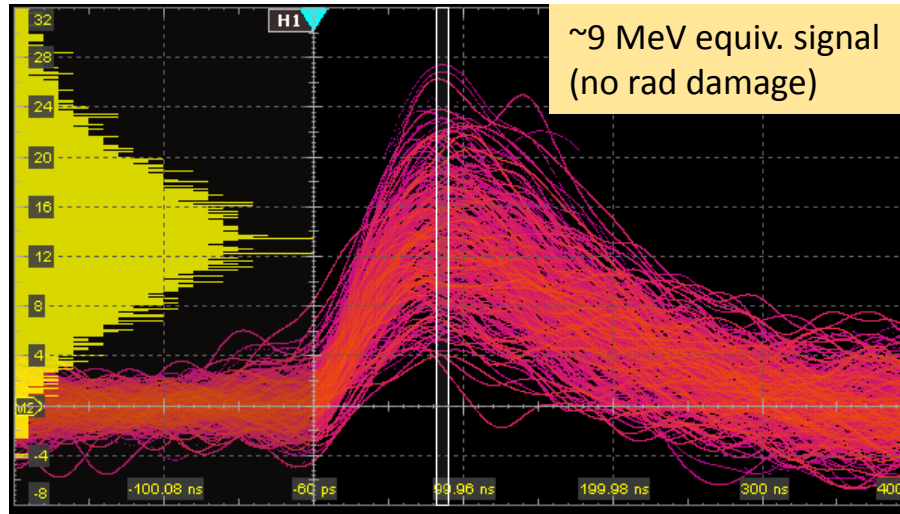
468 FEB (14976 channels)
14592 channels really used
(others masked)

SiPM frontend



New inductor load circuit improves SiPM recovery time.

Preamp/shaper follows FCS design.



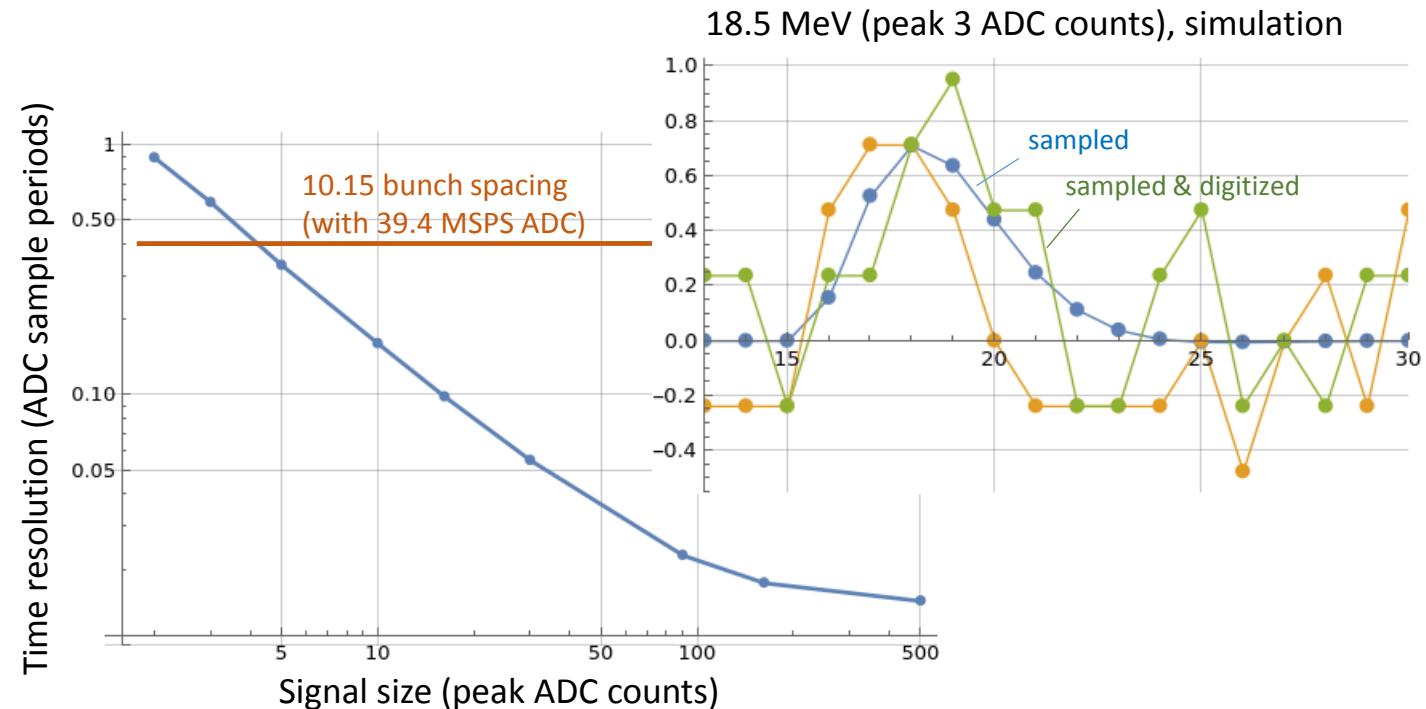
Digitizer

Baseline plan *has to be 14 bits*, with 100 GeV signal peak at $\sim 16,200$ counts. *12 bits is pointless.*

Optimum peaking time ~ 80 ns (integration-by-summing vs. DCR pile-up)

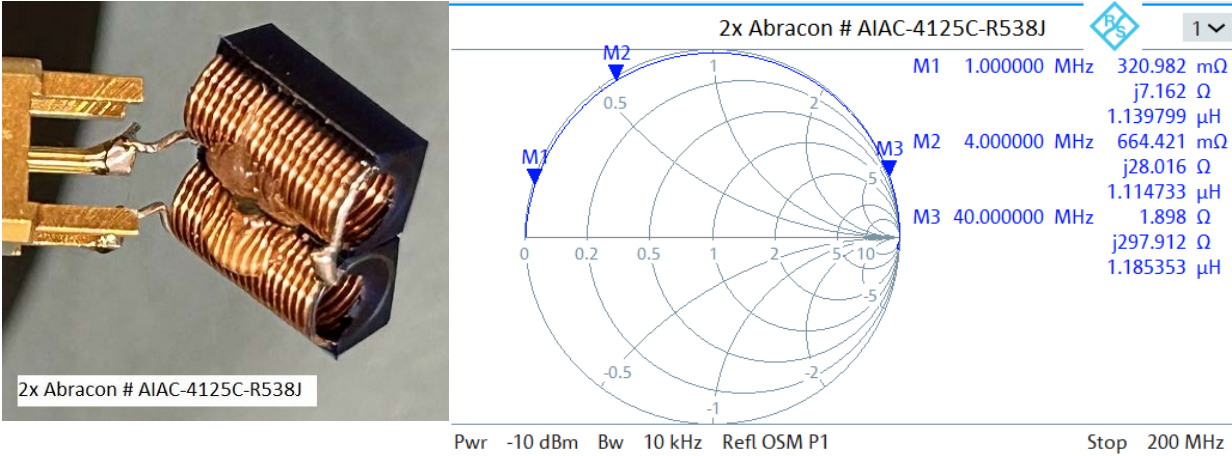
Explored 'dynamic range extension' by dual-gain circuit but it is not promising – too much worry about calibration...

Small signals ~ 15 MeV required, will be very difficult to handle. (Biggest problem with the small signals though is DCR, not digitizer resolution. Improved light yield would help.)

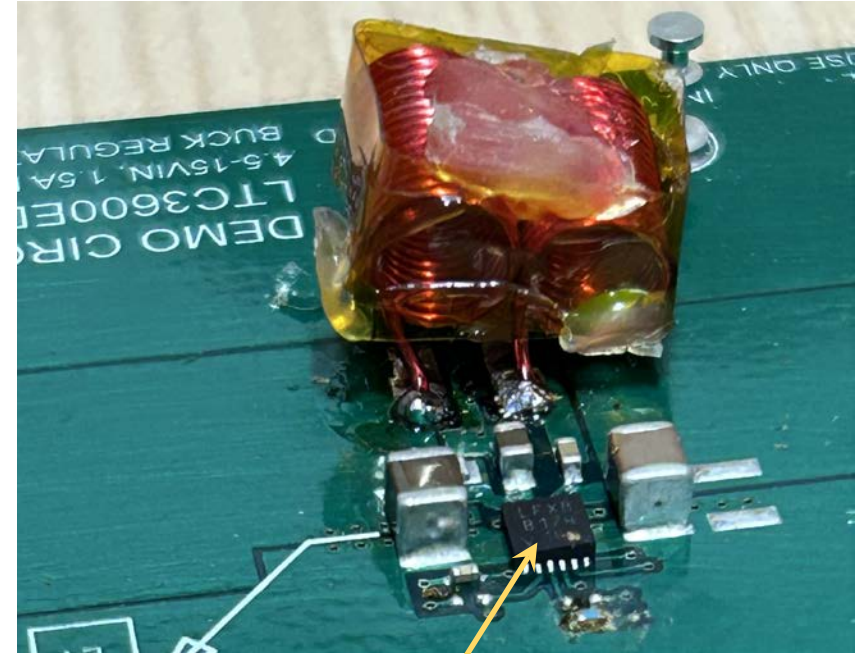


All to be presented in 2/7/24 calorimeter meeting with complete details

Power

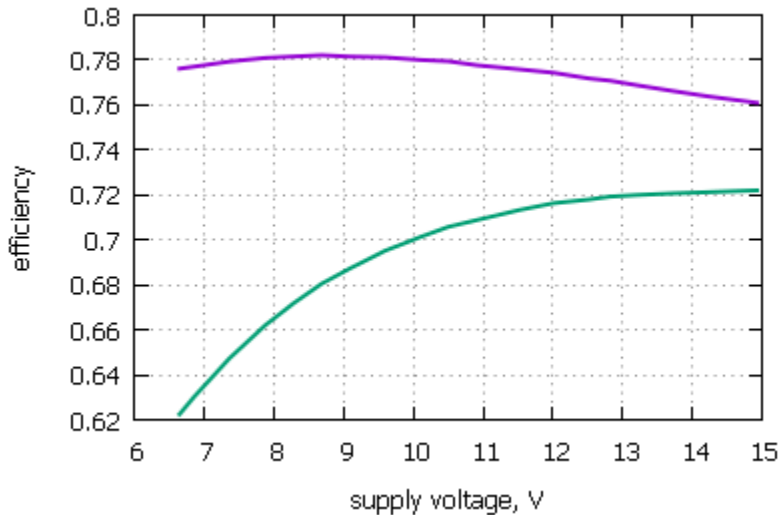


- Antiparallel pair of solenoids should have modest far field
- Confirmed that ground plane / shield has little performance impact
- Shield will be incorporated in new prototype
- Measured performance with stock inductors is quite sufficient



LTC3600

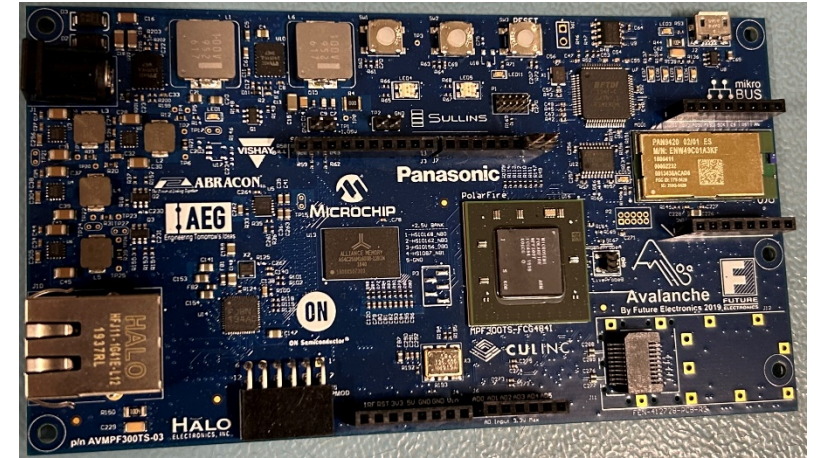
alternative: bPOL48V (too large...)



Efficiency (w/ 1 A 1.8V load)
 board only
 with 50' 20AWG shared to 6 boards

Radiation testing will be needed
 Test fixture could be ready on short notice...
 Opportunities? → Let's discuss

- Specifications/requirements documented
 - Seems like close to finalizing rate requirements!
- FEB-detector integration is well developed
- Key parts procured: ADC, FPGA, DC/DC, preamp
 - Including more FPGA dedicated to bwd ECAL application
- Learning PolarFire FPGA details
- SiPM carrier board & interconnections sketched out
- Lightguide improvements (→ Required for FEB mechanical, and possible light yield improvements are of the greatest importance for readout – min signal size challenge!)
- Cooling prototyped with dummy load
- LTC3600 DC/DC circuits with air-core inductor
- SiPM frontend prototyped / improved from STAR FCS
- Working to define FEB-RDO interface
 - Expect to make simple FMC board to interface to ppRDO (Tonko)
- **Next steps / in-progress**
 - **Two channel signal path prototype to fit to PolarFire eval board**
 - SiPM board layout & produce prototypes
 - FEB Main Board layout & produce prototypes
 - Considerations for application to bwd ECAL
- **Other to-do:**
 - **Radiation testing**
 - Improvements to STAR FCS bias circuits (cost reduction etc.)
 - Continue 'dynamic range extension' ideas as a plan B



PolarFire Eval Board – nice/simple/\$200

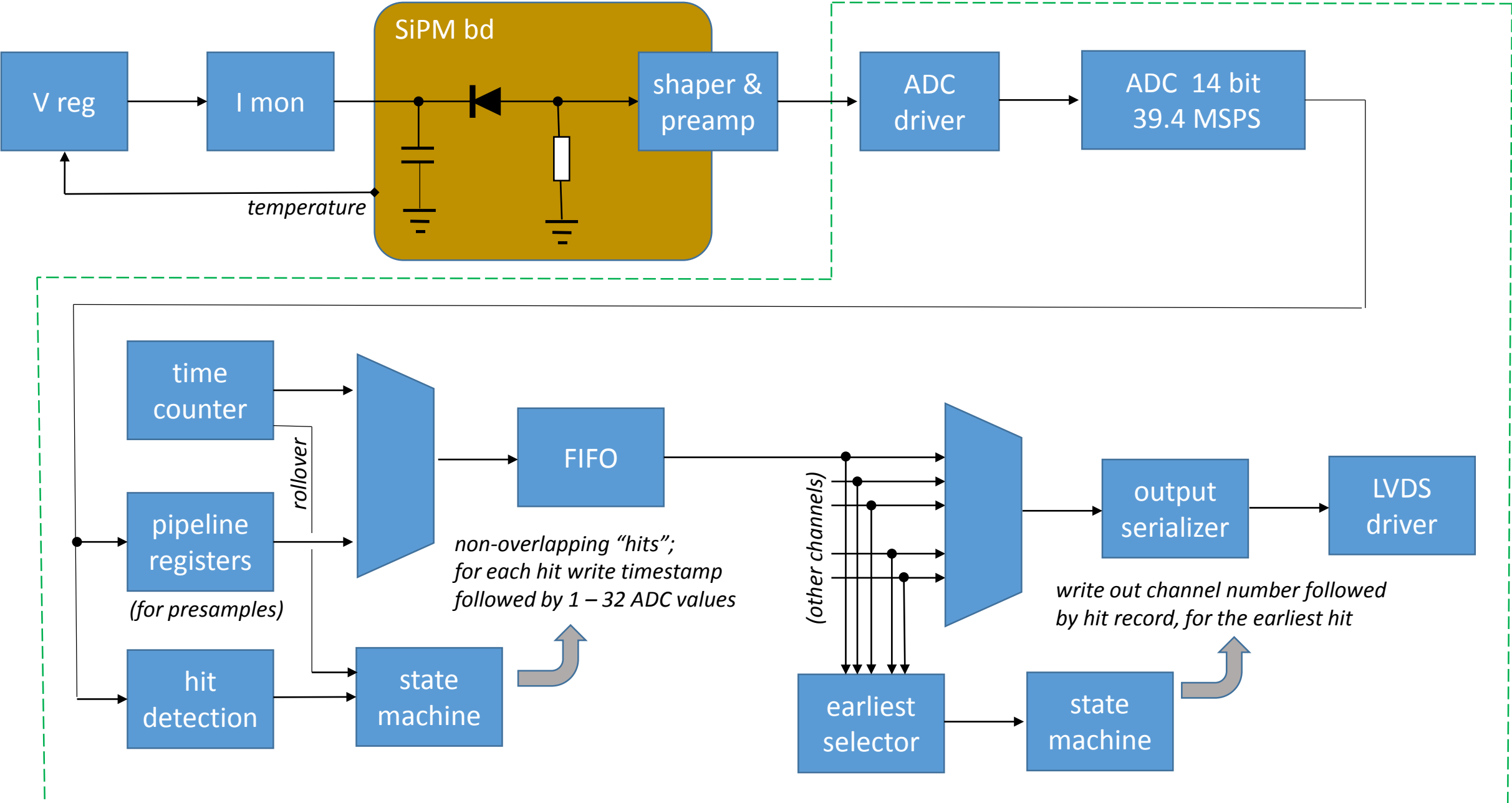
I've deviated somewhat from the sequence of milestones in contract. Trying to do always what is best to push forward the design.

So far have not really tackled comparisons to HGCROC nor waveform ASIC possibilities. These will be done, but I think the first emphasis has to be on design.

On the other hand, have put early effort into possible application to bwd ECAL.

backup slides

Block diagram



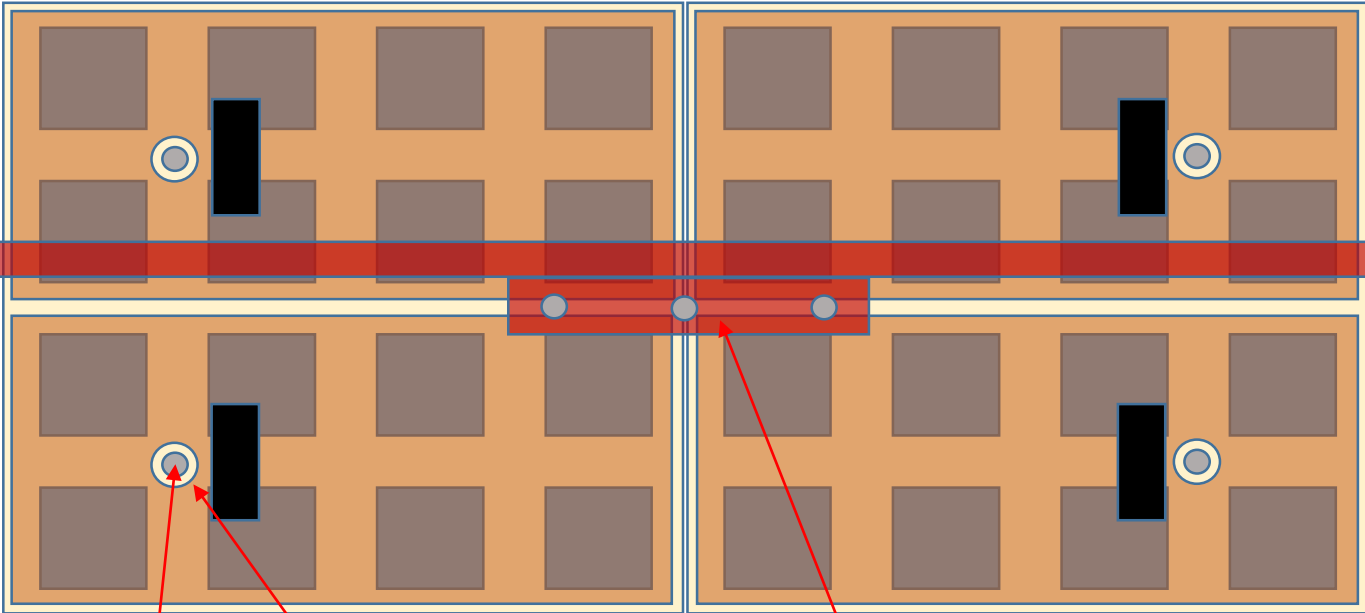
FEB & SiPM carrier mechanical cartoons
(dimensioned sketches will be made later)

2-block (32 tower) FEB

(forced) air cooling option now ruled out, too difficult to integrate

This was sketched with old lightguide (one pyramid per tower). This is out of date (see Oleg's presentation). No impact on FEB, so for simplicity (or laziness) I'm not updating it here.

FEB not shown (in this view only)
(but see next page)



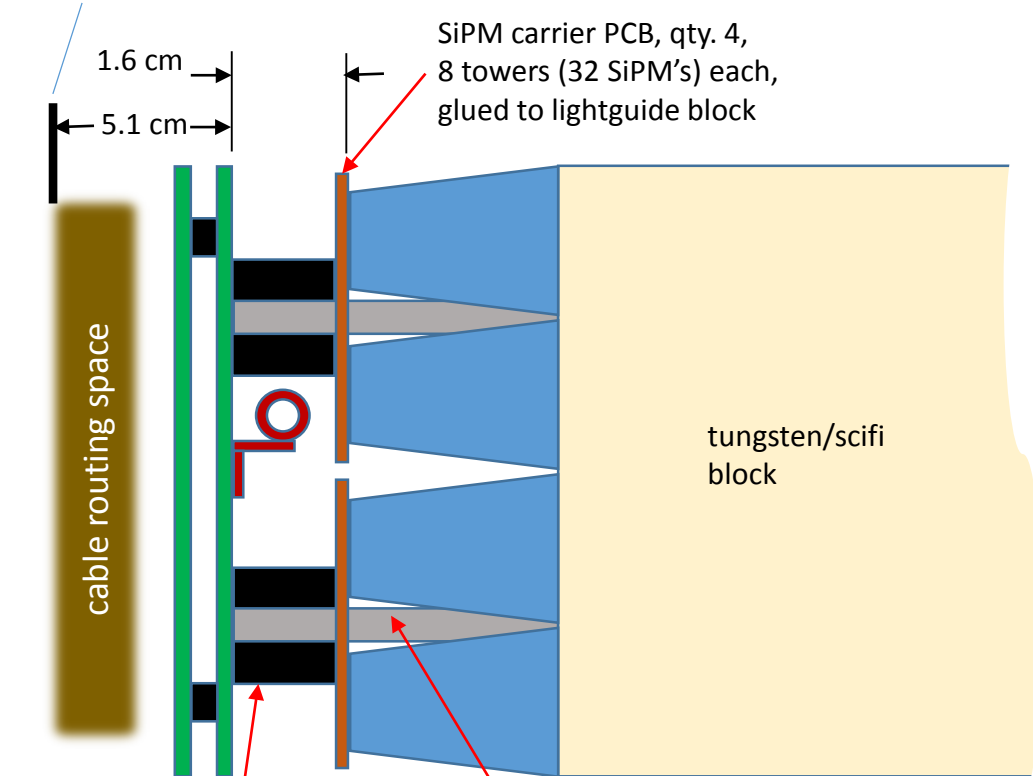
standoff clearance hole through SiPM carrier PCB

6 or 7 4-40 pan head screws to attach FEB on 4 standoffs and 2 or 3 thermal tab nuts

water tubing connection to FEB is also an electrical ground for FEB (important for noise/EMI and safety)

cooling water tubing & small "tab" to PCB
0.19" OD, 0.13" ID
copper "refrigeration tubing"
no fittings inside detector

Integration limit (new)



SiPM carrier PCB, qty. 4, 8 towers (32 SiPM's) each, glued to lightguide block

tungsten/scifi block

cable routing space

FEB PCB stack
2 - 3 PCB's

4x aluminum 3/16" hex 4-40 standoffs to LG, support FEB independent of SiPM boards

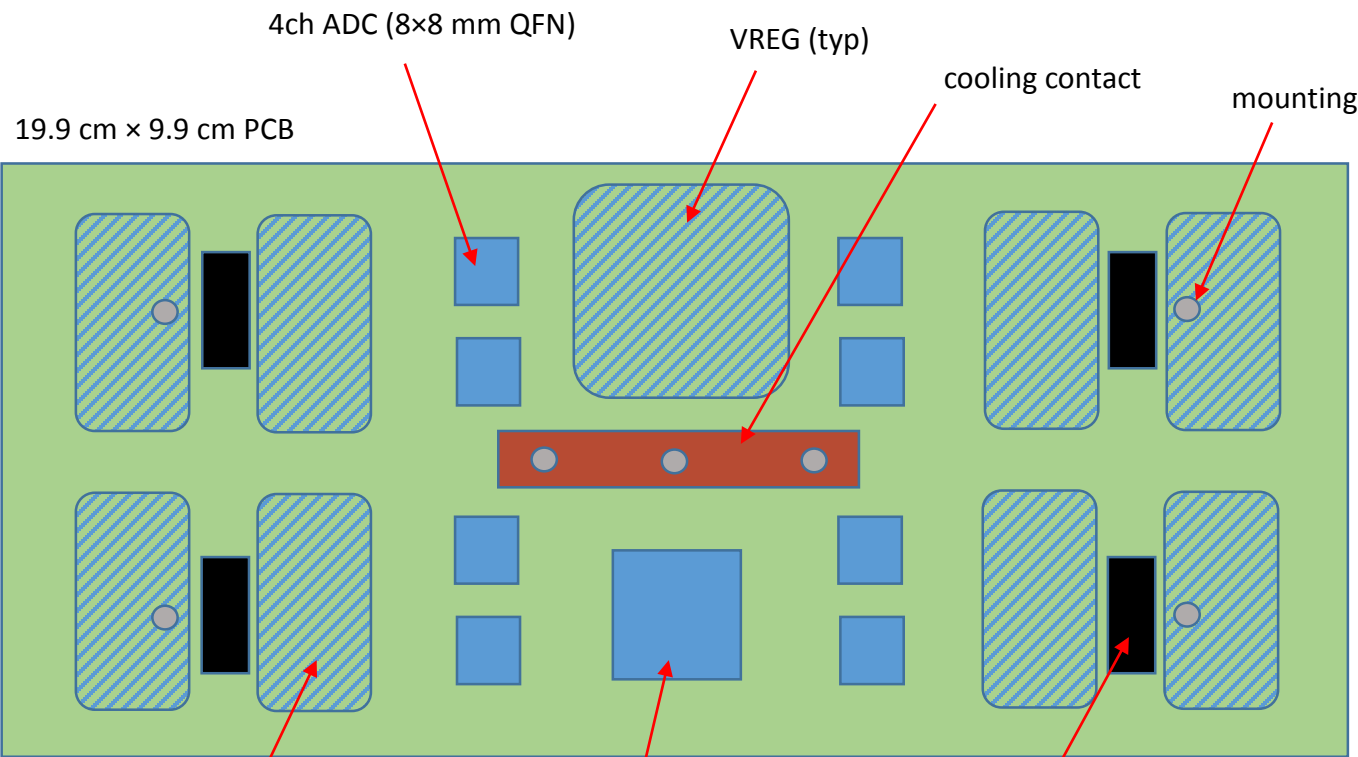
floating connectors, 1 per SiPM carrier
JAE AX01 series (30 pos) or similar



prototype FEB mounting standoff

all cables and water tubing route basically *only horizontally* on detector

rear view of inner FEB PCB



4x amplifier/shaper
(4 places)

4ch ADC (8x8 mm QFN)

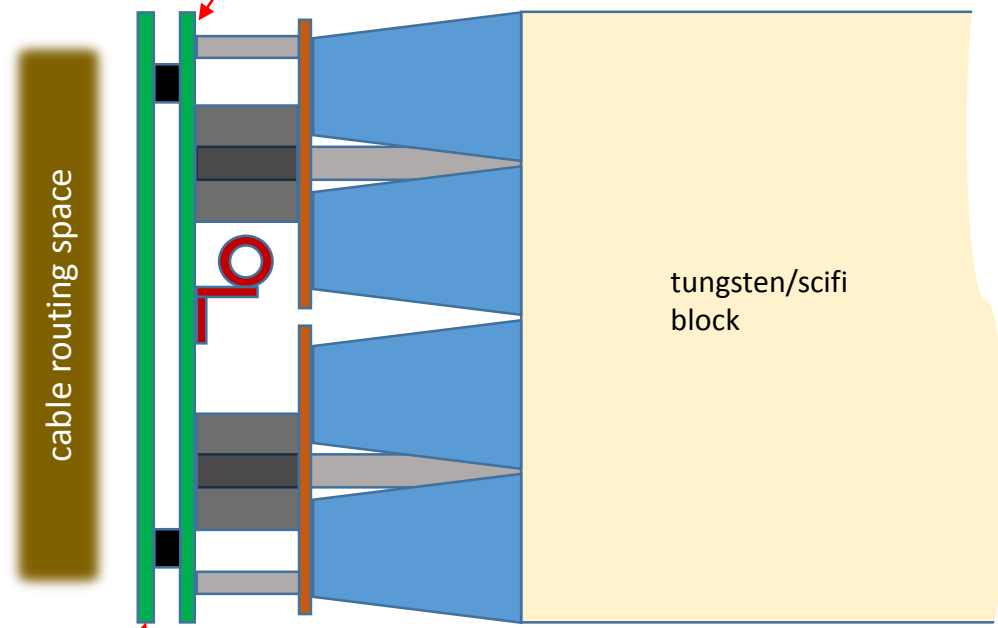
VREG (typ)

cooling contact

mounting holes (to standoffs)

FPGA (17x17mm BGA)

floating connectors
JAE AX01 series (30 pos) or similar
(8 places)



outer FEB PCB(s)
(bias voltage regulators & current monitors,
cable interface circuits and connectors,
misc. lower power stuff)

tungsten/scifi
block

