ALCOR - dRICH Readout

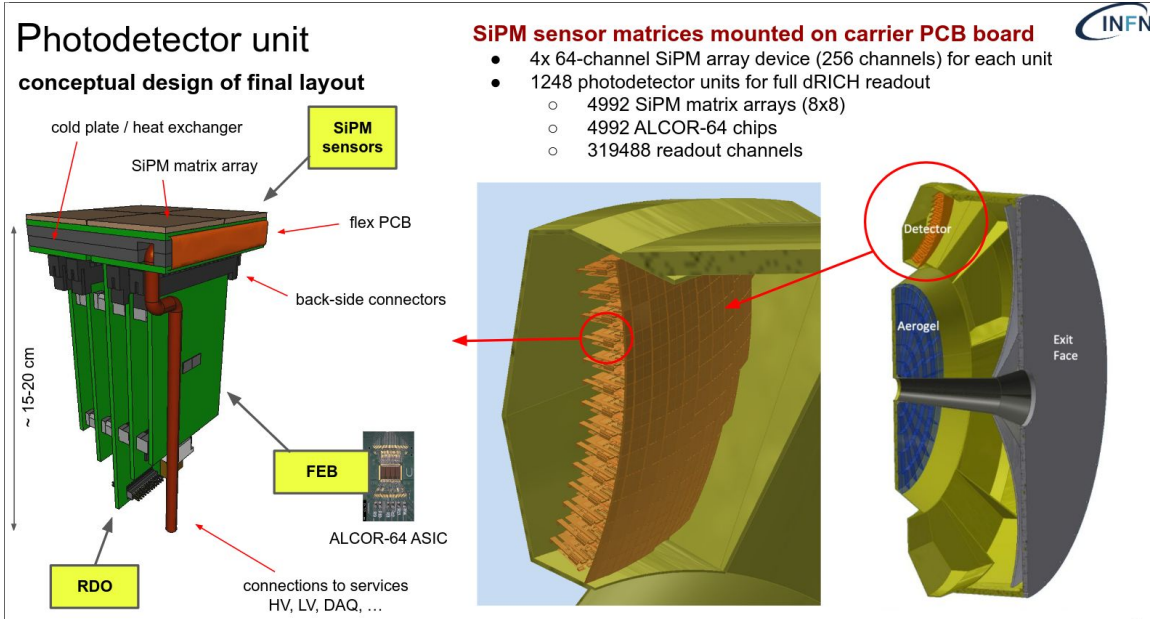
Fabio Cossio on behalf of the ALCOR and dRICH Readout Team
INFN Torino

EPIC Electronics & DAQ WG meeting
eRD109 Monthly Progress Reports

01.02.2024

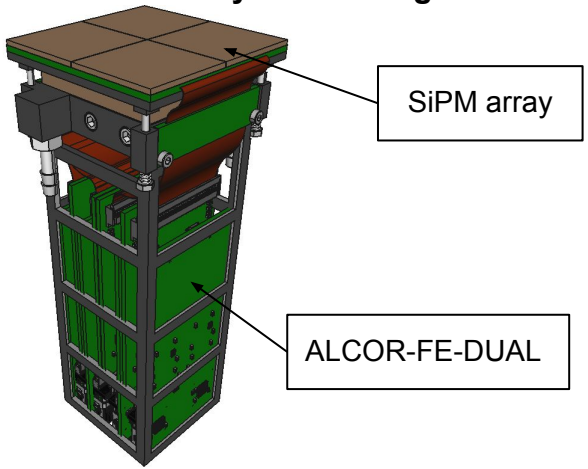
Outline

- Current status with **ALCOR v2**
- **ALCOR v3** design status
- **RDO** design status



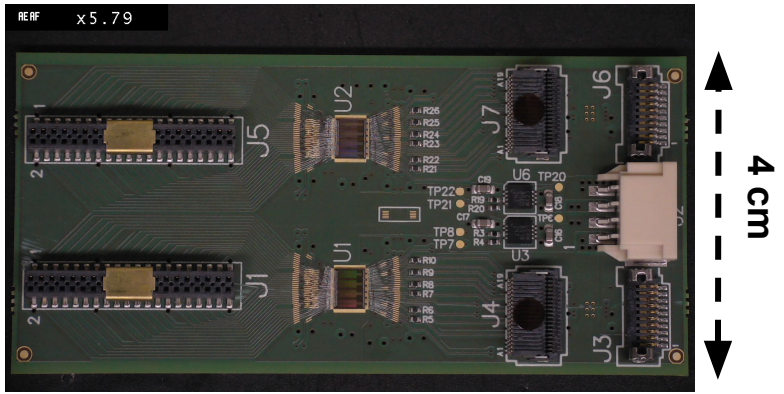
ALCOR 2023 readout system

Prototype photodetector unit (PDU) by INFN Bologna

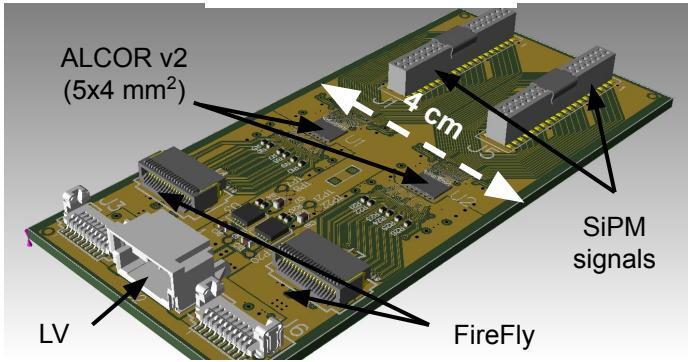


ALCOR-FE-DUAL board

- Two **32-channel** ALCOR v2 ASICs **wire-bonded** on the PCB
- 4 ALCOR-FE-DUAL boards for each PDU
- System used for Oct 2023 CERN PS beam test



designed by INFN Torino



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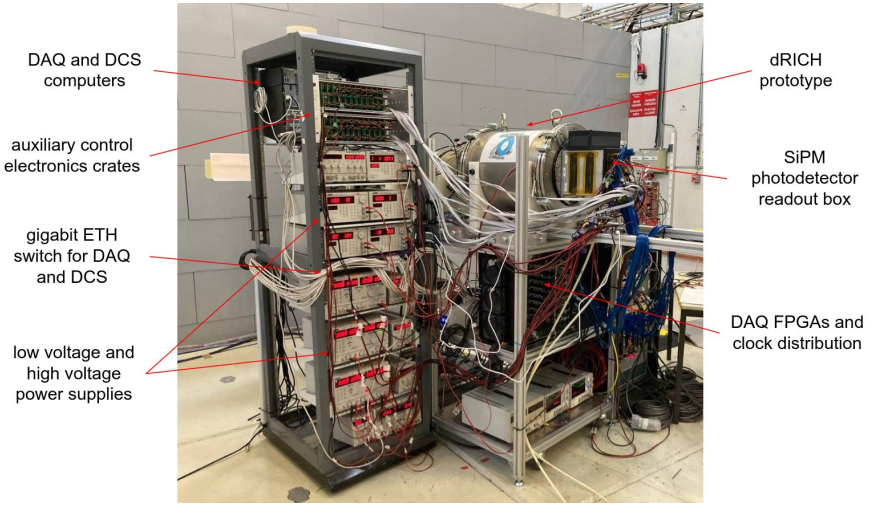
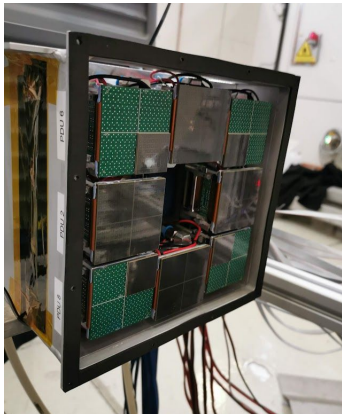
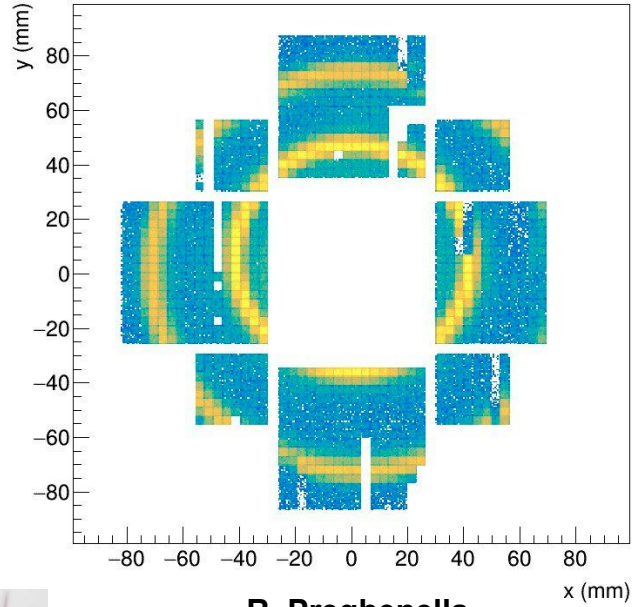




20 ALCOR-FE-DUAL, 40 ALCOR v2 (1280 channels)

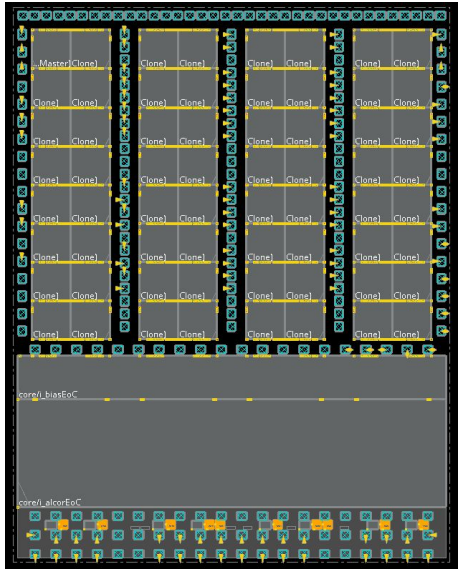


R. Preghenella

Towards ALCOR v3

Now: 32-channel wire bonded ASIC

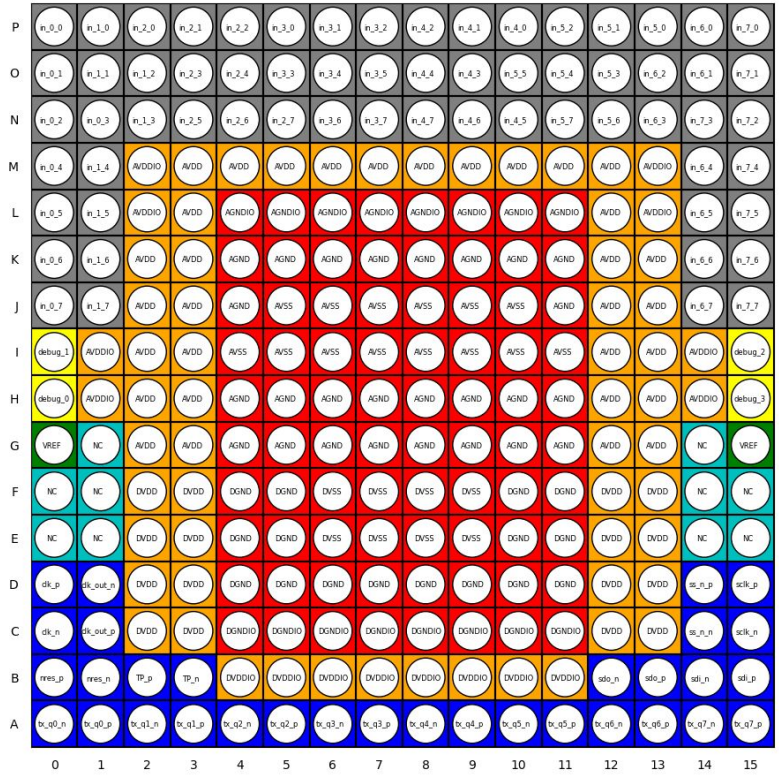
Next: 64-channel ASIC inside BGA package



8x8 pixel matrix ASIC

- SiPM inputs bump pads between the pixel sectors
- Digital EoC in the bottom part

Preliminary floorplan



256 balls BGA package (size = 12-16 mm)

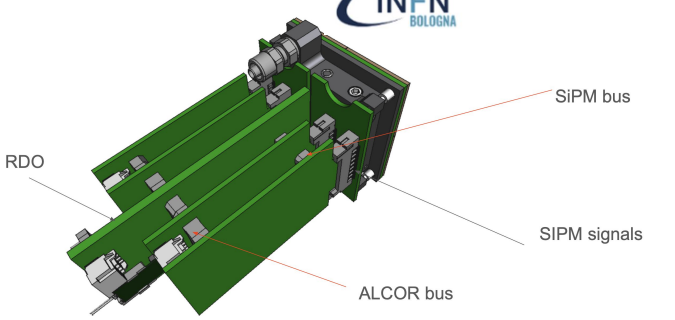
- Power and ground on inner/mid contacts
- I/O on outer contacts

Towards ALCOR v3

- **64-channel** version with **BGA package**
- Revise **ALCOR FE** design to optimize ALCOR response with dRICH SiPM sensors
  - Small internal modifications: increased amplifier bandwidth + hysteresis discriminator (schematic done, layout ongoing)
  - Studies on **time walk** correction: **ToT mode** already tested (Oct 2023 beam test) → ok, but not perfect due to *afterpulse* and *crosstalk* effects. **Slew Rate** mode also available in ALCOR v2 → to be tested in the next months (simulations, laser tests, beam test)
- **Digital logic** new features and bug fixes
  - **Digital shutter** for data reduction (EIC bunch crossing: 10 ns → 1-2 ns time window)
  - Operation of ALCOR with multiple of EIC clock frequency (98.52 MHz): **394.08 MHz** (or 295.56 MHz)
  - TDC logic fix to remove orphan data, increased EoC FIFO size to cope with higher data rates

Update on dRICH RDO design (January activity)

- Challenging constraints on dimensions for dRICH (4x9 cm)
- Started **design** for **schematics**/selection of components
- Currently porting **firmware** currently running on KC705 to AUP15 FPGA for ALCOR readout

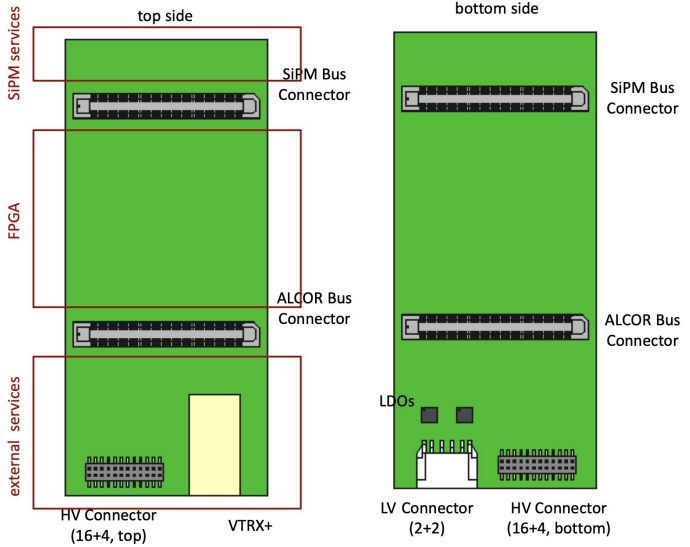


Current components candidates:

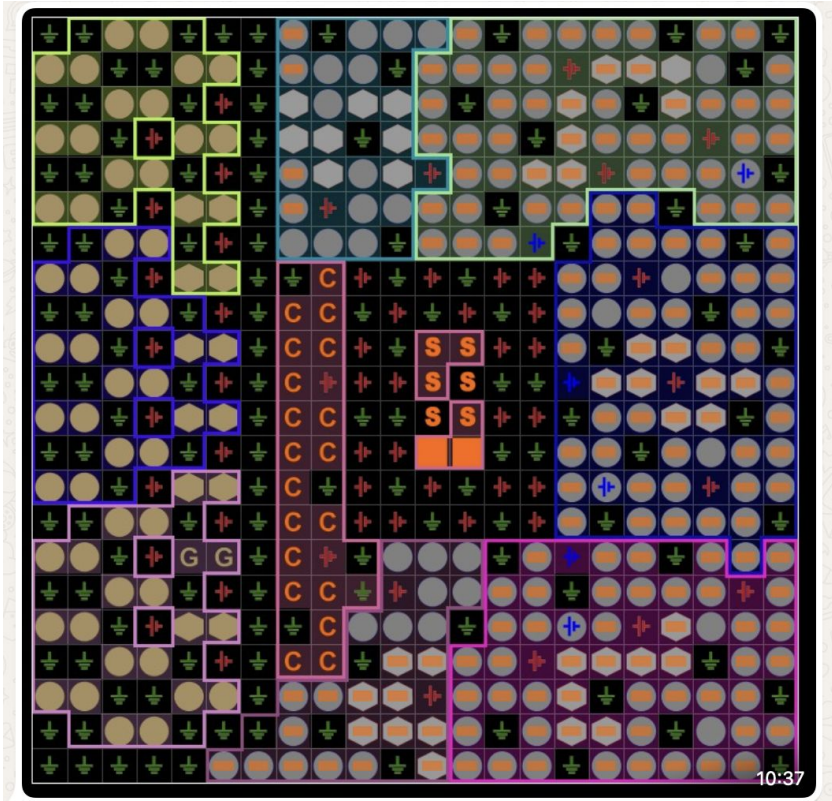
- Main FPGA: Xilinx AU15P-SBVB484
- Opt. tranc. VTRx+
- Scrubber FPGA: Microchip MPF050T-FCS9325
- QSPI Flash
- Samtec connectors (ALCORbus and SIPMbus): ERM5-050/020-XX
- Clock multiplier/jitter cleaner: SkyWorks SI5326
- T sensor: AD7416AR3 (close to LDOs and VTRX+)

- 1 MCU to be selected
- LDOs and current monitor to be selected
- I2C I/O expander TBC

We plan to “validate” with pin plan study the AU15P and then move to study PolarFire scrubber and then to LDO scheme/power management



- **pin-plan study** for Xilinx AU15P-SBVB484
- support connections for 4 ALCOR-64 (4 FEB)
- not yet fitting!



Power Management ideas:
- LV needed: 0.85, 0.90, 1.0, 1.2, 1.8, 2.5, 3.3
- primary LV may be 1.5 and 3.3V?
- MAX893L as current monitor?
- MCU? (AVR/ATmega..)
- an attractive LDO might be: LTM4709 (triple 3A)

Might be useful a common ePIC database/repository for selected components with respect to irradiations tests

AND: Preparing application for PAC of Trento proton facility for ALCOR **irradiation** in June/July and RDO in December for irradiation tests

Table 1. Product Selection Guide

Part Number	Control	Number of Inputs and Outputs	Input Frequency (MHz)*	Output Frequency (MHz)*	RMS Phase Jitter (12 kHz–20 MHz)	PLL Bandwidth	Hitless Switching	Free Run Mode	Package
Si5315	Pin	1PLL, 2 | 2	0.008–644	0.008–644	0.45 ps	60 Hz to 8 kHz	•		6x6 mm 36-QFN
Si5316	Pin	1PLL, 2 | 1	19–710	19–710	0.3 ps	60 Hz to 8 kHz			6x6 mm 36-QFN
Si5317	Pin	1PLL, 1 | 2	1–710	1–710	0.3 ps	60 Hz to 8 kHz			6x6 mm 36-QFN
Si5319	I²C/SPI	1PLL, 1 | 1	0.002–710	0.002–1417	0.3 ps	60 Hz to 8 kHz		•	6x6 mm 36-QFN
Si5323	Pin	1PLL, 2 | 2	0.008–707	0.008–1050	0.3 ps	60 Hz to 8 kHz	•		6x6 mm 36-QFN
Si5324	I²C/SPI	1PLL, 2 | 2	0.002–710	0.002–1417	0.3 ps	4 Hz to 525 Hz	•	•	6x6 mm 36-QFN
Si5326	I²C/SPI	1PLL, 2 | 2	0.002–710	0.002–1417	0.3 ps	60 Hz to 8 kHz	•	•	6x6 mm 36-QFN
Si5327	I²C/SPI	1PLL, 2 | 2	0.002–710	0.002–808	0.5 ps	4 Hz to 525 Hz	•	•	6x6 mm 36-QFN
Si5328	I²C/SPI	1PLL, 2 | 2	0.008–346	0.002–346	0.35 ps	0.05 Hz to 6 Hz	•	•	6x6 mm 36-QFN
Si5366	Pin	1PLL, 4 | 5	0.008–707	0.008–1050	0.3 ps	60 Hz to 8 kHz	•		14x14 mm 100-TQFP
Si5368	I²C/SPI	1PLL, 4 | 5	0.002–710	0.002–1417	0.3 ps	60 Hz to 8 kHz	•	•	14x14 mm 100-TQFP
Si5369	I²C/SPI	1PLL, 4 | 5	0.002–710	0.002–1417	0.3 ps	4 Hz to 525 Hz	•	•	14x14 mm 100-TQFP
Si5374	I²C	4PLL, 8 | 8	0.002–710	0.002–808	0.4 ps	4 Hz to 525 Hz	•	•	10x10 mm 80-BGA
Si5375	I²C	4PLL, 4 | 4	0.002–710	0.002–808	0.4 ps	60 Hz to 8 kHz	•	•	10x10 mm 80-BGA
Si5376	I²C	4PLL, 8 | 8	0.002–710	0.002–808	0.4 ps	60 Hz to 8 kHz	•	•	10x10 mm 80-BGA

***Note:** Maximum input and output rates may be limited by speed rating of device. See each device's data sheet for ordering information.

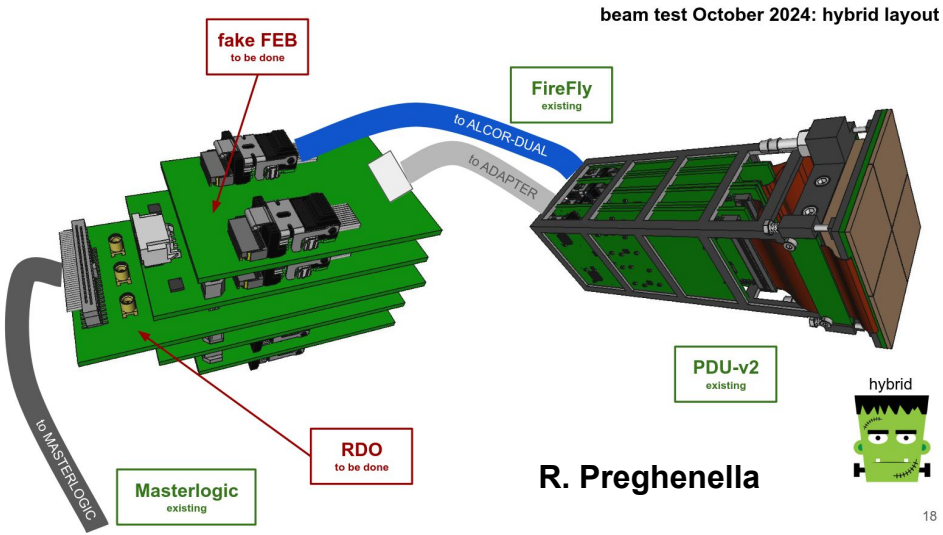
Note on clock selection/jitter cleaner:

- current candidate assumes we recover 98.5 MHz from link and we then multiply x4 to feed ALCOR (via FPGA)
- any experience in radiation? This is critical!

FEBs design

This will allow us to replace the stack of commercial FPGAs with prototype RDOs already during 2024 (without new ASIC)

- **“Fake-FEB”**: interface board only for 2024 activities
  - Use current **ALCOR-FE-DUAL** boards with **RDO**
  - Defined digital signals distribution: it will mount some LVDS splitters to control the two 32-channel ALCOR chips on the ALCOR-FE-DUAL



- **Final FEB**: ePIC dRICH Front-End Board
  - Host ALCOR v3 chip inside the BGA package (available in 2025)
  - Started selection of components to match RDO design

Plans for 2024

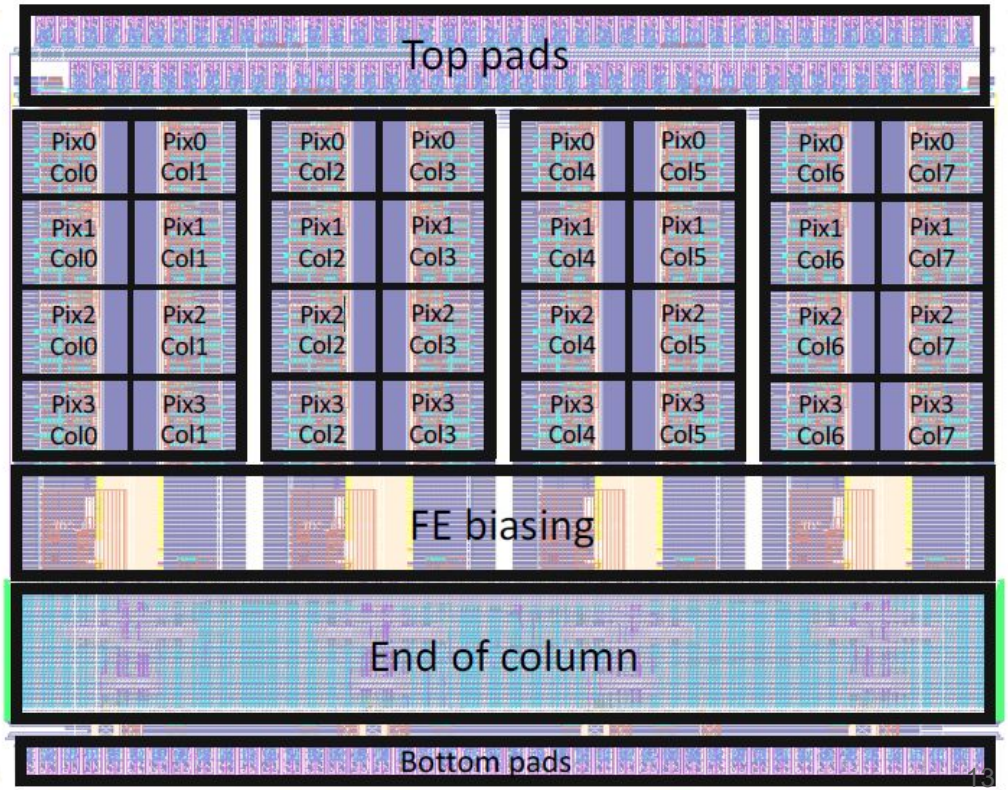
- Complete design of **ALCOR v3**: ASIC tape-out (Sep 2024) + package design (Fall 2024)
- Design of **RDO prototype,** as close as possible to final (Jun 2024)
- **RDO readout** using current ALCOR FE-DUAL board (Oct 2024 beam test)
- **Irradiation tests** campaign (SEU and TID) at Centro of Proton-Therapy in Trento: ALCOR v2 (Jul 2024) and RDO (Dec 2024)

Spare slides

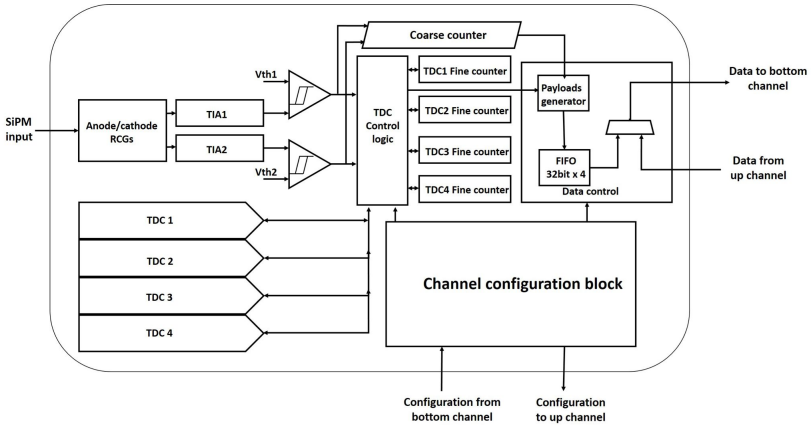
ALCOR (**A** **L**ow Power **C**hip for **O**ptical Sensor **R**eadout)

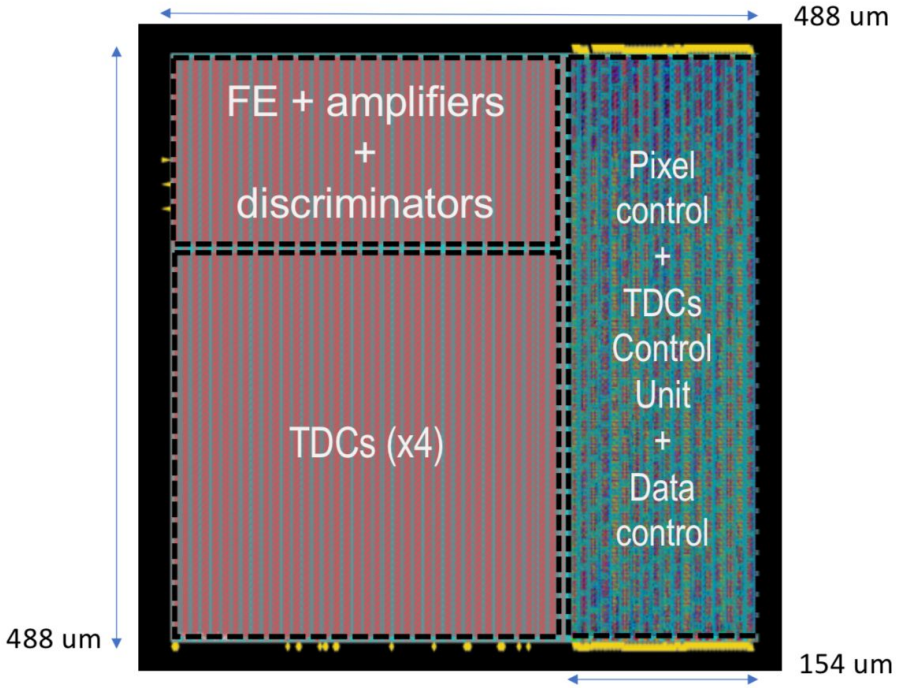
ASIC developed for the readout of the EIC dRICH SiPM sensors

- **32-pixel** matrix (8x4) mixed-signal ASIC
- **SiPM readout**: single-photon time tagging + Time-over-Threshold measurement
- 32-bit (64-bit in ToT mode) event word generated on-pixel and propagated down the column
- **Fully digital output**: 4 LVDS 320 MHz DDR Tx links



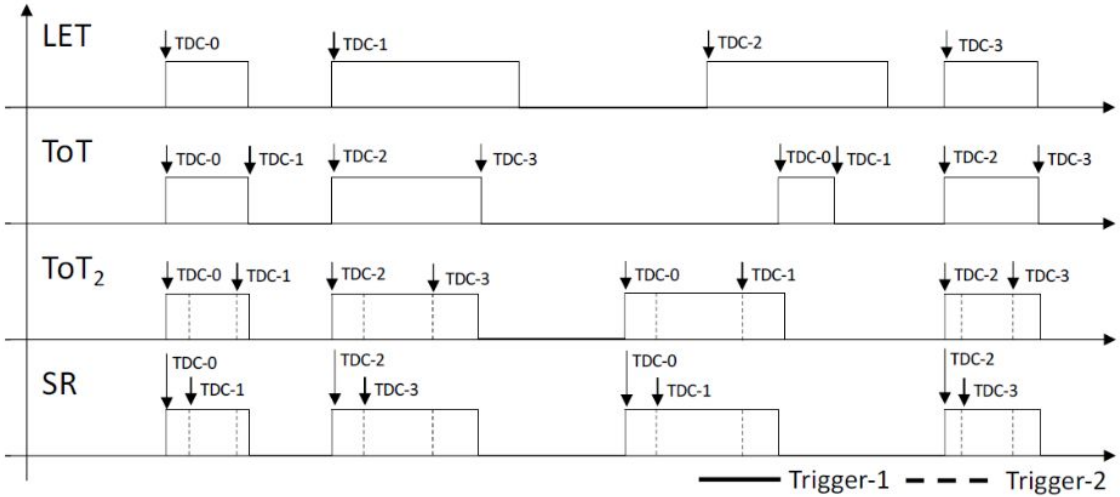
Pixel architecture





- **TIA amplifier** with RCG input stage
- 2 independent post-amp branches with 4 gain settings
- 2 **leading edge discriminators** with independent (and per pixel) threshold settings (6-bit DAC)
- 4 **TDCs** based on **analogue interpolation** with 25-50 ps time-bin (at 320 MHz clock frequency)
- Pixel control logic handles TDC operation, pixel configuration and data transmission

ALCOR pixel operating modes



4 operating modes:

- LET: leading edge measurement
- ToT: Time-over-Threshold measurement using the first discriminator for both edges
- ToT2: Time-over-Threshold measurement using both discriminators
- SR: slew-rate measurement

Each mode can be set to:

- FE: normal operation mode
- FE_TP: send test-pulse to analogue front-end
- TDC_TP: send test-pulse to pixel control logic to test and calibrate TDCs (bypass front-end)

Each pixel can also be disabled

ALCOR v3 (digital)

Definition of ALCOR-64 digital I/Os to match RDO design → **16 LVDS signals**

- 8 DOUT
- 1 CLKIN
- 1 CLKOUT
- 1 TP/SHUTTER
- 1 RESET
- 4 SPI

394.08 MHz clock frequency operation (4 x 98.52 MHz): tested ALCOR v1 at 390 MHz with promising results, more detailed tests and simulations are required, digital implementation must be re-done with new constraints

Digital shutter: “inhibit” pixel digital logic to reduce data throughput (10 ns bunch crossing, 250 ps bunch length, select 1-2 ns → 5-10x data reduction before ALCOR digitization)
→ Asynchronous digital shutter implemented in ALCOR v3 pixel logic

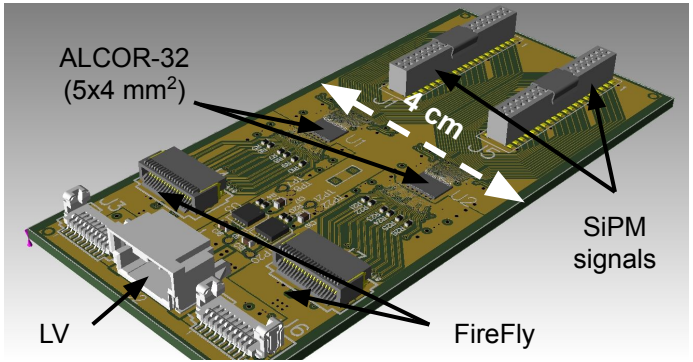
- Programmable delays to guarantee same time window for all the channels across the matrix
- Need to evaluate effect due to time-walk and thresholds dispersion

ALCOR v3 FEB

Start design of the EPIC dRICH Front-End Board (FEB), hosting the ALCOR v3 chip inside the BGA package

- Two ALCOR v2 (32 channels) replaced by one ALCOR v3 (64 channels)
- Firefly connectors replaced by connectors towards RDO board
- Add annealing Mosfets (currently mounted on adapter board)

ALCOR-FE-DUAL (2023-24 version)



Photodetector unit
(conceptual design
of final layout)