EICROC Progress Report

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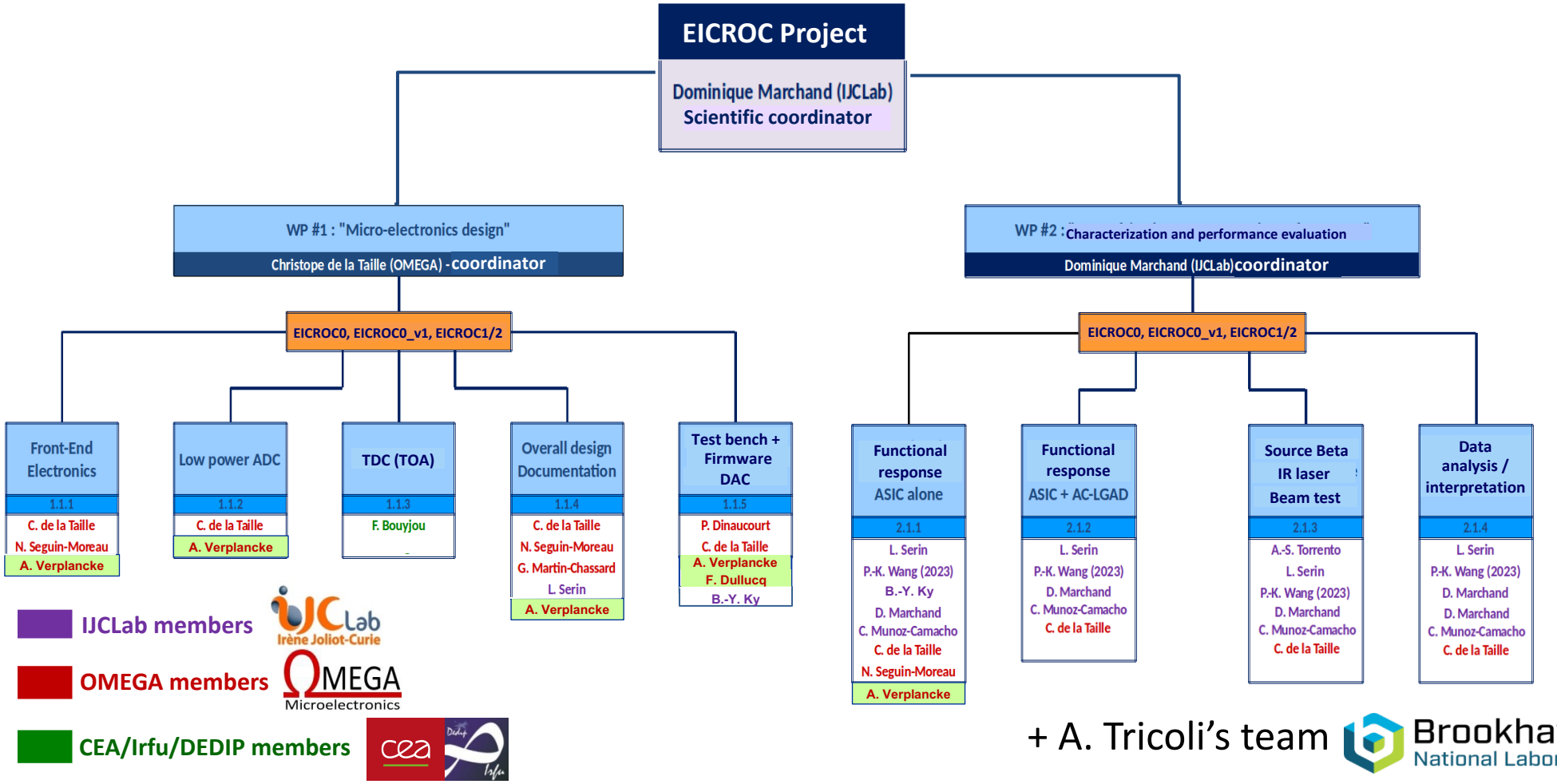
Objective: **Development** and **characterization** of an **ASIC EICROC (32 x 32)**
able to read-out the new generation of pixelated (500 x 500 µm^2) silicon sensors: **AC-LGAD**
(**L**ow-**G**ain **A**valanche **D**iode) coupled **AC**
for the **Electron Ion Collider** (EIC)
1st intention: optimized for **Far Forward detectors:** the **Roman Pots**

Method: stepping up through succesive ASIC iterations
to control performances fulfilling ePIC detector requirements

- **EICROC0 prototype** (16 channels; 4 x 4): under test since March ‘23

The EICROC project team



IJCLab members

OMEGA members

CEA/Irfu/DEDIP members

+ A. Tricoli's team

synergy with
Japanese & Taiwanese teams

IJCLab : + **1 year postdoctoral position (Spring '24, Univ. Paris-Saclay/P2I)**

EICROC0 requirements and design: 16 channels (4x4)

Requirements:

- pixel size **0.5 x 0.5 mm²** *(HGTD 1.3x1.3 mm²)*
- low power consumption < **2 mW/channel**
- low jitter **~ 20 ps**
- low noise **~ 1 mV/channel**
- sensitivity to low charge **(2 fC)**
- time resolution: **30 ps**
- spatial resolution: **50 microns**

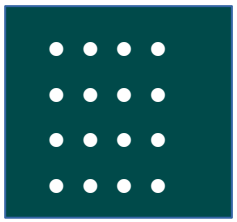
Charge sharing studies

(simulation + β source w/ **ALTIROC1**_v2)

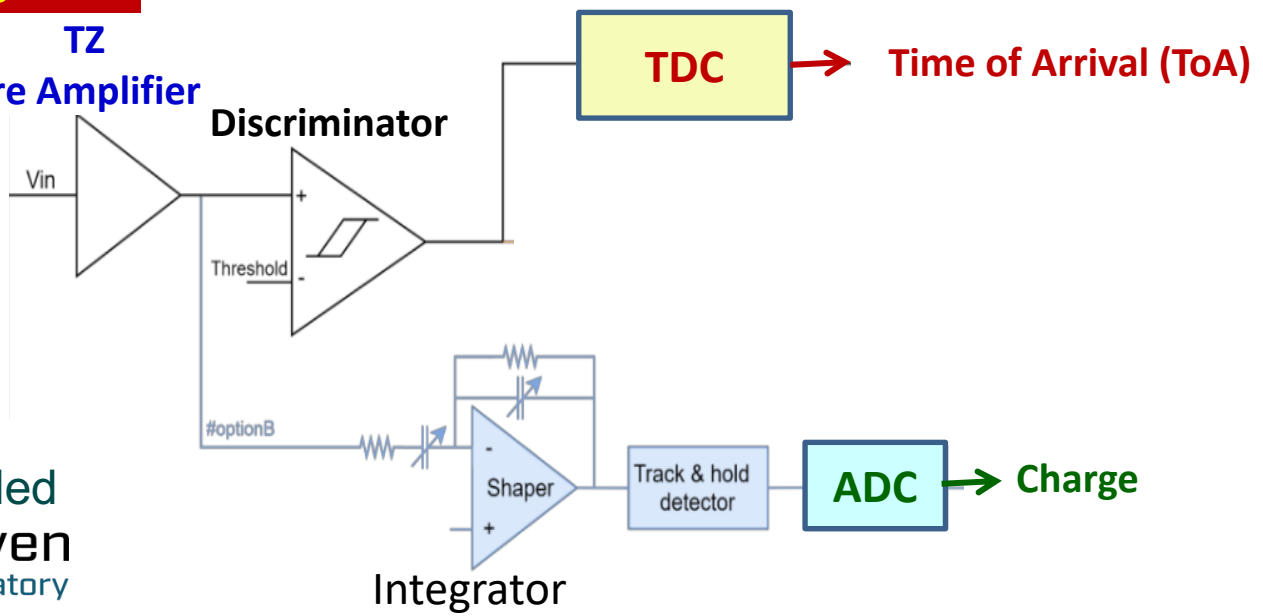
EICROC0 design:

- **TZ Pre Amplifiers** from ALTIROC (ATLAS/HGTD)
- 10 bit **TDC** from HGCROC (CMS, CEA/Irfu)
- **8 bit ADC** for time-walk correction (AGH Krakow, adapted from HGCROC)

1 channel (1 pixel) schematics



AC-LGAD
pixelated sensor
designed and provided
by Brookhaven National Laboratory



Compared to ALTIROC (ATLAS/HGTD), ToT TDC (non-linear behavior versus the deposited charge) replaced by an ADC

EICROC project: status

EICROC0 characterization (OMEGA, CEA/Irfu, IJCLab):

- **Individually each component shows performance in agreement with design**
- Evaluation of cross-talk between channels underway, results to be released shortly
- Further investigation of noise/clock couplings mandatory to drive next ASIC iteration (EICROC0A)
- Support to BNL team to set up an EICROC0 test bench
- Periodic working meetings with BNL
- Periodic progress reports in ePIC eRD112/AC-LGAD meetings

Outreach

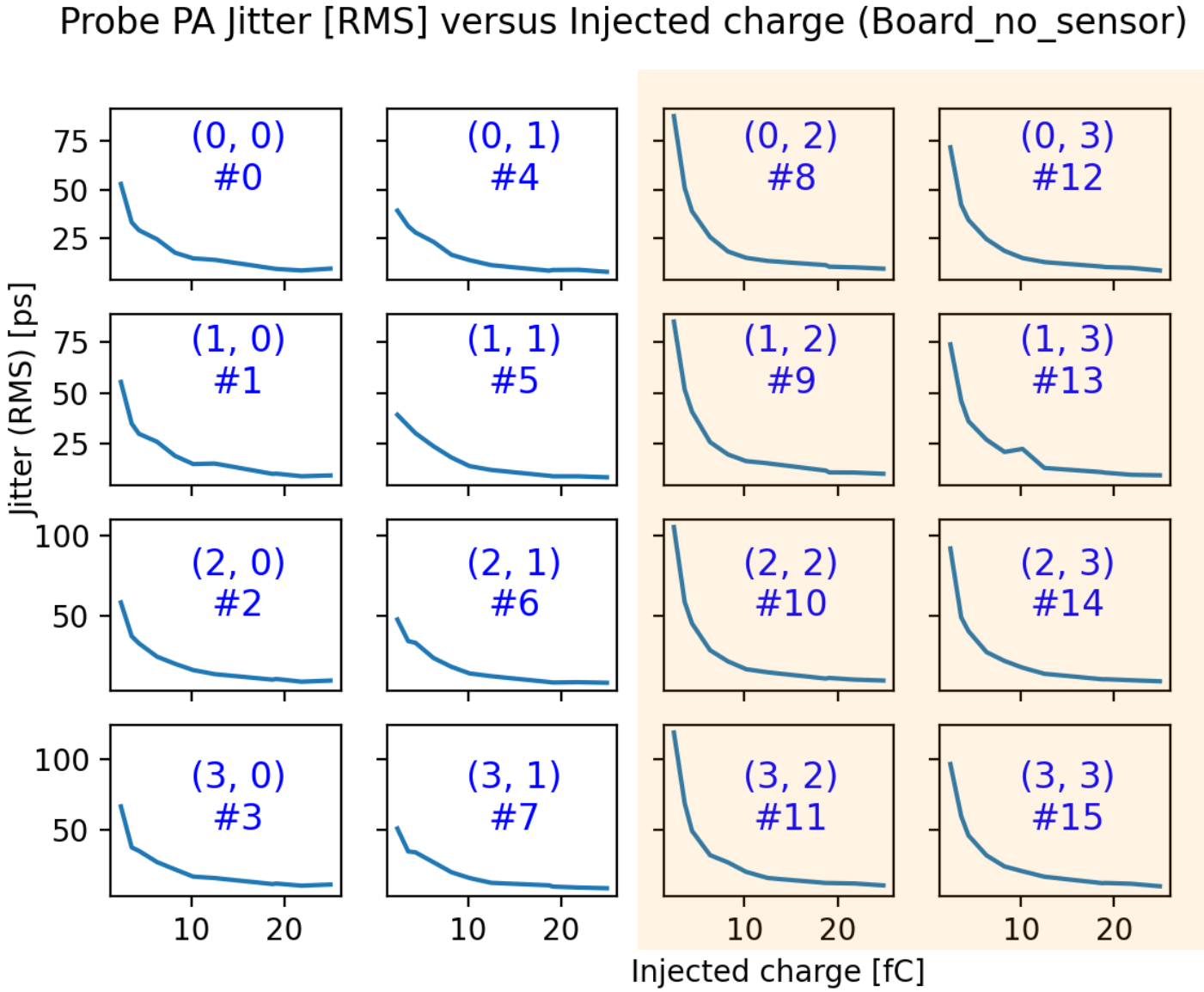
P.-K. Wang PhD defense: 12/09/2023, partly on EICROC project

Strong support from DOE/eRD109 Consortium

EICROC Project: recent/on-going work

- Still investigationg couplings
- Focusing on data (rather than analogiocal probe PA signal)
  - ➔ Efficiency curves scripts (discriminator threshold, TDC hits vs inj. Charge)
- Exploiting External Trigger
- Board with AC-LGAD sensor (IJCLab & BNL) ➔ oscillations > 2 PA channels observed

EICROC0: Probe PA Jitter vs Injected Charge



EICROC Project: update & perspectives

ePIC Argonne 2024 NATIONAL LABORATORY

01/09 - 01/13, 2024

A very fruitful working winter meeting!

- « AC-LGAD and associated electronics & DAQ » dedicated sessions: workfest:
  - Feedbacks from CMS/HGCROC testing (wire/bimp-bonding),
  - Feedbacks from FermiLab/FCFD testing
- EICROC0 hands-on sessions organized by the BNL team (about 70 pers.)
- EICROC0 « expert » working sessions on the test bench (thanks to Argonne colleagues for providing scope, LV, place, help):
  - scripts (discri, Ext. Trigger) / method sharing, bootfiles updates,
- In person very constructive meetings/chats with people involved in FW & Far FW detectors (BNL team, Alex J., Yulia F., Zhenyu Y., Satoshi Y., Mathieu B., …) to draw perspectives for ramping up on EICROC0 testing

  ➡️ Exploiting EICROC0 analogical Probe PA output signals & digital outputs:

  * Laser test bench (at BNL) requires synchronisation capabilities,
  * Beta source (IJCLab & BNL) requires triggerless acquisition
  * Will to take part to the DESY testbeam next June at DESY (wire- & bump- bonded AC-LGAD & EICROC0)

EICROC Project: update & perspectives

- **EICROC0 chips**
  - 15 will be sent to BNL mid-February in view of hybridation (EICROC0+AC-LGAD)

- **Updated EICROC0 PCBs (test boards)**: 20 pieces
  - Submitted for fabrication before Christmas should be received by mid- January
    Unfortunate misunderstanding between Company & OMEGA
    ➡️ delivery expected 2nd week of February
  - Components for cabling: ordered ; delivery expected next week
  - Cabling will be performed at IJCLab by the end of February
  - 5 PCBs will be sent to IPHC (Strasbourg, France) to wire-bond an EICROC0 (March)
  - 4 PCBs will be sent to IPHC (Strasbourg, France) to wire-bond an EICROC0 + AC-LGAD
    [AC-LGAD sensors provided by BNL]
  - 6 PCBs will be sent to BNL (March)
  - 5 PCBs will be sent to IPHC (Strasbourg, France) to wire-bond an hybrid
    [when hybrids ready; Hybrids provided by BNL]

Should we consider to also test HPK AC-LGADs?

EICROC Project: update & perspectives

Next iterations: EICROC0A & EICROC1

- **EICROC0A: including a low power ADC + improved testing capabilities**

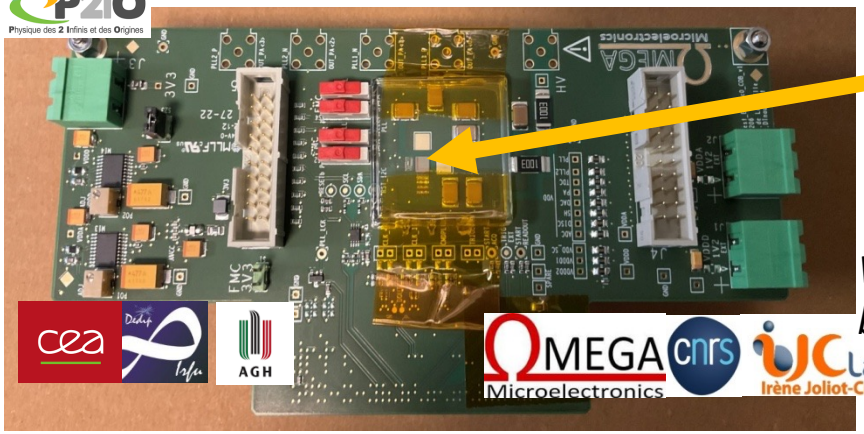
- **EICROC1:**
  - **4 (or 8) x 16 to investigate floor planning**
  - **improved/additional testing capabilities**

EICROC (0A & 1) and H2GCROC ASICs will be submitted together for fabrication (summer/fall 2024)

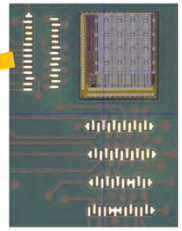
BACKUP

Status of EICROC0 Test Bench at IJCLab

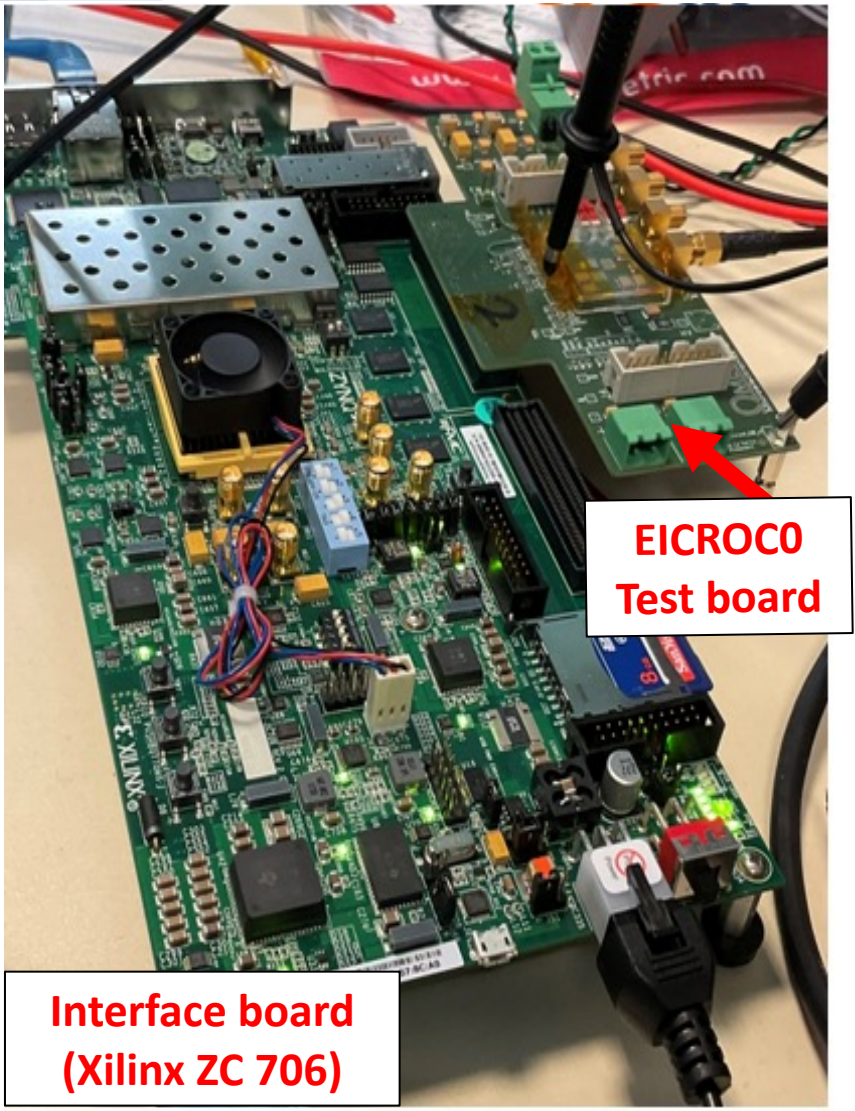
EICROC0 Test board



EICROC0 chip



Wire-bonding by Brookhaven National Laboratory

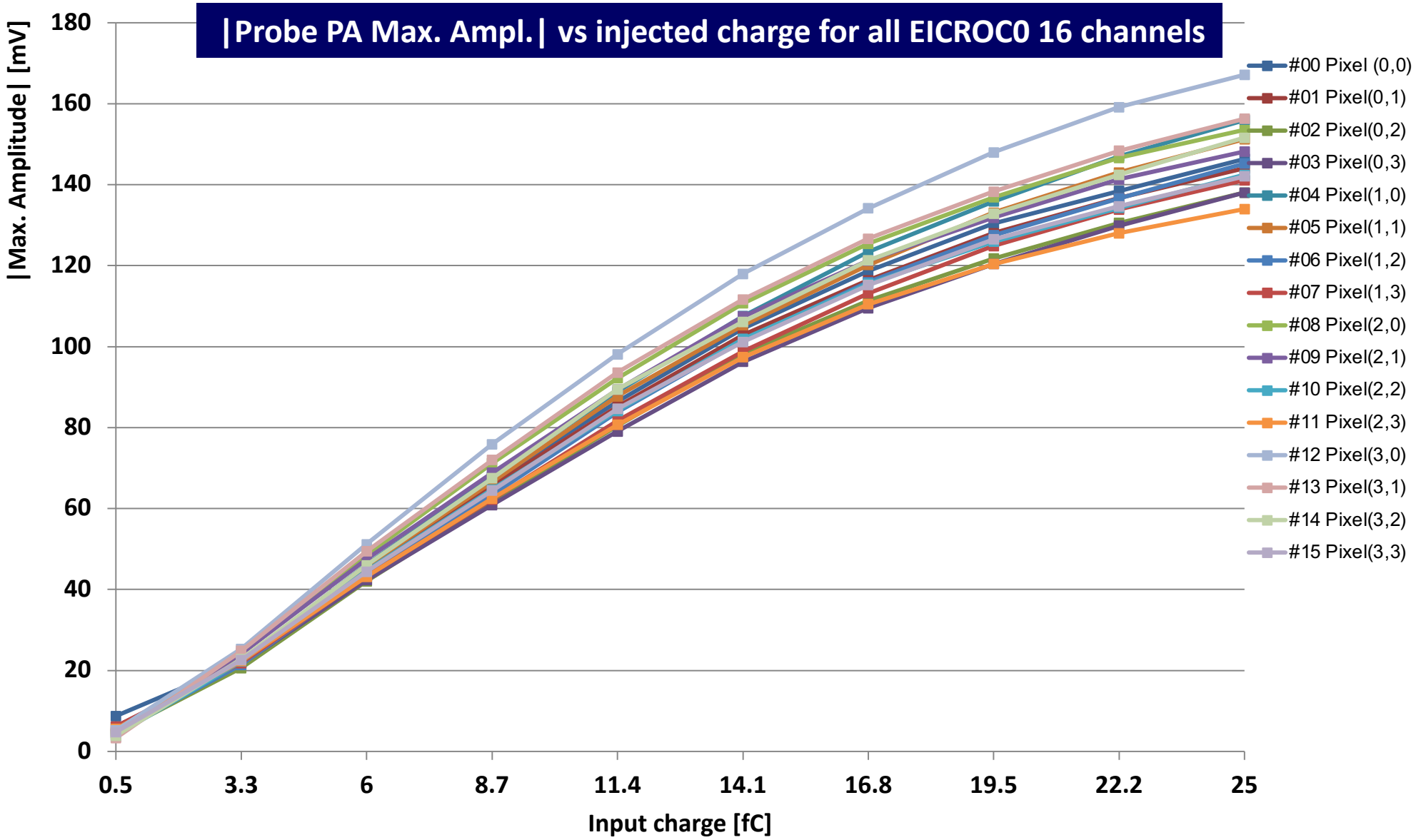


EICROC0 test bench operational at IJCLab since March '23

- ✓ I^2C communication (firmware + software developments)
- ✓ Data stream written/read
- ✓ EICROC0 DC levels
- ✓ Discri. threshold exploration
- ✓ **EICROC0 charge injection system (0 to 25 fC)**
- ✓ **EICROC0 decoding (TDC, ADC) Firmware + software**
- ✓ **External trigger**: *signal directly injected into TDC*

Additional EICROC0 test benches operational at:
OMEGA (May '23), BNL (July. '23), CEA/Irfu (Sept. '23)

EICROC0 TZ Pre Amplifier Probe output signal amplitudes



Status of EICROC0 Test Bench at IJCLab

Current studies [board w/ EICROC0, no AC-LGAD sensor]

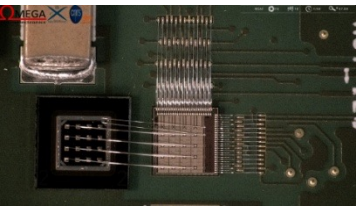
- **TZ Pre Amplifier** output signals
  - SNR > 70 for 12.5 fC input ; SNR > 6 for 1 fC input)
  - Jitter evaluation: < 20 ps (≥ 6 fC) ; 8 ps (25 fC)

- **TDC** performance (**alone**): functional
  - quantification step (~25 ps) in good agreement with design
  - observation of a large noise coupled to 160 MHz clock
  - Time of Arrival resolution estimated to 14 ps (25 fC)

- **ADC** performance (**alone**) functional

- Evaluation of cross-talk between channels underway

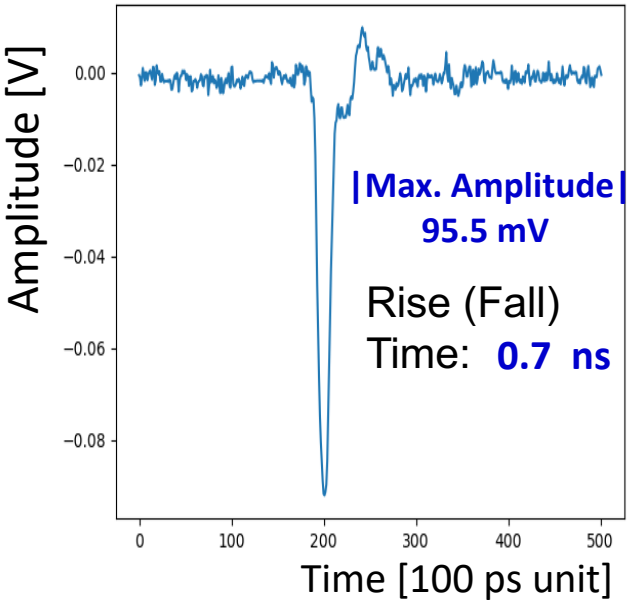
- Further nvestigation of noise / clock (160 MHz) coupling issues (**TDC and ADC**)

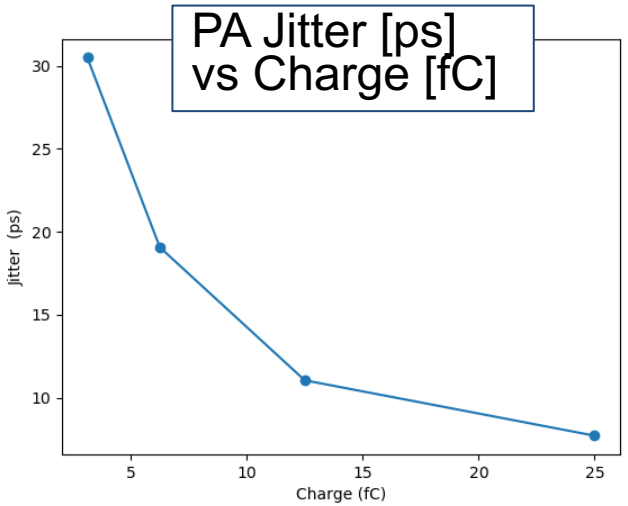


Wire-bonding by Brookhaven National Laboratory

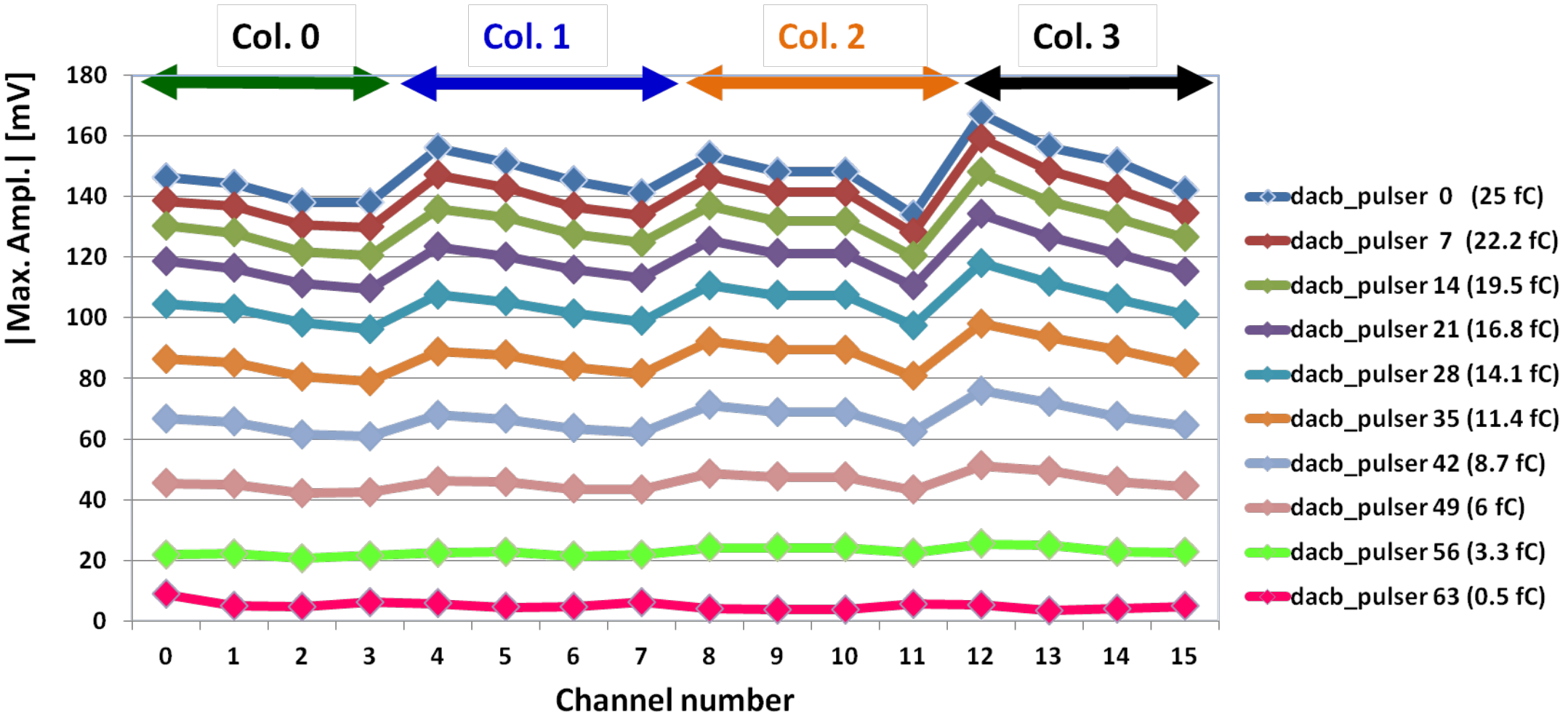
Short term plan: to evaluate performances of the existing board **w/ EICROC0 + AC-LGAD (4 x 4)**

Typical **PA output signal** (12.5 fC input)

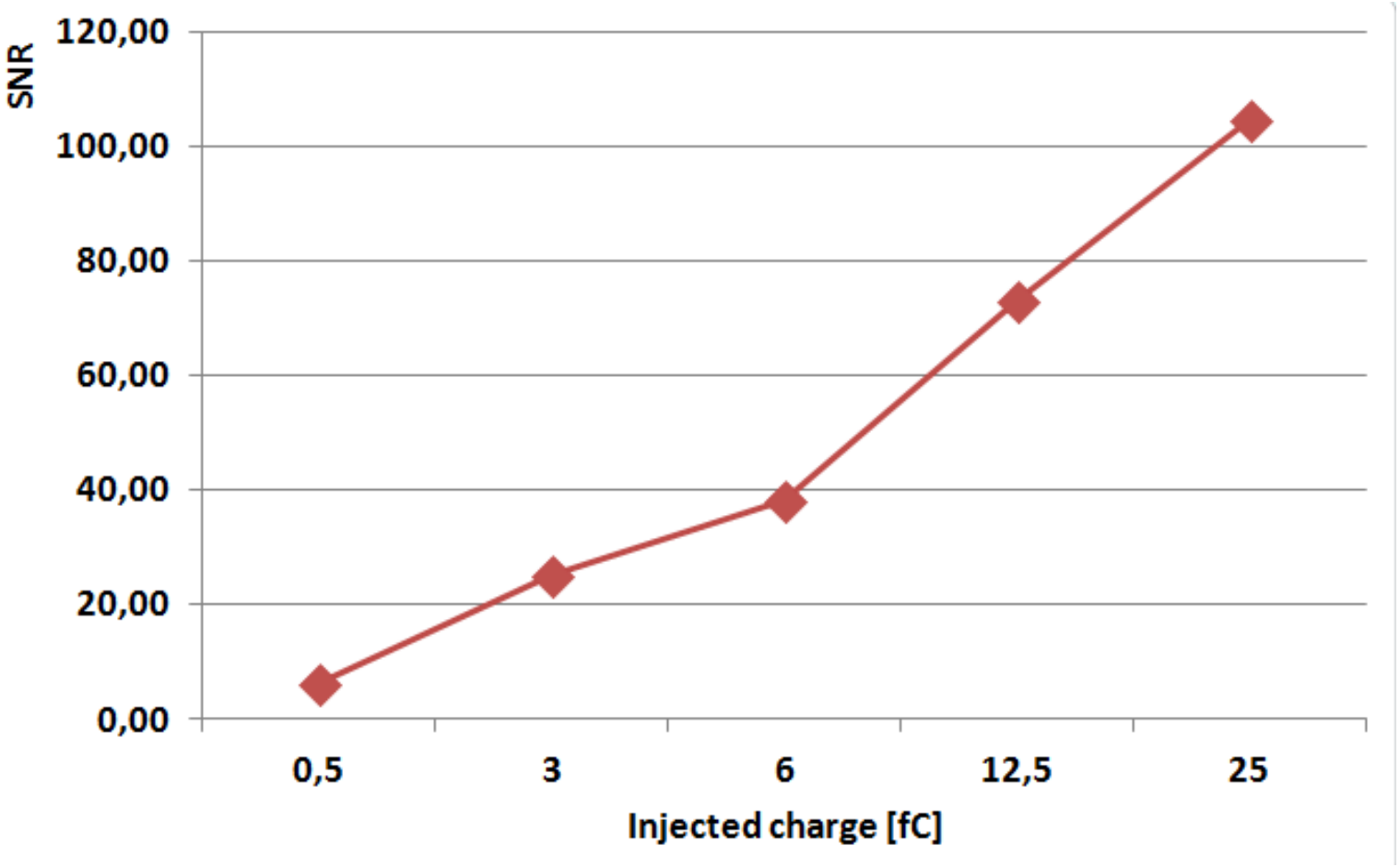




EICROC0 TZ Pre Amplifier Probe output signal amplitudes

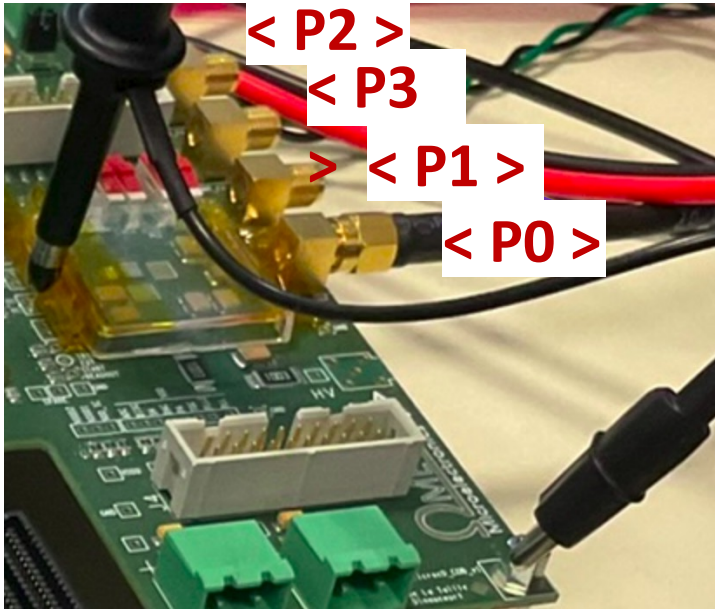


EICROC0 Probe PA output Signal to Noise Ratio (SNR)

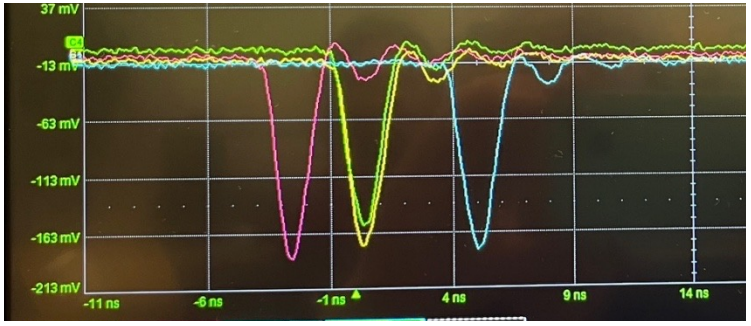


EICROC0 TZ Pre Amplifier Probe output signals

Pixel / Channel Mapping	Column 0	Column 1	Column 2	Column 3
Line 0	Pixel (**0**,0) **#00**	Pixel (**1**,0) **#04**	Pixel (**2**,0) **#08**	Pixel (**3**,0) **#12**
Line 1	Pixel (**0**,1) **#01**	Pixel (**1**,1) **#05**	Pixel (**2**,1) **#09**	Pixel (**3**,1) **#13**
Line 2	Pixel (**0**,2) **#02**	Pixel (**1**,2) **#06**	Pixel (**2**,2) **#10**	Pixel (**3**,2) **#14**
Line 3	Pixel (**0**,3) **#03**	Pixel (**1**,3) **#07**	Pixel (**2**,3) **#11**	Pixel (**3**,3) **#15**



PA output signals through SMA connector s (PCB back plane)



Feature of EICROC0 test board:
Observation of 4 Probe PA channels simultaneously

1 Probe PA per column
Ex.: #00, #04, #08, #12