

eRD109: Progress Report

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UC Santa Cruz UFSD group

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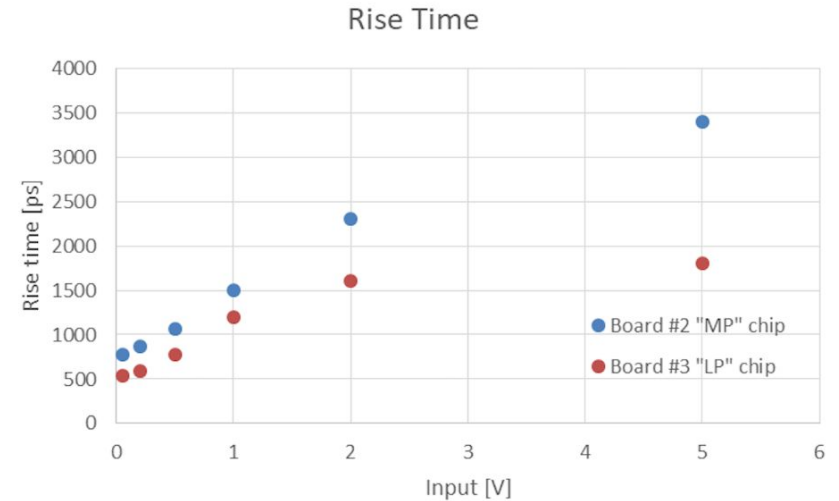
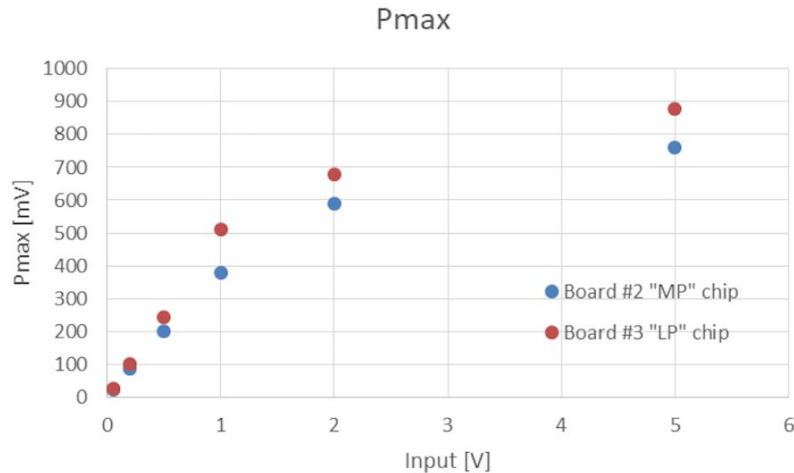
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Investigating third party ASIC solutions for AC-LGAD ToF detectors

- We gave a detailed report on December 14th ([link](#)) – see slides for details
- ***HPSoCv2 ASIC (Nalu Scientific):***
 - Chip with fixed digital back-end under fabrication at TSMC – expected by March
 - Analog front-end characterized standalone; testing with strip sensors currently underway
 - Once revised chip is in-hand, full re-characterization with and without sensors planned
- ***AS-ROC (Anadyne Inc.)***
 - Components on the readout boards reworked → boards working as expected
 - Reliable power measurement made: chip marked as "LP" drains 1.4 mW per channel, while the chip marked as "MP" drains 0.88 mW per channel (likely incorrectly labelled & swapped)
 - Still observe issues with cross-talk between channels; chip designers are coming to UC Santa Cruz next week to test & investigate this issue
 - Full characterization underway in the next 1-2 months, early results on next slide

AS-ROC characterization

- The performance of the "LP" chip is better in terms of preamp gain, rise time and dynamic range. The noise of the "LP" chip is also slightly (<10%) higher, so the S/N is more or less the same in both. The clear advantage of "LP" is the lower rise time.



Milestones and timelines

- ~~1. ASROC and HP-SoC board design, layout, and production (Summer-Fall 2023)~~
2. ASROC and HP-SoC ASIC characterization (Fall 2023)
3. ASROC and HP-SoC integrated system tests & characterization. ASICs will be paired with eRD112 sensors (Winter 2024)

Both chips have been characterized standalone and when paired with sensors already → however, testing will continue as we continue to learn about the performance of these chips & receive next version of the HPSoCv2 chip