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Status report of the eRD109 project on SALSA chip development

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EPIC DAQ/electronics WG meeting

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SALSA CHIP TARGET SPECIFICATIONS

Versatile front-end characteristics

- Dedicated to MPGD detectors and beyond
- 64 channels
- Large input capacitance range, optimized for 50-200 pF, reasonable gain up to 1nF
- Large range of peaking times: 50-500 ns
- Large gain ranges: 0-50 to 0-5000 fC
- Large range of input rates, up to 100 kHz/ch with fast CSA reset (limit assumed for EPIC: 25 kHz/ch)
- Reversible polarity
- Front-end elements can be by-passed

Digital stage

- Fast sampling ADC for each channel on 12 bits (> 10 effective bits) at up to 50 MS/s
- Possibility to double rates by coupling pairs of channels
- Integrated DSP for internal data processing and size reduction, treatment processes to be selected according to user needs
- Continuous readout compatible with streaming DAQ foreseen at EIC, triggered mode also available
- Several 1 Gb/s output data links

General characteristics

- ~1 cm² die size, implemented on modern TSMC 65nm technology
- Low power consumption ~ 15 mW/channel at 1.2V
- Radiation hardened (SEU, TID), working at 2T magnetic field

STATUS OF SALSA0 AND PRISME PROTOTYPES

SALSA0_analog

- Tested from mid-July 2023 for front-end performance evaluation
- All features tested and are OK
- Nominal performance (noise, gain and timing) except noise at lowest gain, now understood and reproduced in simulation
- Corrections already implemented in present front-end design
- Tests finished, further tests with radiation and temperature will be done on SALSA1

SALSA0_digital

- Tested from end of November 2023 to evaluate ADC block performance
- Resolution OK but max sampling rate too low, fixed in present version
- Problem of offset of the digital 0 still not understood in simulation, study ongoing
- Some issues with bonding in packages → packaging of 10 more ongoing, expected to be delivered soon

PRISME PLL prototype

- Evaluation of the newly developed 65nm PLL block
- Packaged chips delivered mid-December
- Test cards equipped with chips expected these days

STATUS OF SALSA1 DEVELOPMENT

Purpose and architecture

- Performance evaluation of front-end + ADC chain, + tests of different blocks
- 4 front-end channels + 2 direct inputs to ADC
- 12-bits parallel output with static multiplexer, with possible dynamic mux of 4 1st channels
- Integrate PRISME PLL + some blocks from PRISME proto (including CERN ones)

Schedule

- Submission to TSMC foreseen April 17th
- → schematics frozen March 1st, tight time line !

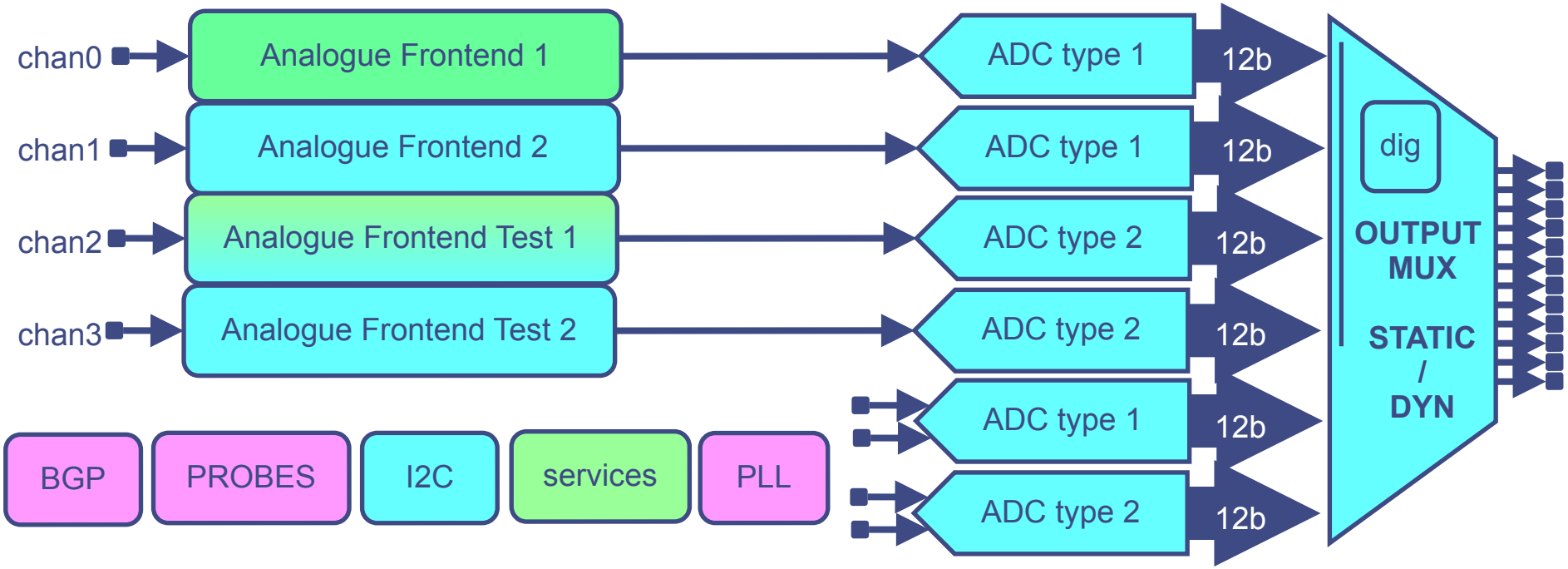
Front-end

- 2 kinds of front-end
  - SALSA0_analog one with corrections
  - New version of front-end with improved pole-zero cancellation
- 2 front-end blocks (one per kind) with debug outputs

ADCs

- ADC 1: updated Sao Paulo ADC with faster sampling rate, up to 50 MS/s. Impact of sampling clock duty cycle on conversion speed observed, addressed in the updated design
- New simulation environment, with large speed improvement → larger test coverage
- ADC 2: development of a new ADC at IRFU for DRD7 started one year ago, aiming low power consumption and high speed
- Adaptation ongoing to SALSA requirements (12 bits) as backup, to be included in SALSA1

SALSA1 ARCHITECTURE



From PRISME

Layout done

Layout in progress

STATUS OF SALSA2 DEVELOPMENT

Purpose and architecture

- Like final SALSA but with reduced number of channels - 32 ?
- Implement full chip architecture including DSP and input/output interfaces in a version close to the final one
- Expected to be submitted first trimester 2025

DSP

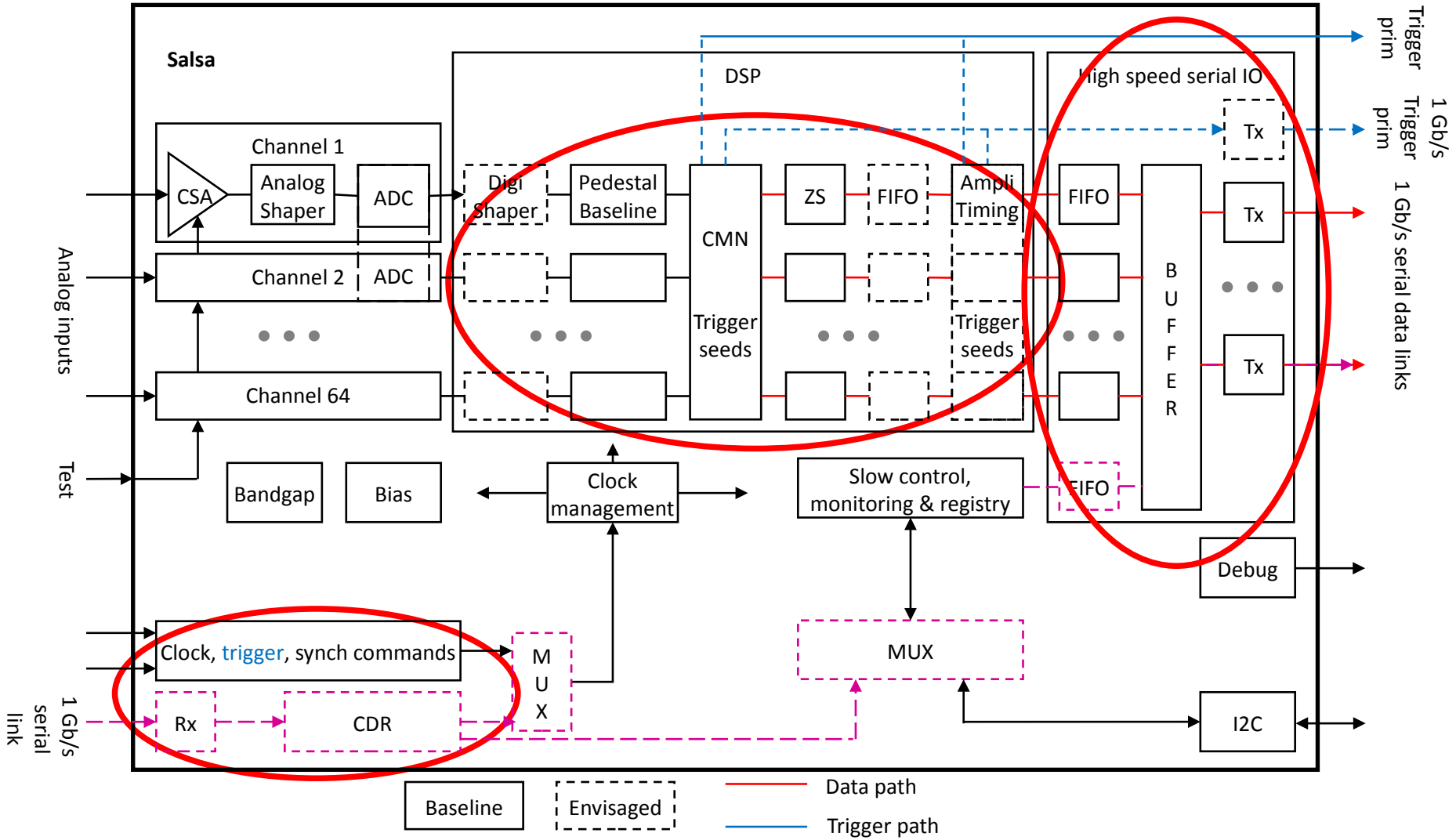
- First draft of data processing established and presented last week (EPIC DAQ WG)
- Draft list of processes: baseline correction, common mode correction, digital filtering, zero suppression, feature extraction, trigger management, generation of calibration data, data formatting
- Data format still in discussion

Input interface

- Unified interface proposed, combining clock + synchronous commands + slow-control in one diff line, under study
- Would simplify connection and ASIC integration in DAQ system
- Also synchronization of chip with EIC/EPIC time structure, connection with DAQ commands, etc... under discussion with EPIC DAQ community

PRELIMINARY CHIP ARCHITECTURE

DSP, input and output interfaces discussed today



MILESTONES AND NEXT STEPS

eRD109 FY23 milestones

- Specifications of SALSA1 design → done
- Production of SALSA1 prototypes → submission expected April 17th
- Packaging and test card production → expected Autumn 2024
- Performance evaluation → expected end of 2024 / beginning of 2025

Milestones of generic R&D program for EIC (new 65nm PLL block)

- PRISME prototype submission → done July 19th 2023
- Packaging (done) and test card production in progress → expected very soon from assembly company
- Radiation tests → Summer 2024 ?

eRD109 FY24 milestones (proposal)

- SALSA2 specifications → July 2024
- SALSA2 submission → March 2025
- Beginning of SALSA2 tests → September 2025

Very next steps

- Beginning of tests on PRISME prototypes → next weeks
- SALSA1 submission → April 17th
- SALSA2 specifications