Status of the eRD109 “RDO/Timing/Service Hybrid”

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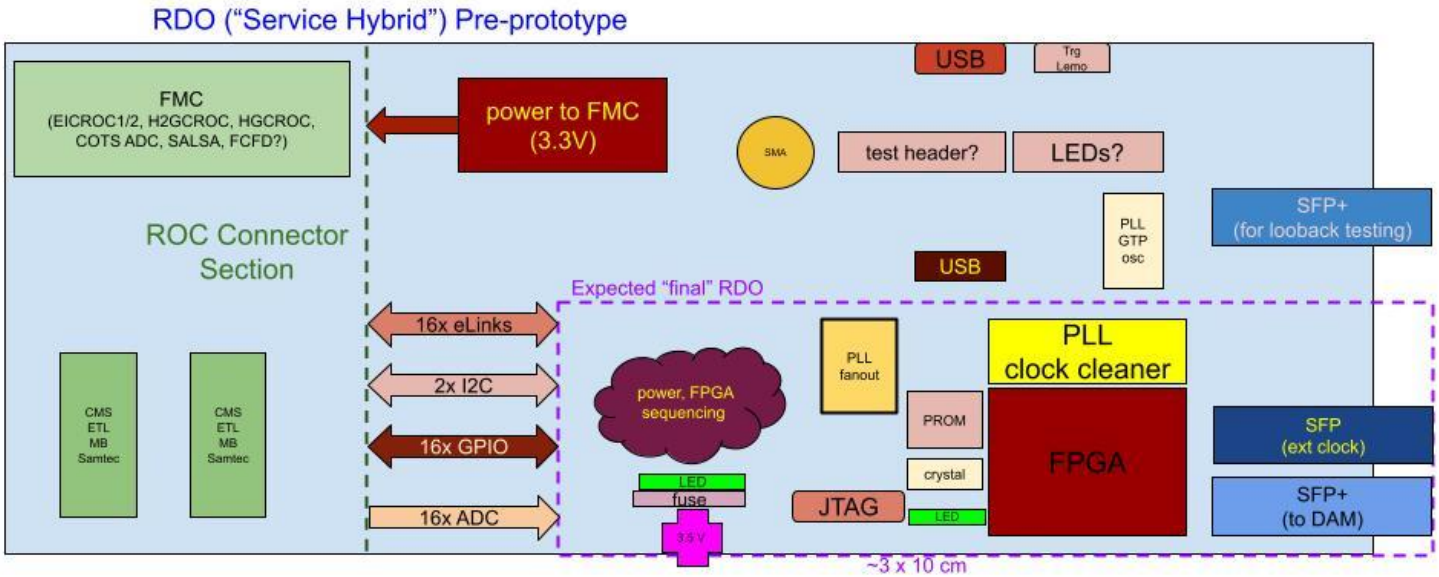
The Pre-Prototype RDO (“ppRDO”)

- General Design ✔ – 100% complete



ppRDO Features

- Artix+ FPGA AU15P & associated PROM
- Fiber SFP+ interface to DAM ala CERN TClink (Timing “Option A”)
  - with Clock Cleaner Si5345
- Fiber SFP+ interface for direct clock evaluation (Timing “Option B”)
  - Si5338 as the on-board clock source for local testing
  - and Clock Cleaner Si5345
- Fiber SFP+ interface for auxiliary fiber/loopback testing
- FMC connector with generalized pinouts (close to final) to support future ASIC integration
  - supports 8 “typical” ASICs: 8 clocks, 8 FCMD, 16 DAQ, 8 differential GPIO, 4 I2C buses, etc
    - modelled according to the HRPPD FMC pinouts
  - clocks are fanned out to the ASICs with very-low jitter Si53302 fanout chip
- Connectors to the CMS ETL ETROC daughtercard
  - NOTE: ETROC is our stand-in for future EICROC and other ASICs because it already exists
- Components carefully chosen from the CERN list of rad-hard(ish) chips
- Current measurement possible on all regulators

Status

- Board Design ✔ – 100% complete
- Board Schematics ✔ – 90% complete (expected complete by 2/15)
  - FMC pinout (proposed) will be sent out to all interested parties “soon”
- Firmware
  - “0th” firmware (to test basic features, clocks and blink an LED) ✔ — 90% complete
- Next steps
  - purchase long-lead items (e.g. FPGAs) ⇒ now – need funding
  - board layout
    - general parts placement ✔ – 50% complete
    - PCB design – TBD (will be done by an outside vendor)
  - continue with firmware for reading/controlling ETROC, timing, fiber protocols, I2C, …
    - for other ASICs (e.g. HGCROC) I would need help and example VHDL code