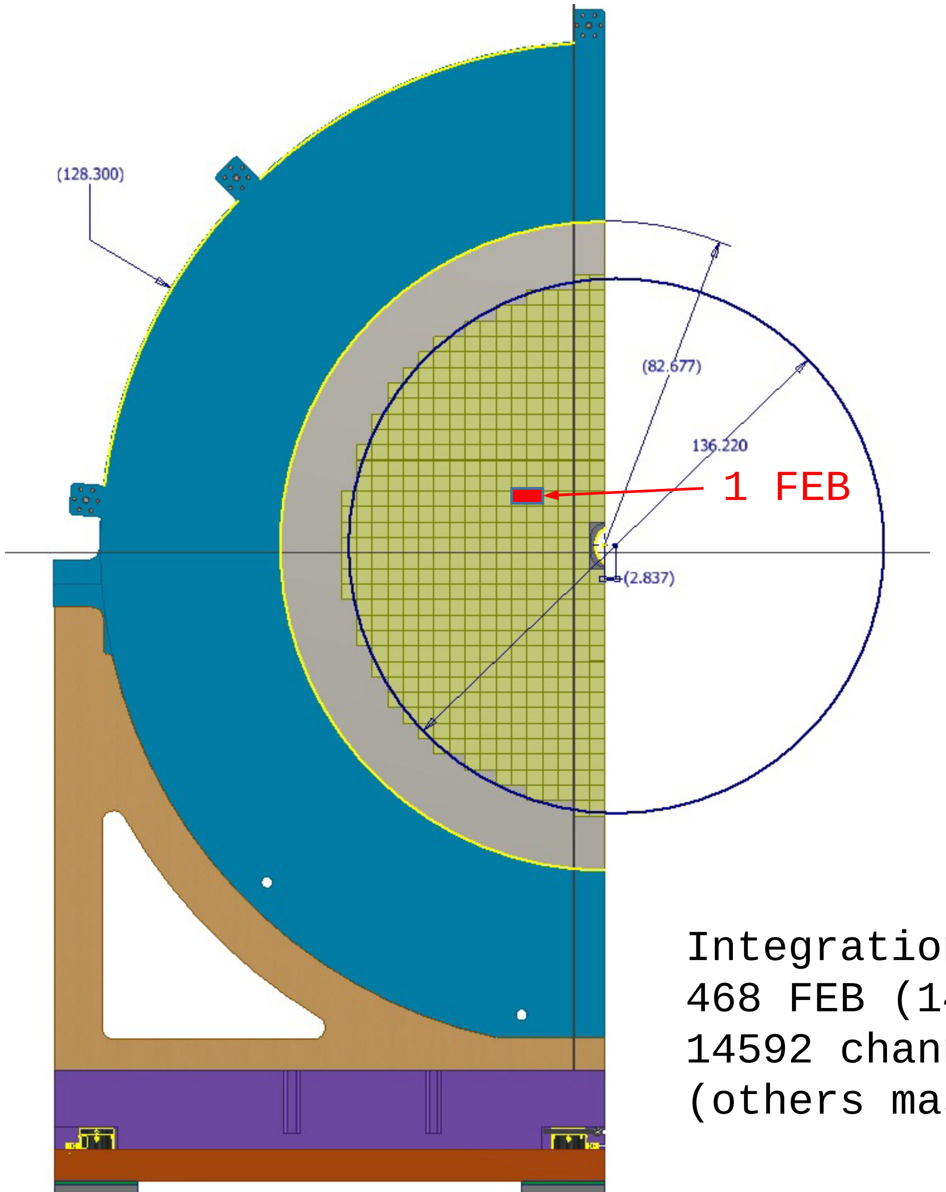


Update on forward ECAL readout

- Bench tests with SiPM's and preamp
- Digitization resolution study

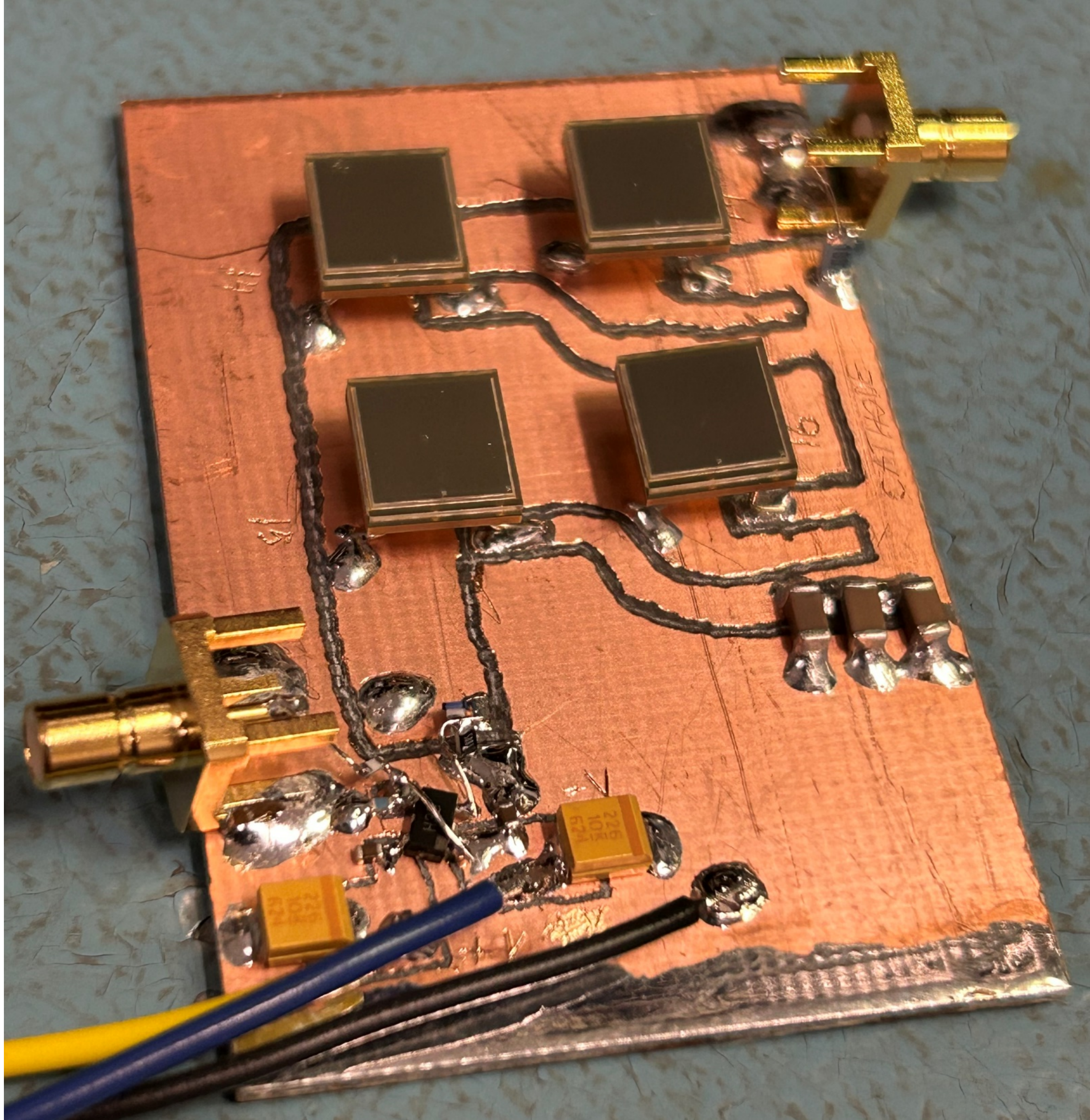
Integration view:
468 FEB (14976 channels)
14592 channels really used
(others masked)

G. Visser
Indiana University
2/7/24 Calo. Meeting

1 channel pre-prototype

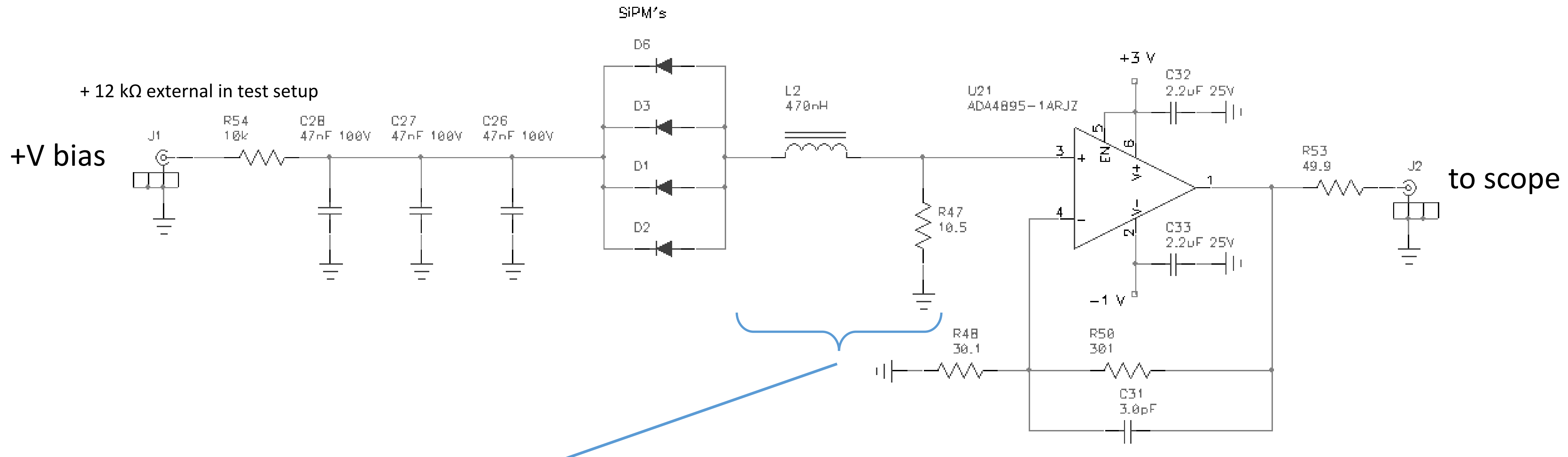
4× S14160-6015PS (matched in Vbr) in simple parallel connection

spacing as in fwd ECAL (12.5 mm)

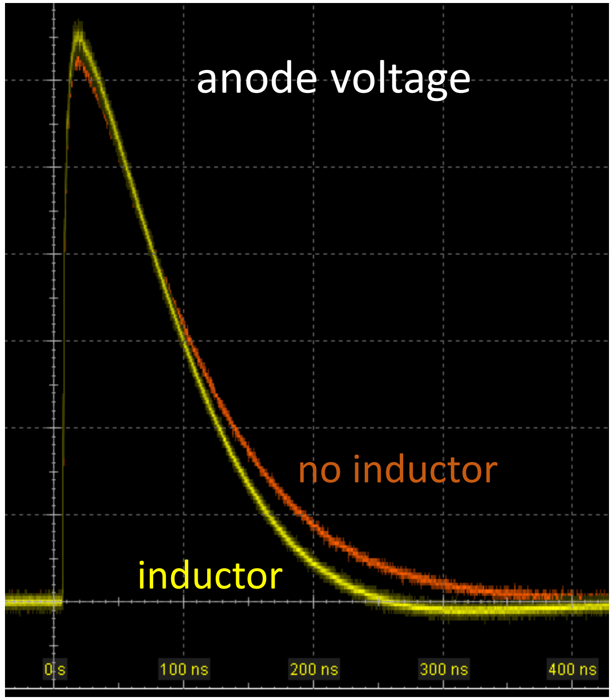


For the real boards

- Capacitors, thermistor will be on SiPM board
- Preamp TBD – on SiPM board will be much less risk of noise pickup, and better use of limited board space, but preamp reliability must be perfect and heating SiPM's is not helpful
- 2nd shaping and gain stage and ADC on FEB
- LED and LED driver on SiPM board, not included in this prototype



SiPM load impedance: 470 nH + 10.5 Ω (inductor is used for shaping and at the same time for faster recovery of SiPM gain)



signal tapped from the 10.5 Ω resistor, fed into ADA4895 preamp, DC coupled, voltage gain 11.0

the shaping configuration is novel, but the ADA4895 chip was used similarly for SiPM preamp in STAR FCS and seems happy with *that* radiation environment (it is also the lowest (noise × power) chip on the market)

preamp power 12 mW (@ −1 V & +3.3 V supplies)

- *for now, the SiPM's are operated at Hamamatsu recommended V_{OV}*
- studies will be needed with radiation damaged SiPM's to see if operating at reduced V_{OV} can improve S/N ratio – *if irradiated DCR grows more slowly with V_{OV} than PDE does*
  - this was the experience from older SiPM's (STAR FMS preshower)
  - lower V_{OV} makes stable bias, correct temperature compensation, and SiPM matching more critical
  - results on following pages show we could, if necessary, operate with gain reduced by factor of about 2 without seeing electronics noise dominate
- these 4 particular SiPM's per Hamamatsu test sheet (V_{OV} = 4.0 V, gain 3.6×10^5):
  - #14, Vop = 42.23 V, Idark = 0.35 μA
  - #15, Vop = 42.12 V, Idark = 0.33 μA
  - #16, Vop = 42.11 V, Idark = 0.36 μA
  - #19, Vop = 42.19 V, Idark = 0.36 μA
- measured dark current 1.45 μA (see next slide), good agreement with sum of the above (1.40 μA)
- note, DCR is about 26 MHz (for these 4 SiPM together)
  - spec is typ. 3 MHz, max 10 MHz per device

~13 pixel LED signal

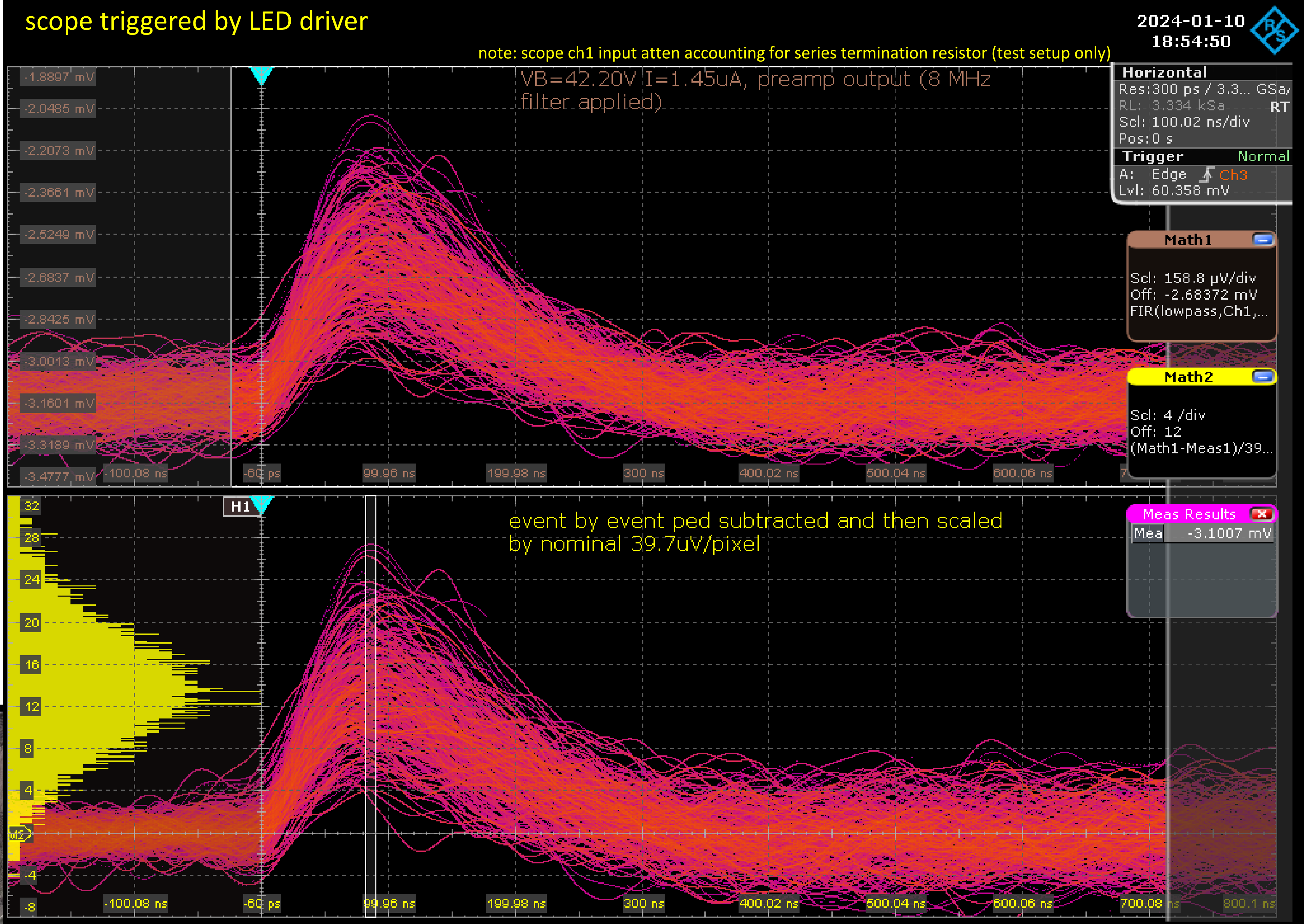
that is ~9 MeV (at projected light yield)

N.B. threshold goal 15 MeV

Looks “OK” (here w/o radiation damage). But you can see it will not be a sharp threshold.

Peaking time ~85 ns

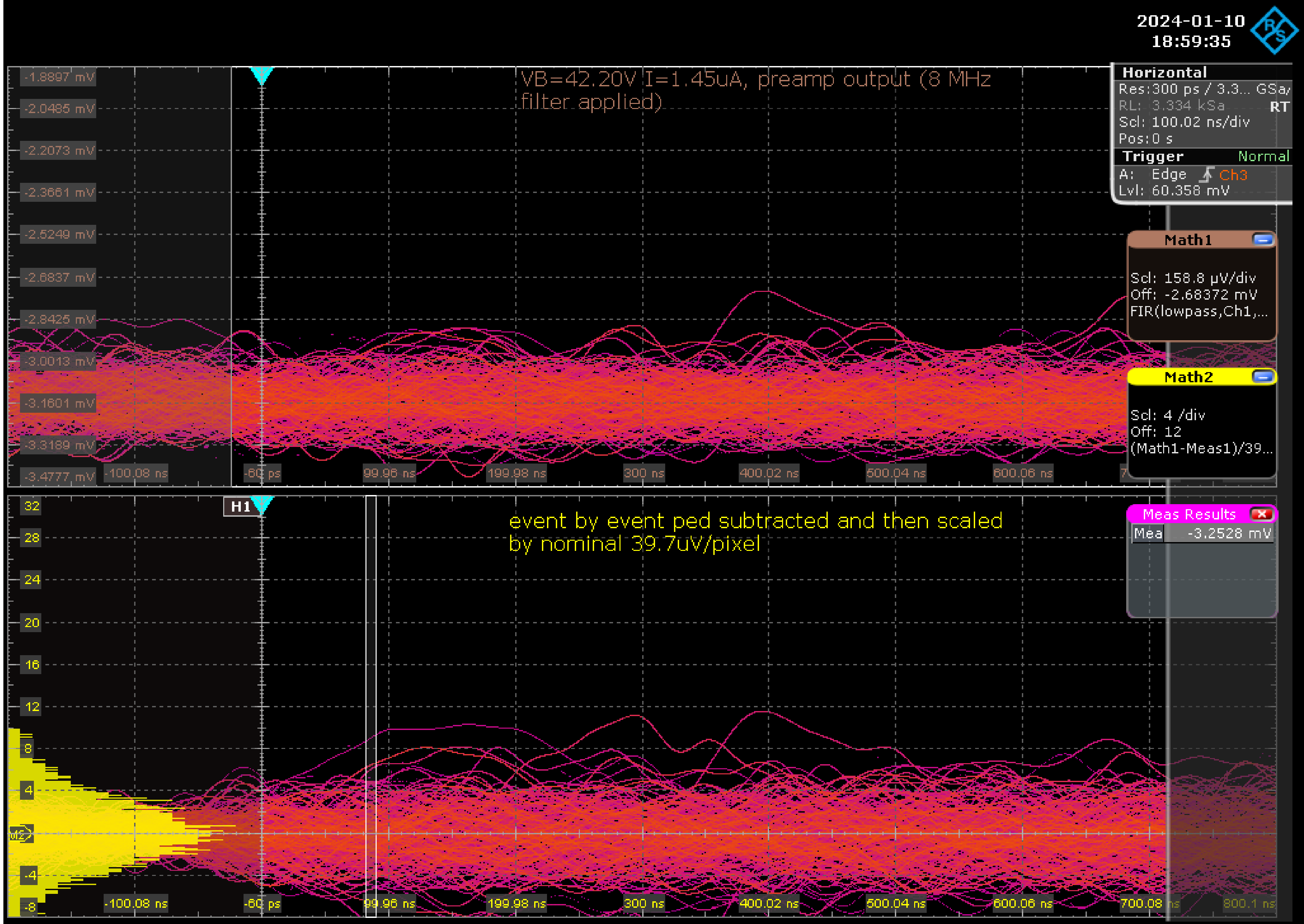
N.B. also -- time resolution of pulses that are just at threshold will be poor (50 ns maybe?)



bias PS V set to account for 22kΩ series resistance in fixture

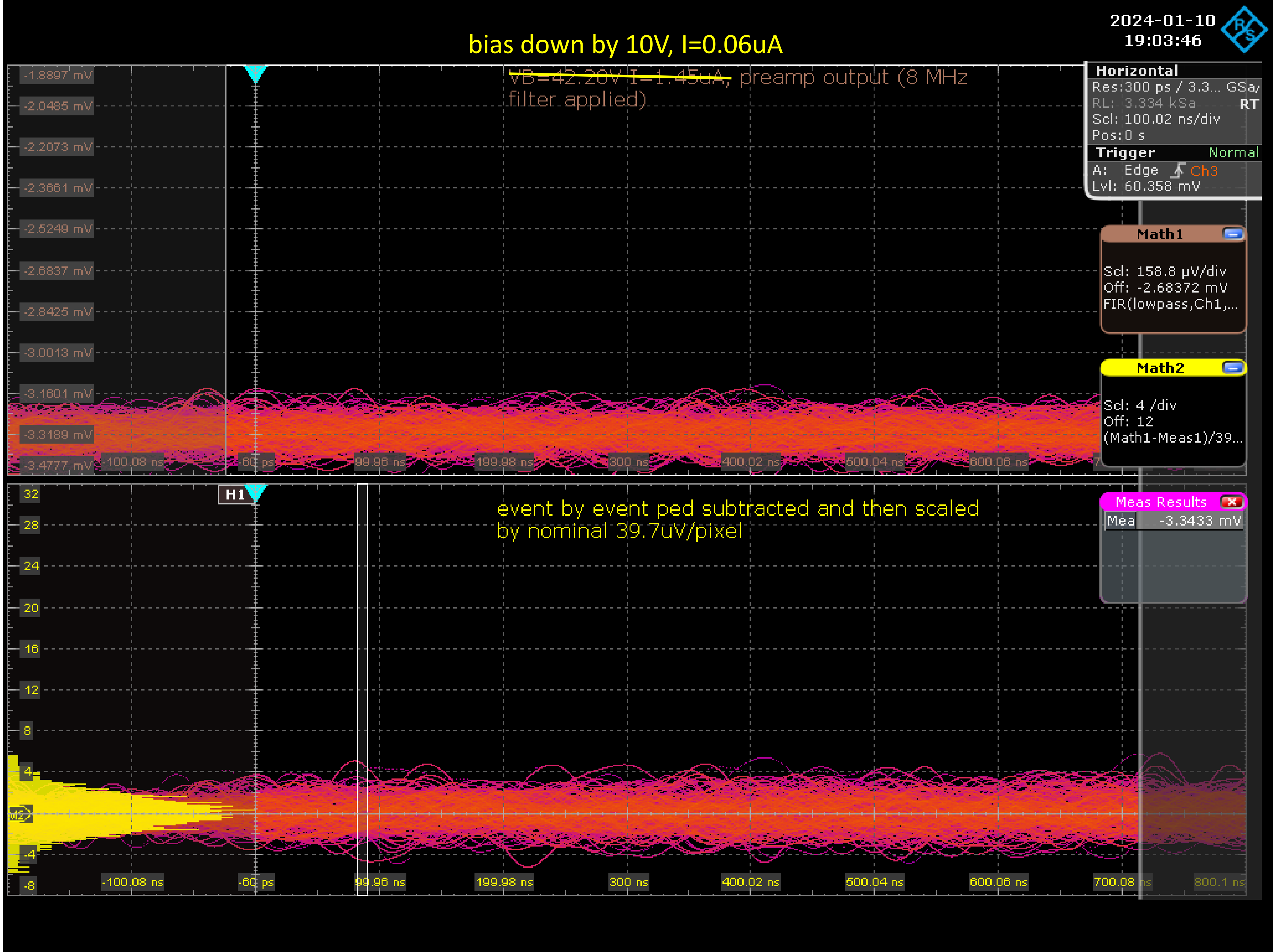
LED off

(Dark noise + electronics noise)



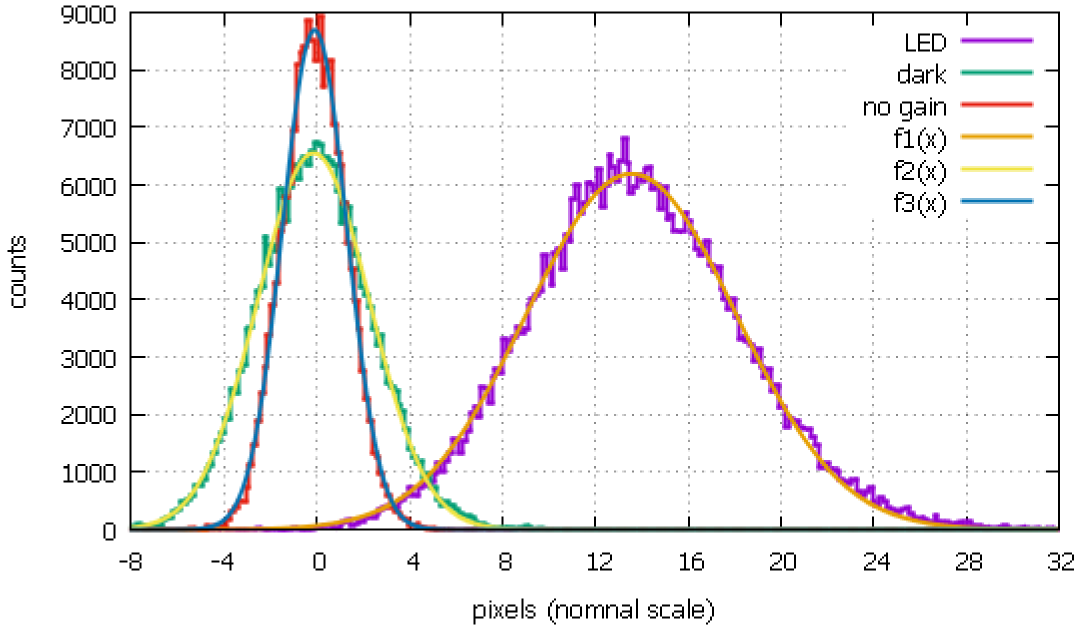
LED off, bias 10V down

(→Electronics noise only)



Summarizing those

	mean	sigma
no gain	-0.09	1.39
dark	-0.14	2.42
LED	13.56	4.51



If we 'remove' the dark noise from LED spectrum, remaining noise is sqrt(4.51^2-2.42^2) = 3.80.
And of course from Poisson statistics we expect sqrt(13.56) = 3.68.

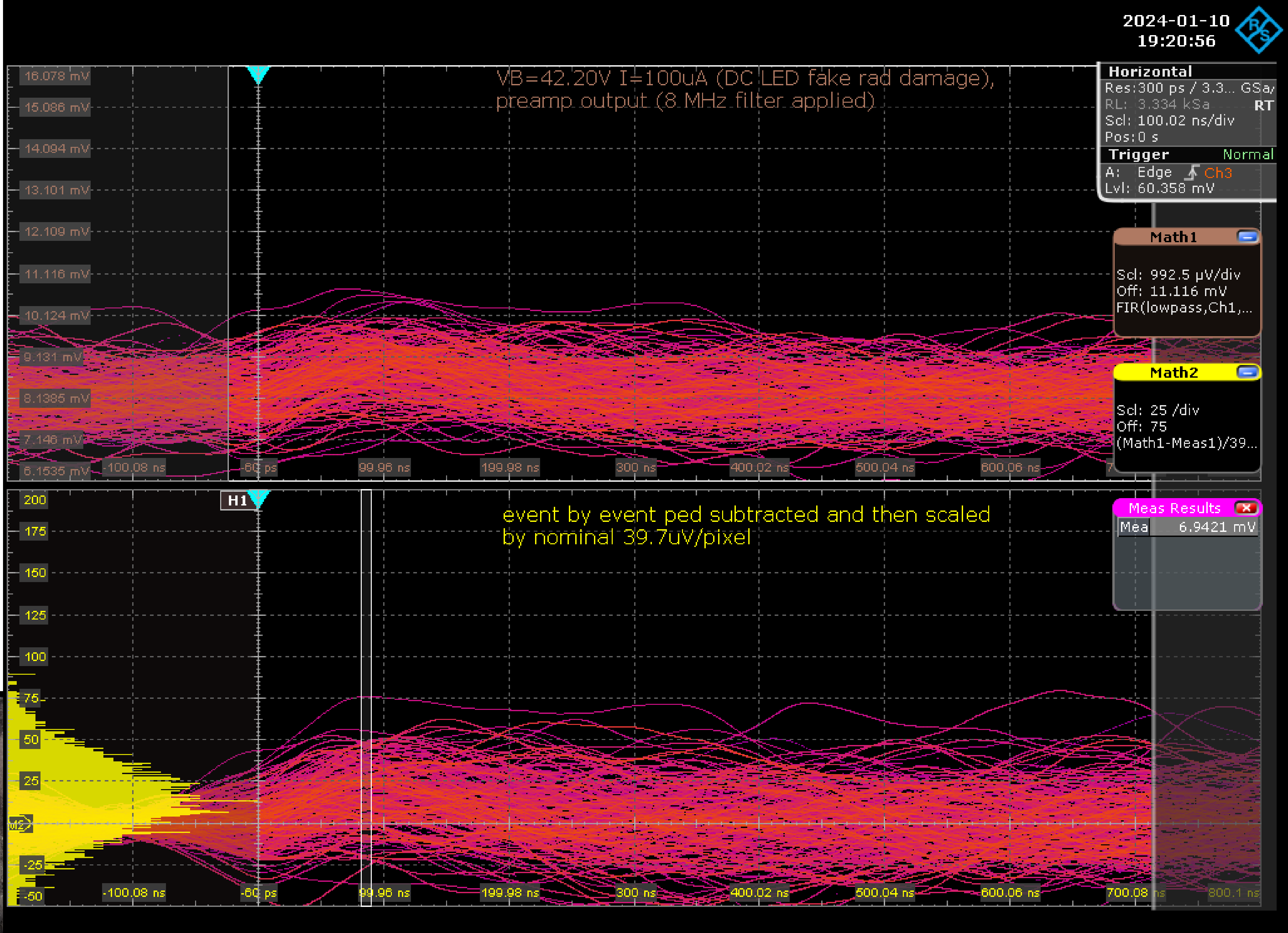
Looks very reasonable.
We do expect some extra noise beyond Poisson statistics, due to gain matching between the four SiPM's. But that should be a small effect.
Of course also the LED pulser may have a little instability/noise.

Fake radiation damage applied. (DC LED illumination to get “dark” current 100 µA).

Same SiPM bias voltage

Same ~13 pixel ~9 MeV LED pulse signal. (DC & pulse are two separate LED’s)

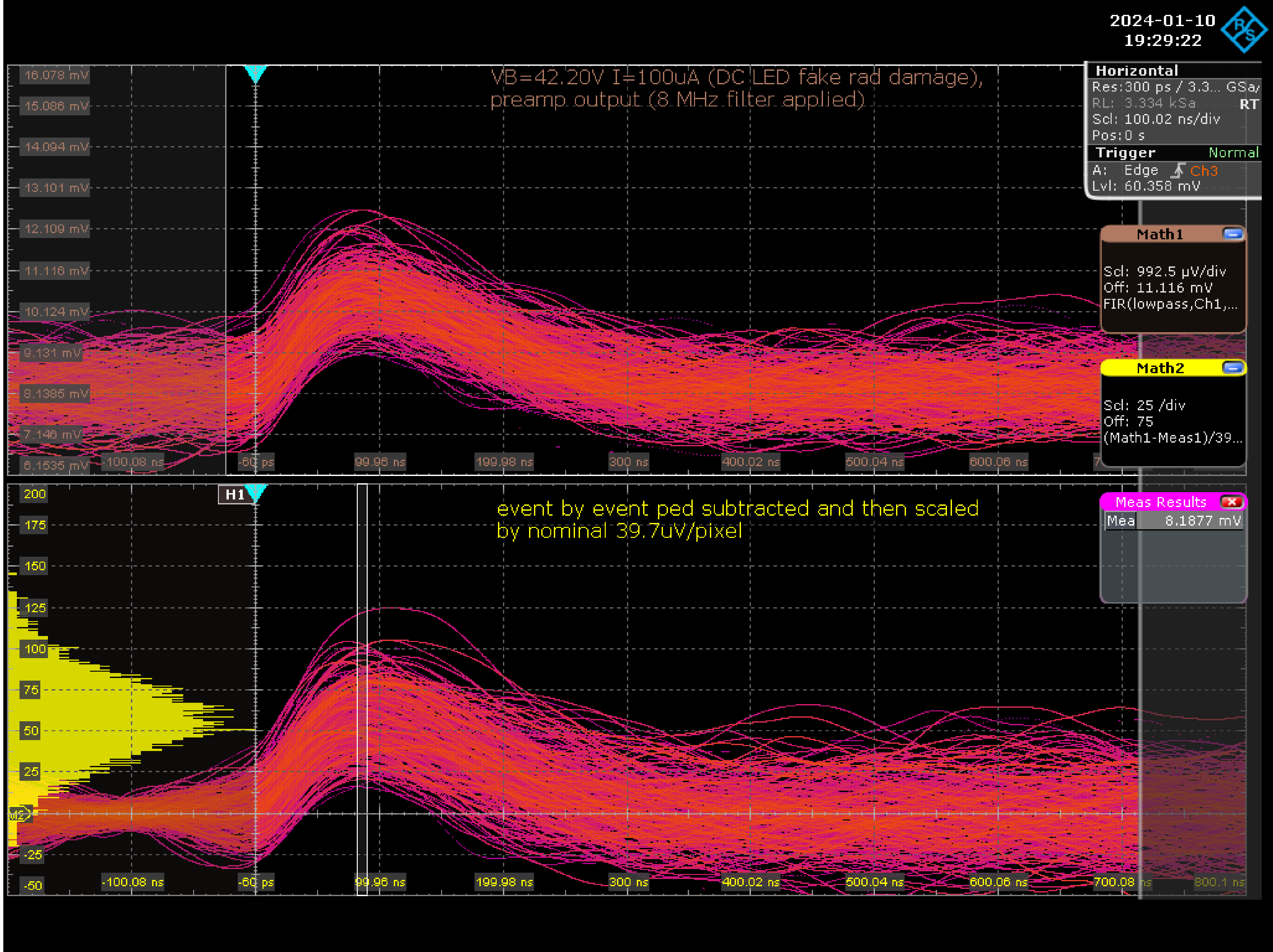
Note Y scale changed →



bias PS V set to account for 22kΩ series resistance in fixture

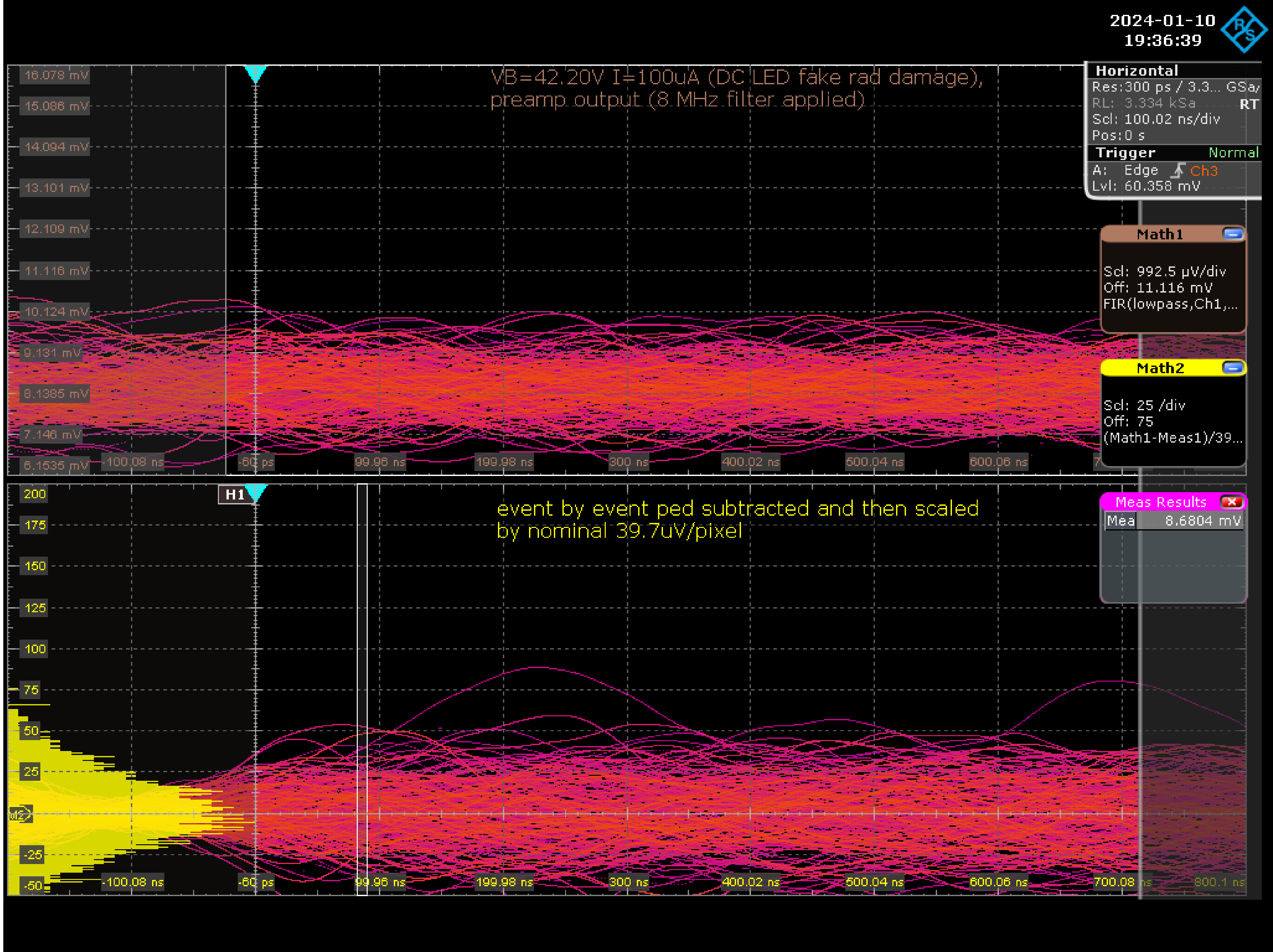
100uA fake rad damage
(as before)

Bigger ~57 pixel (~38 MeV)
LED signal



100uA fake rad damage (as before)

LED (pulse) off

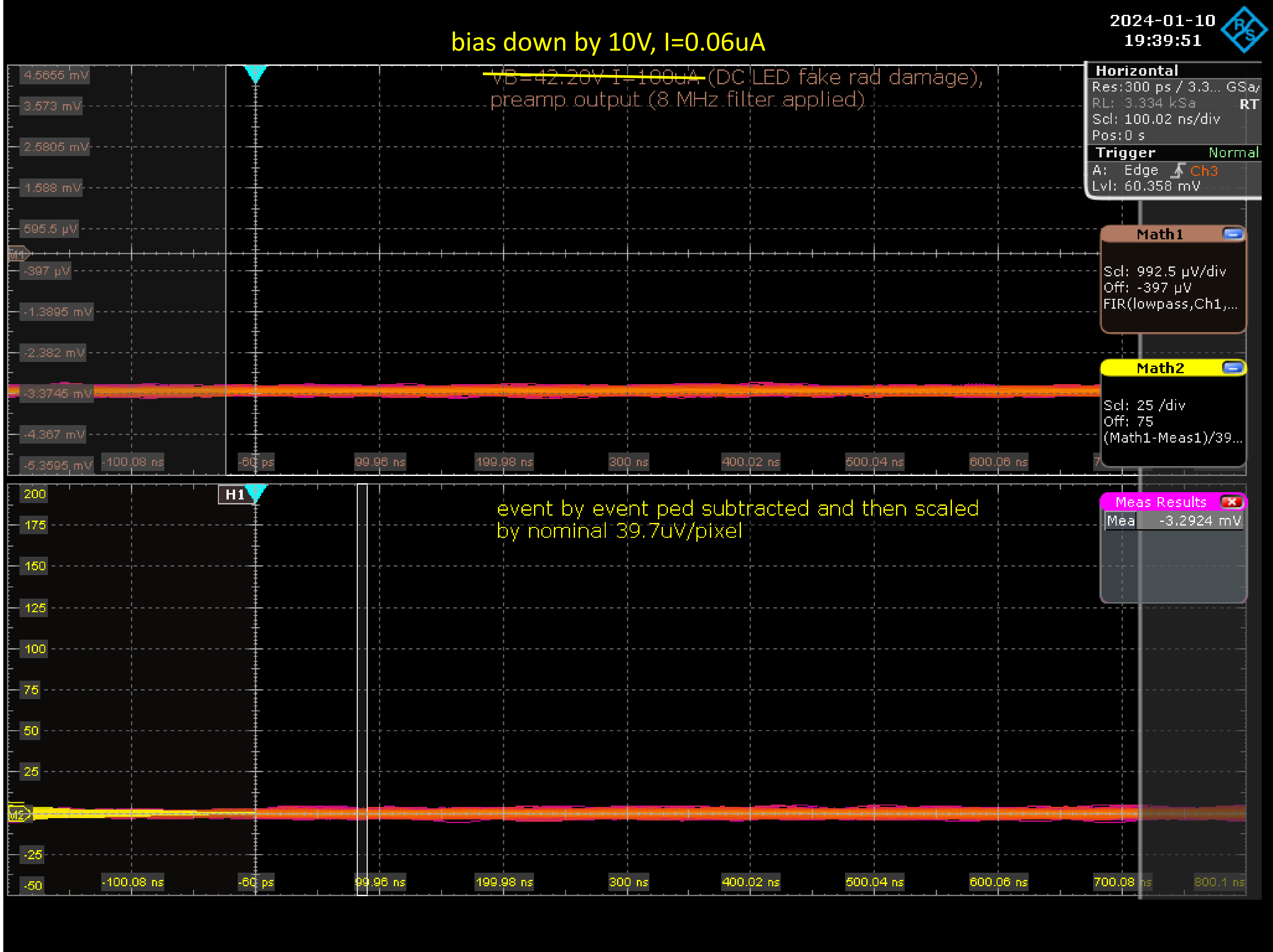


Bias 10 V down, no SiPM gain

DC LED same as it was

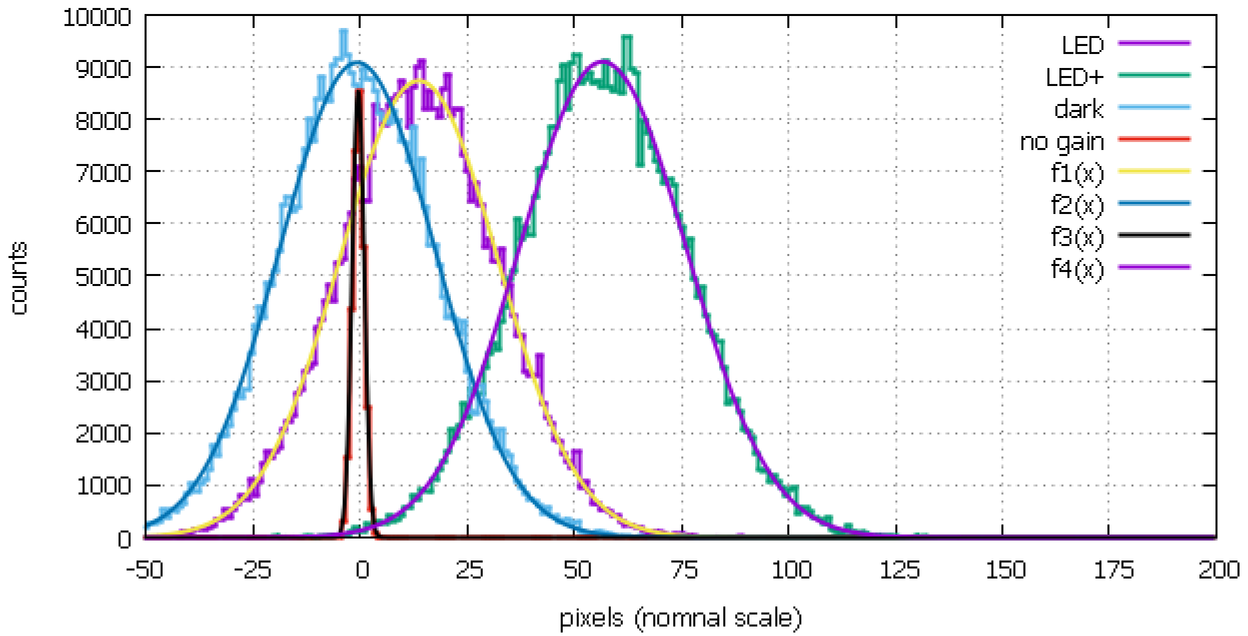
LED pulse still off

(electronics noise only)



Summarizing those

	Idark = 1.45 uA		Idark = 100 uA	
	mean	sigma	mean	sigma
no gain	-0.09	1.39	-0.49	1.42
dark	-0.14	2.42	-0.71	18.17
LED	13.56	4.51	13.66	18.55
LED+			56.63	19.51



If we 'remove' the dark noise from LED+ spectrum, remaining noise is sqrt(19.51^2-18.17^2) = 7.09.
And of course from Poisson statistics we expect sqrt(56.63) = 7.53.

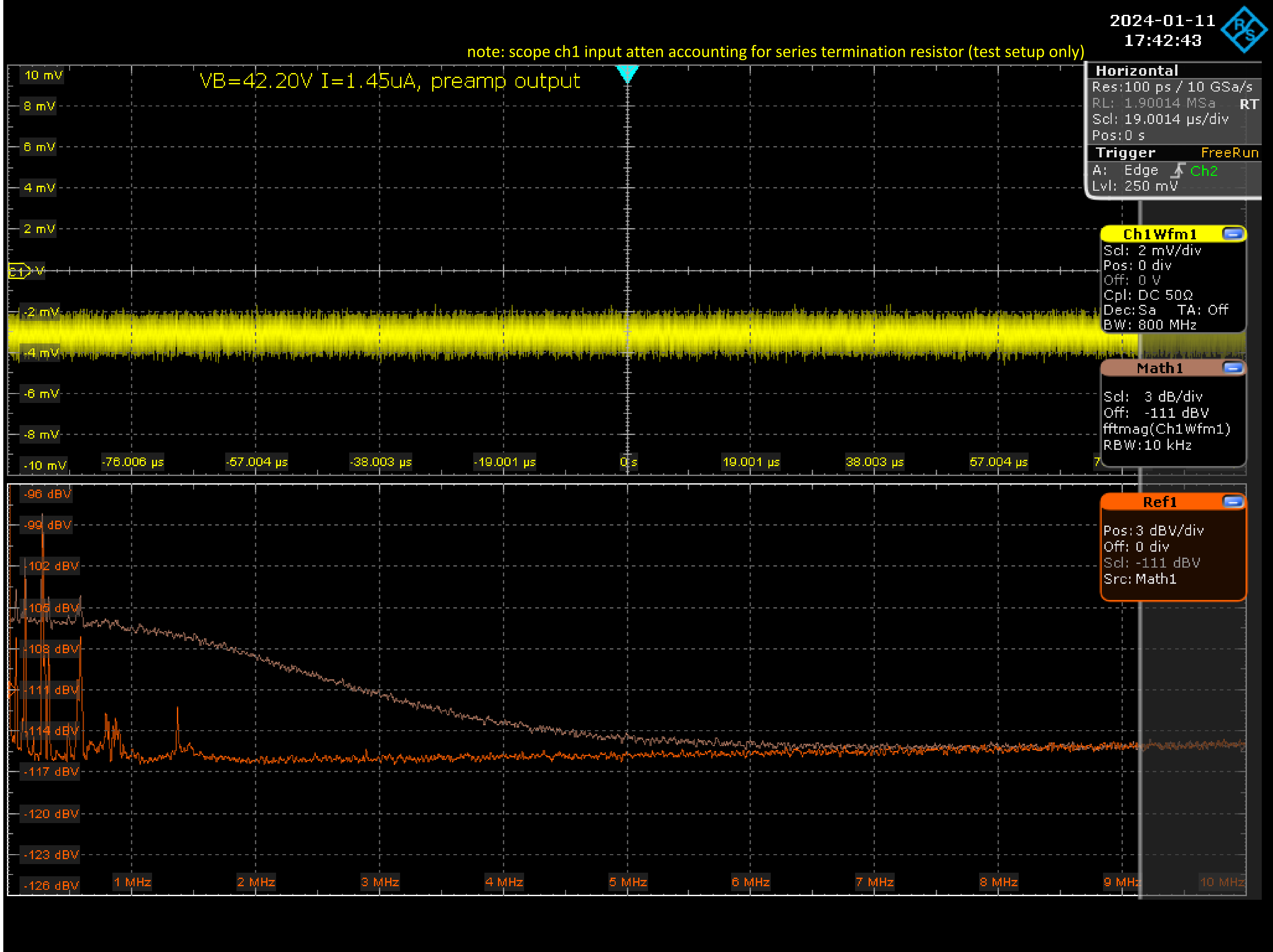
Again, looks very reasonable.

The gain for the smaller LED signal is evidently same as before, correctly.
Electronics noise same as before, of course, correctly.

All results look consistent, and consistent with gain expected from Hamamatsu spec and the test circuit characteristics.

dark noise analysis

magnitude, and frequency spectrum, of dark noise should correspond exactly to the dark current and SiPM gain…



dark noise analysis

magnitude, and frequency spectrum, of dark noise should correspond exactly to the dark current and SiPM gain… **it does →**

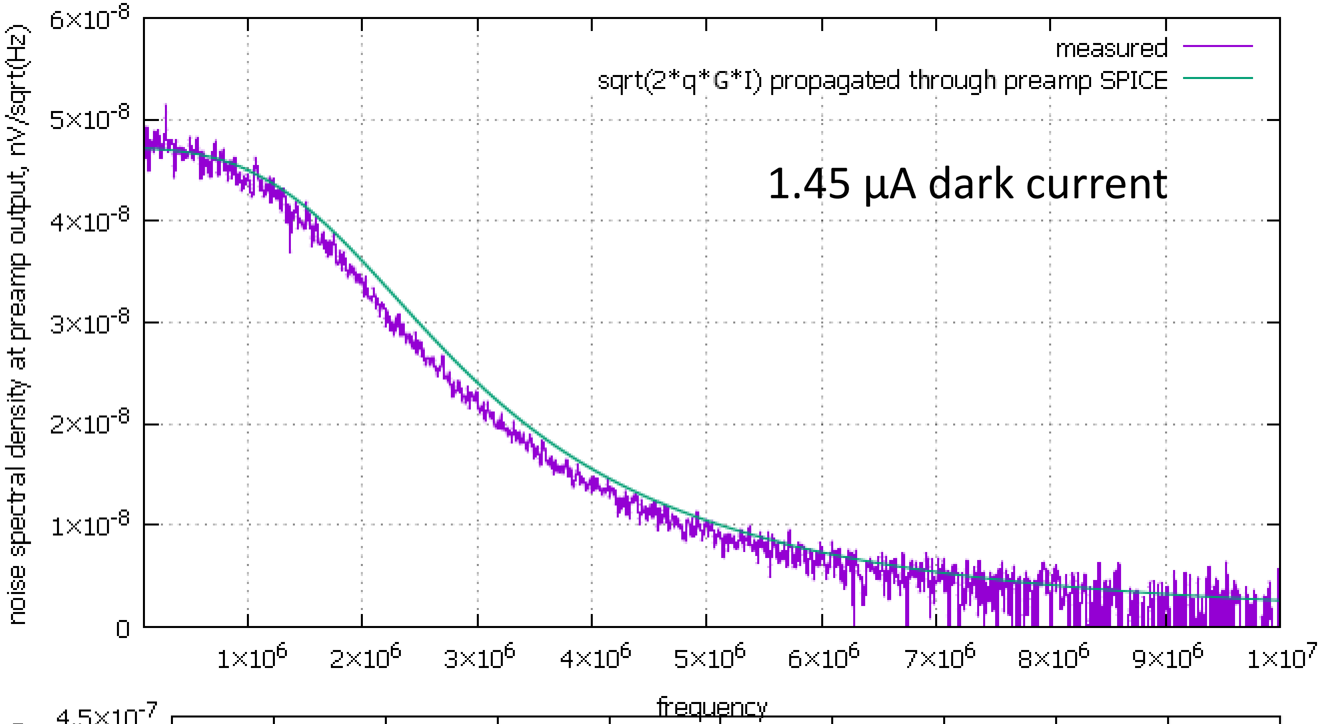
SiPM dark current noise is the same as any diode's shot noise. Except that the quanta of charge is not electron charge q but q G where G is the gain of the SiPM.

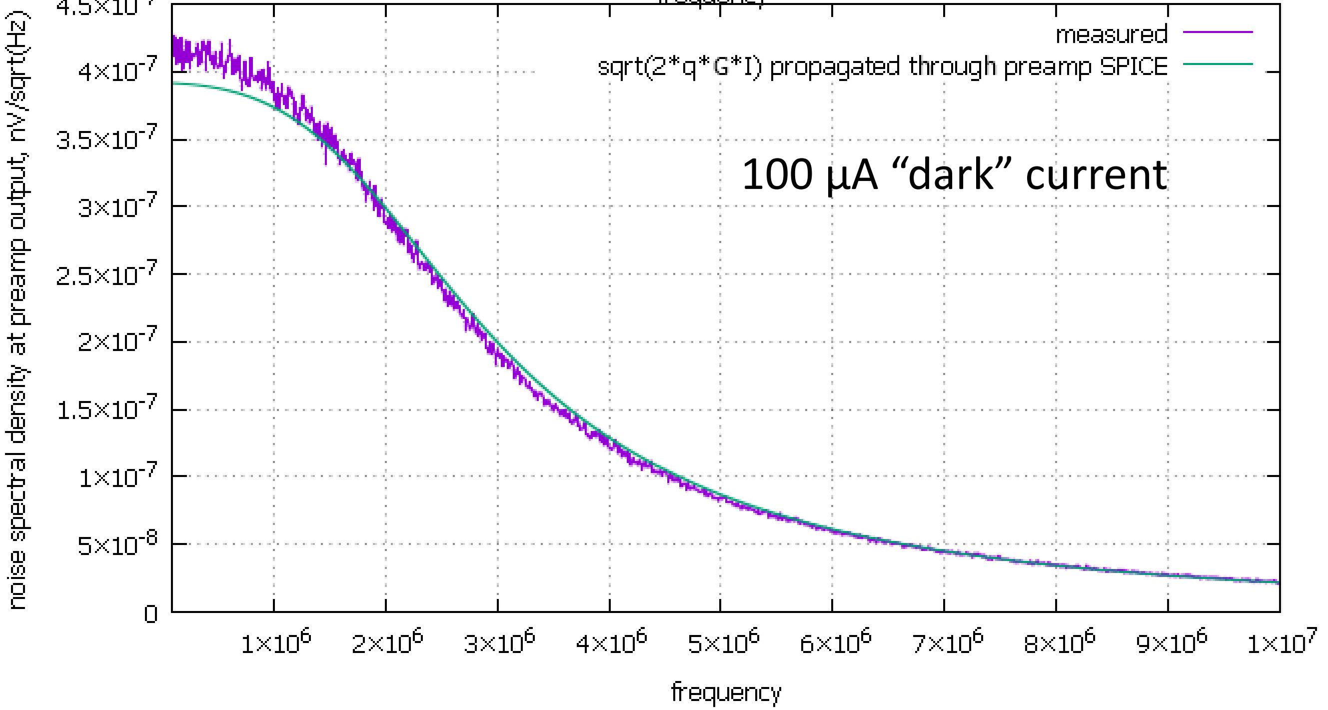
Current noise spectral density is

$$\sqrt{2\ q\ G\ I}$$

(A/sqrt(Hz))
where I is the dark current.

Note this also reconfirms G=3.6E5.

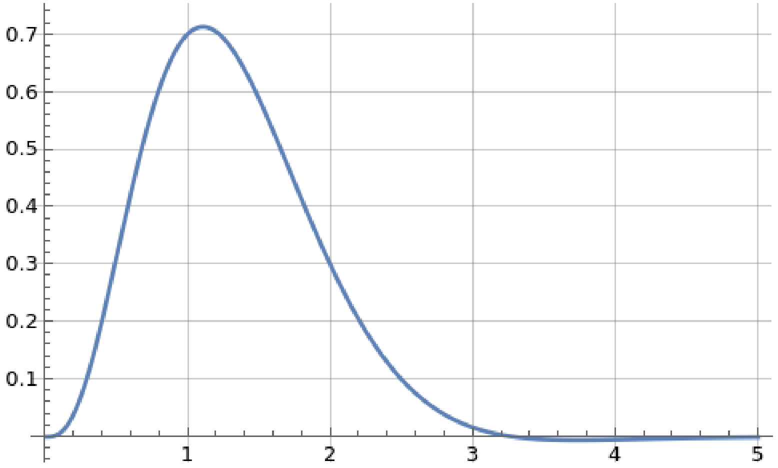




Peaking time study

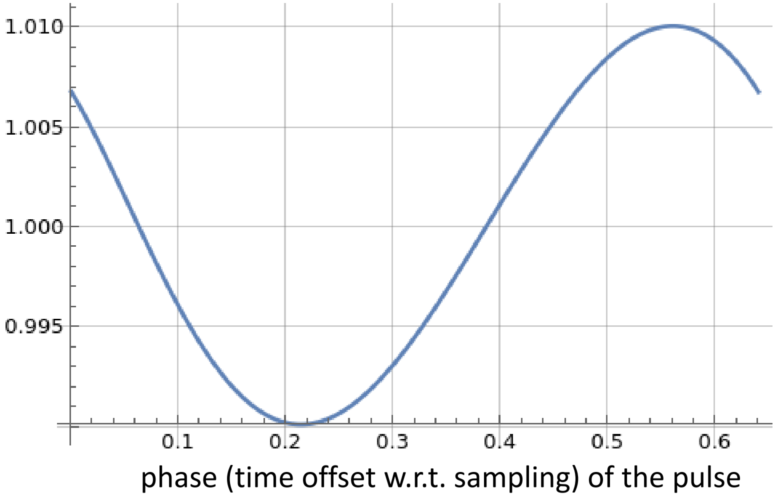
a typical pulse, with peaking time (defined as 1% to peak) = 1 time unit

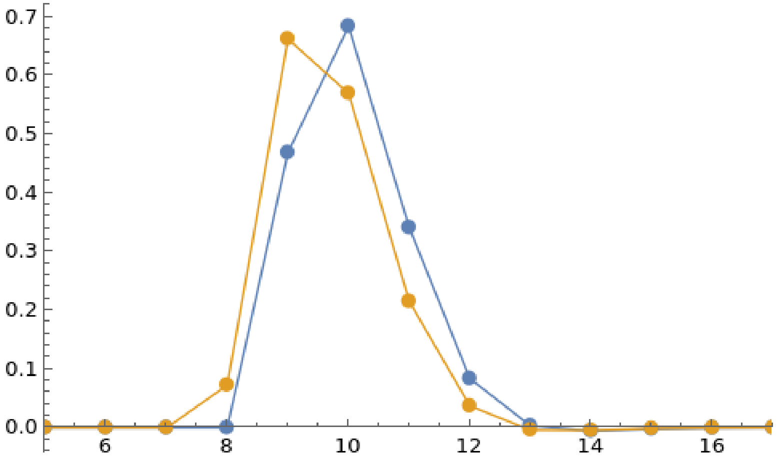
(4 pole shaper)



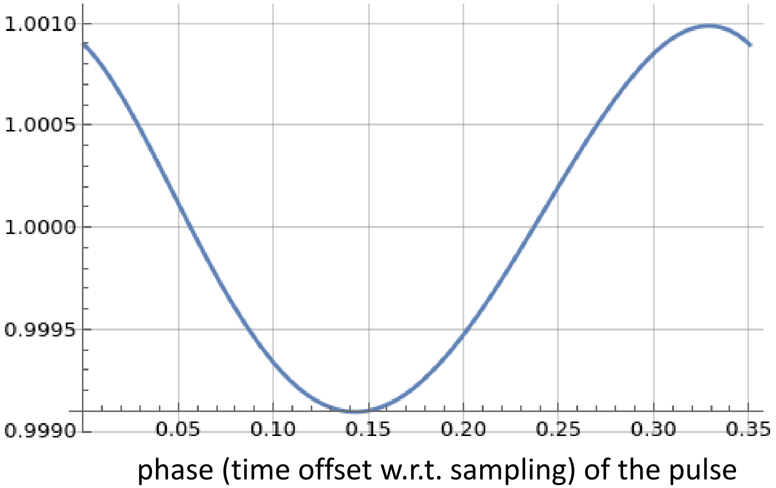
- shape used here is "typical" but of course the results at right depend on shape details – need to recheck later
- this result is about sampling only, not digitization (see next slide)
- assumption is that signal pulse is of constant shape, not quite true of course

sampling at $\leq 0.64 \times t_{peak}$ and summing gives a 1% measurement of the integral

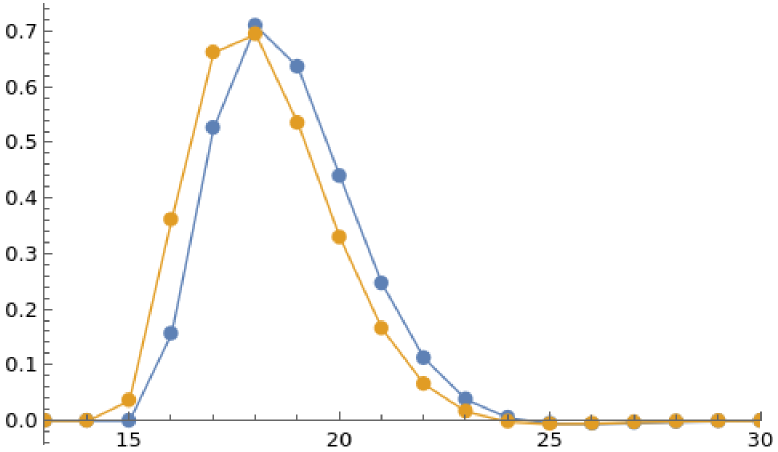




sampling at $\leq 0.35 \times t_{peak}$ and summing gives a 0.1% measurement of the integral



two example sampled pulses



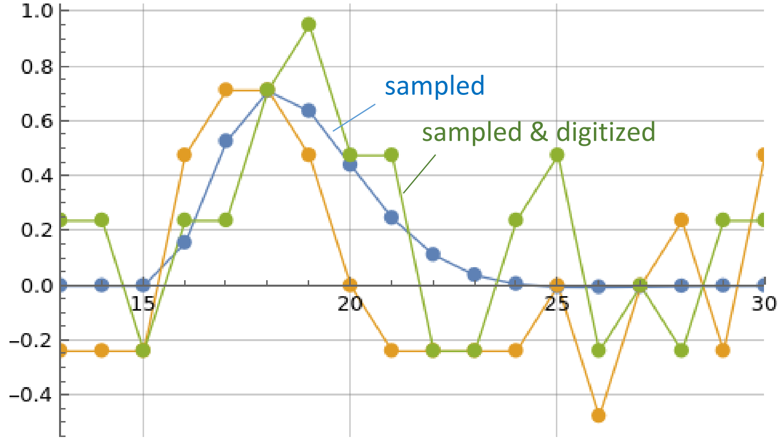
39.4 MSPS → $t_{peak} \geq 72.5$ ns

Bit resolution study – 14 bits, 100 GeV full scale

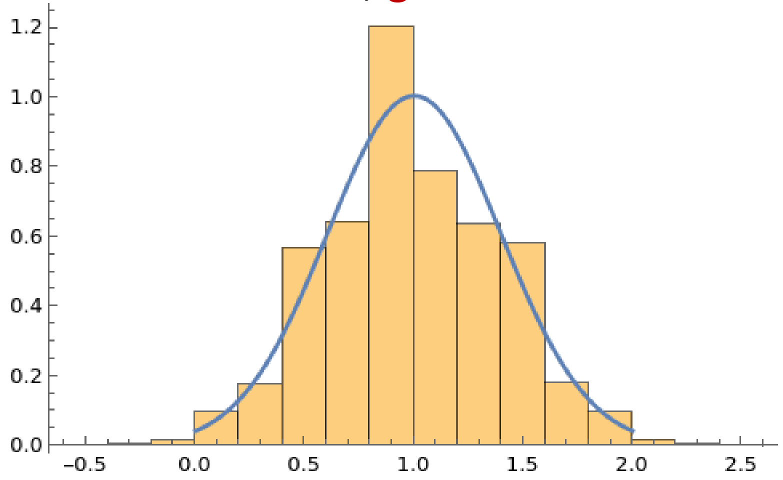
(100k events in each case)

Same pulse, sampling at 0.35 × t_{peak}, all phases considered (uniformly), now digitized w/ +/- 2.13 LSB [↔ datasheet 73.5 dB SNR] ADC noise added.
No dark noise added to signals here!

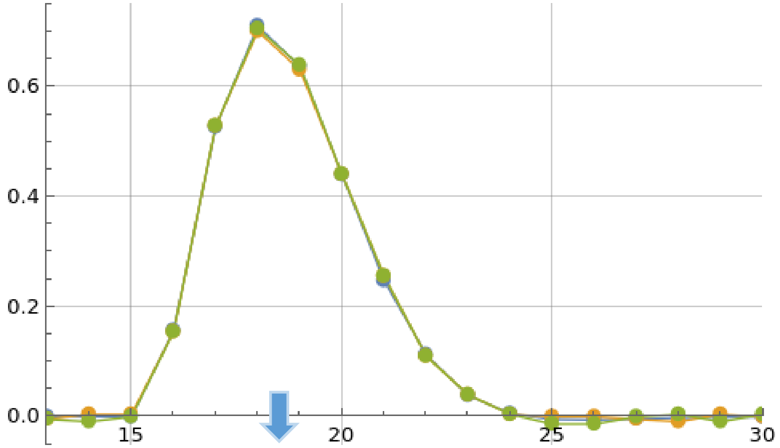
18.5 MeV (peak 3 ADC counts)



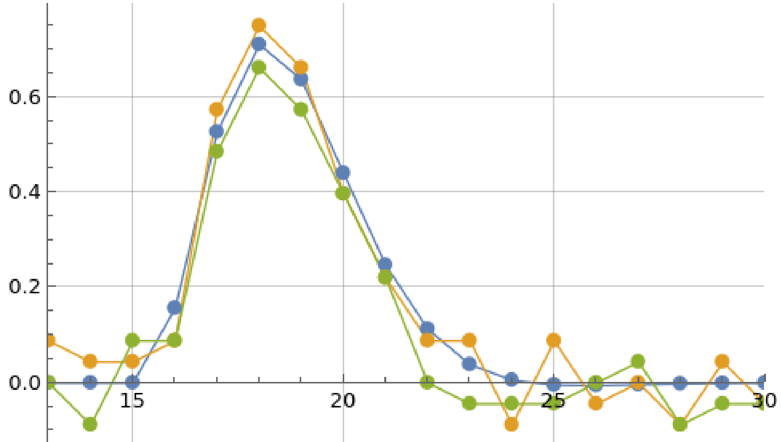
fit σ = 39.7 %, goal < 37%



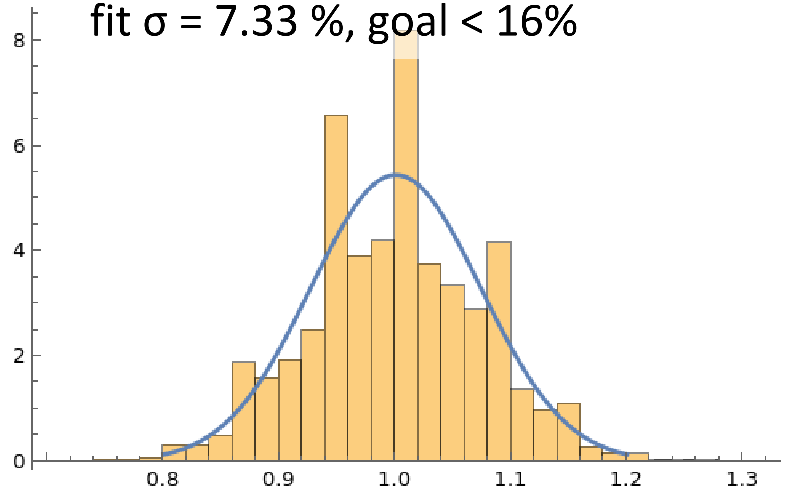
1 GeV (peak 162 ADC counts)



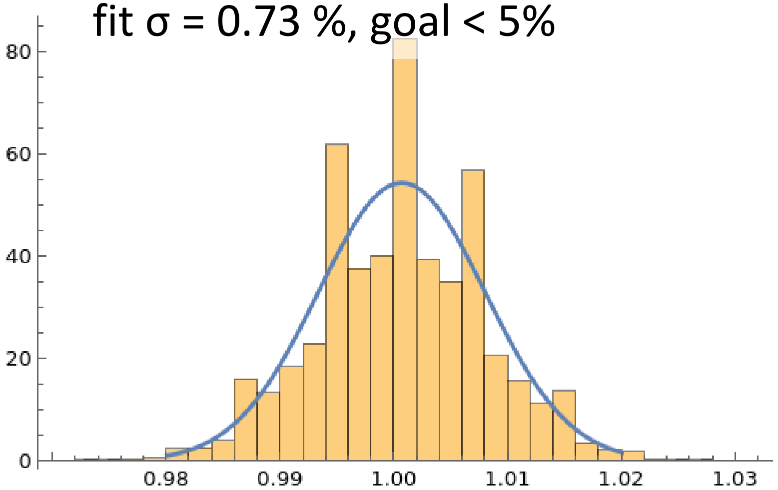
100 MeV (peak 16.2 ADC counts)



fit σ = 7.33 %, goal < 16%



fit σ = 0.73 %, goal < 5%



summing from samples 14 to 27

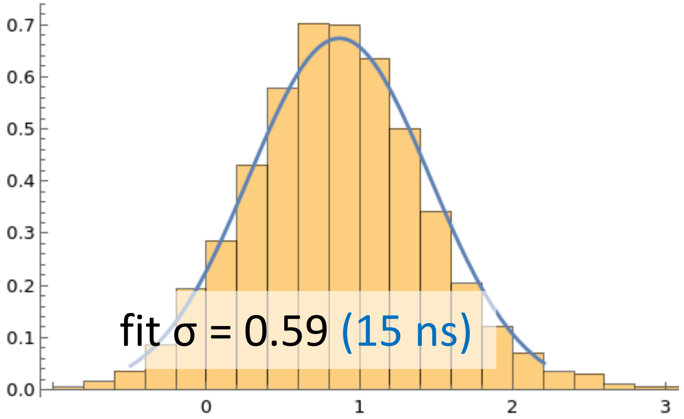
in each case noise is as expected: $\sqrt{14}\,\frac{4.26}{\sqrt{12}}$ ADC units in sum

Bit resolution study – 14 bits, 100 GeV full scale – **time resolution**

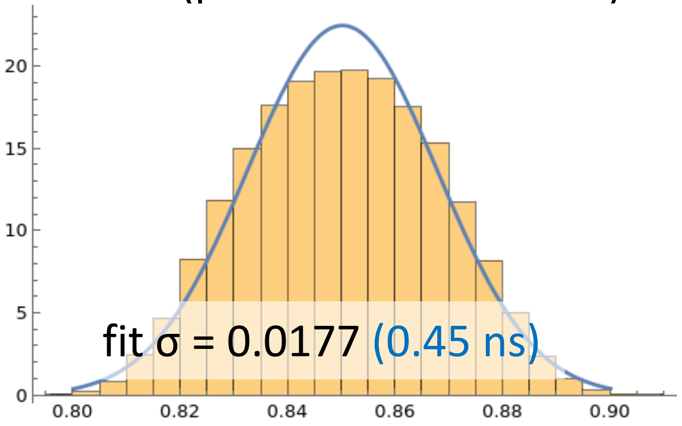
(20k events in each case)

Same pulse, same sampling at 0.35 × t_{peak}, same digitization and ADC noise.
All phases considered, as before.
Timing determined here from maximum correlation to a (20× oversampled) pulse template. *One of several possible methods – simple, not necessarily best.*
No dark noise added to signals here!
Time resolutions in ADC sample period and in ns assuming 39.4 MSPS:

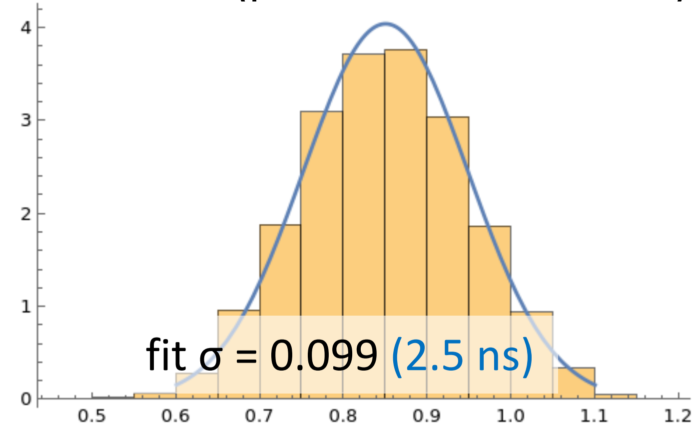
18.5 MeV (peak 3 ADC counts)



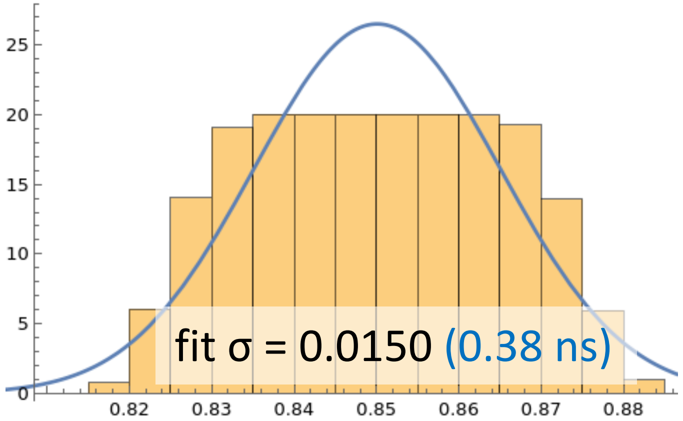
1 GeV (peak 162 ADC counts)

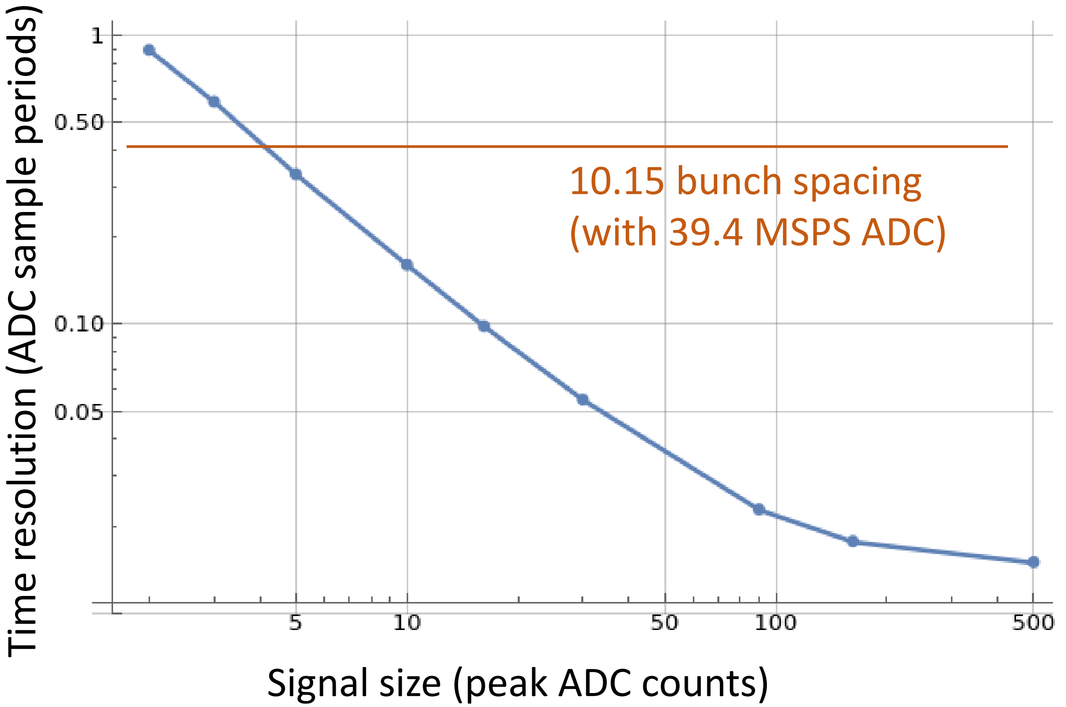


100 MeV (peak 16.2 ADC counts)



3.1 GeV (peak 500 ADC counts)





Pulses larger than ~50 MeV can be attributed to correct bunch crossing. Smaller ones, not always. Dark noise may make this worse.

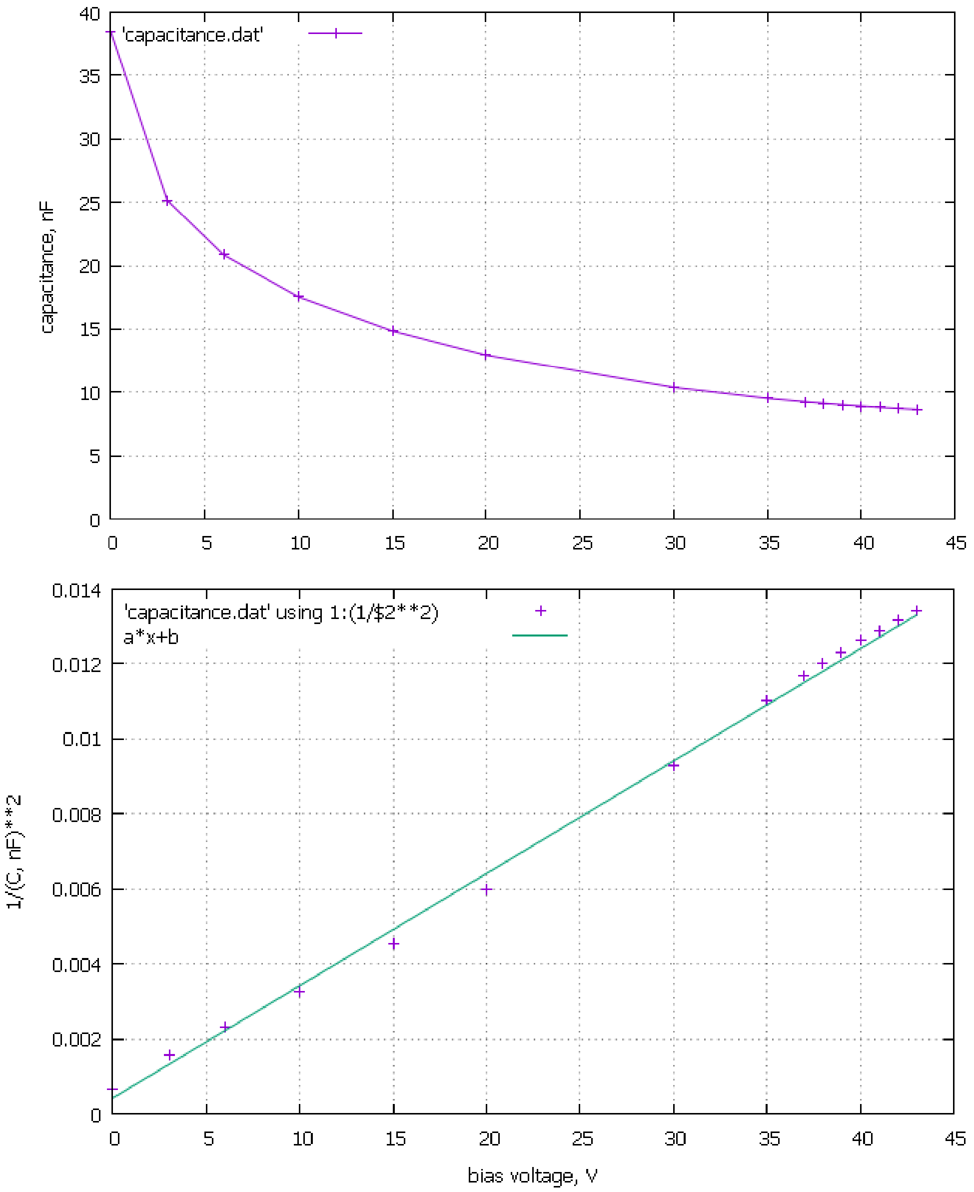
Conclusions

- Response of 4× S14160-6015PS with slightly modified STAR FCS preamp is good
- Before radiation damage, the SiPM / electronics frontend delivers required minimum signal performance with 100 GeV full scale range
- After radiation damage we may have real difficulties with required minimum signals
  - Maybe **40 – 50 MeV at least**, after 100 μA total radiation damage [should† be **~8×10^{9} n/cm^{2} (1 MeV eq.)**]
    - It may be good to cross-check details with STAR FCS results?
  - Improving light yield is the only significant “knob” *(well, besides cooling or annealing)*
  - Peaking time must be as short as possible, it helps somewhat
- Peaking time of ADC sample period / 0.35 is enough for charge measurement (insensitive to phase)
  - 72.5 ns @ 39.4 MSPS, or 58 ns @ 49.3 MSPS (may be feasible, tbd)
  - Peaking times < 80 ns may need complications in preamp – to be investigated
- ADC with 14 bits & 73.5 dB SNR is just adequate for resolution requirements (with 100 GeV full scale)
  - eRD109 bought some 12 and some 14 bits, but we’ll not bother with the 12…
- Small signals (< ~50 MeV) will have a time resolution comparable to bunch crossing period already just due to sampling & digitization
  - Of course dark counts and actual light signal time variations will broaden this further
  - There may be some implications for ‘event building’ from streaming data?

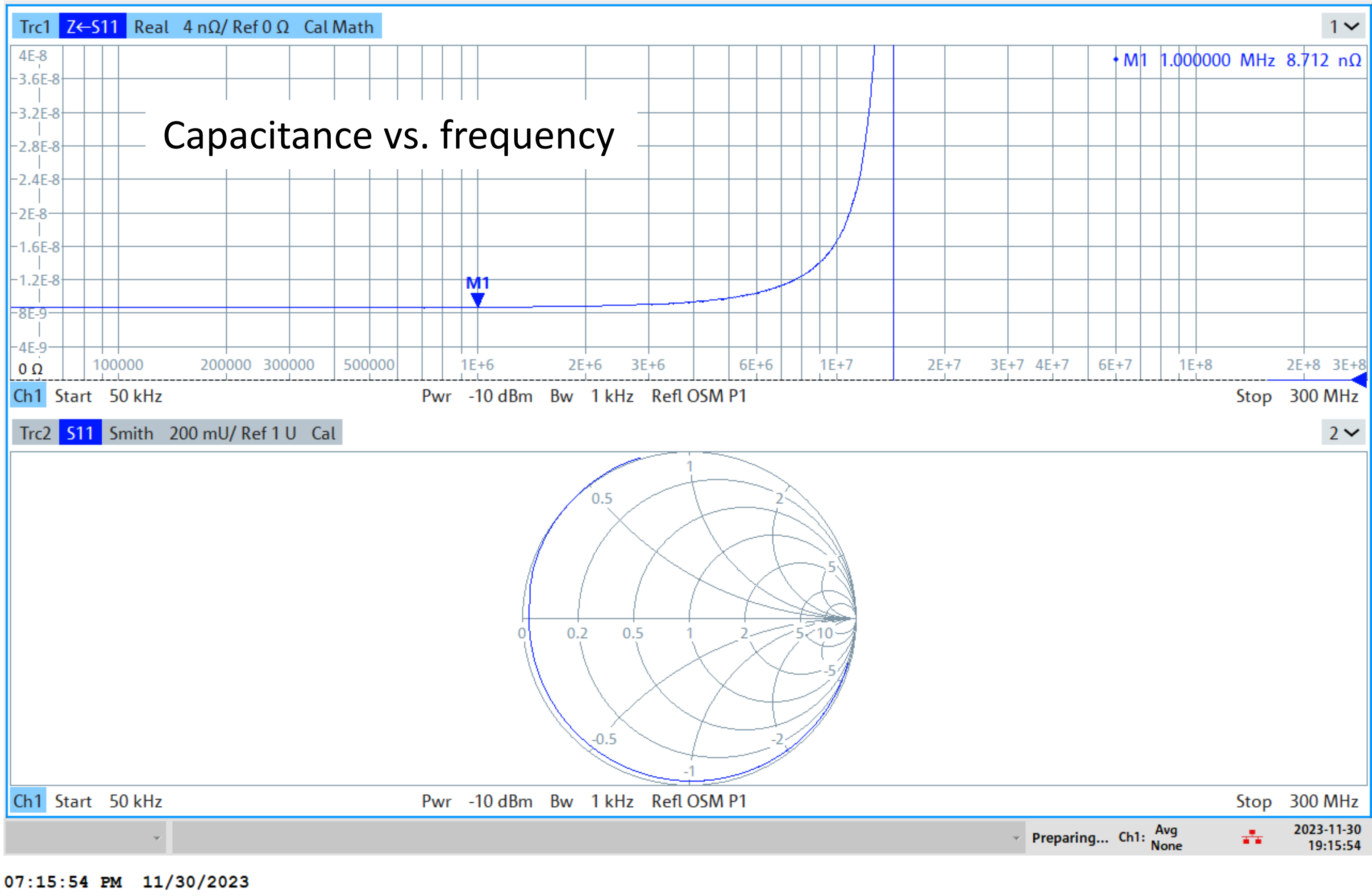
†Assuming 5 μm depletion thickness and damage coefficient $\alpha = 5 \times 10^{-17}$ A/cm

Backup, etc.

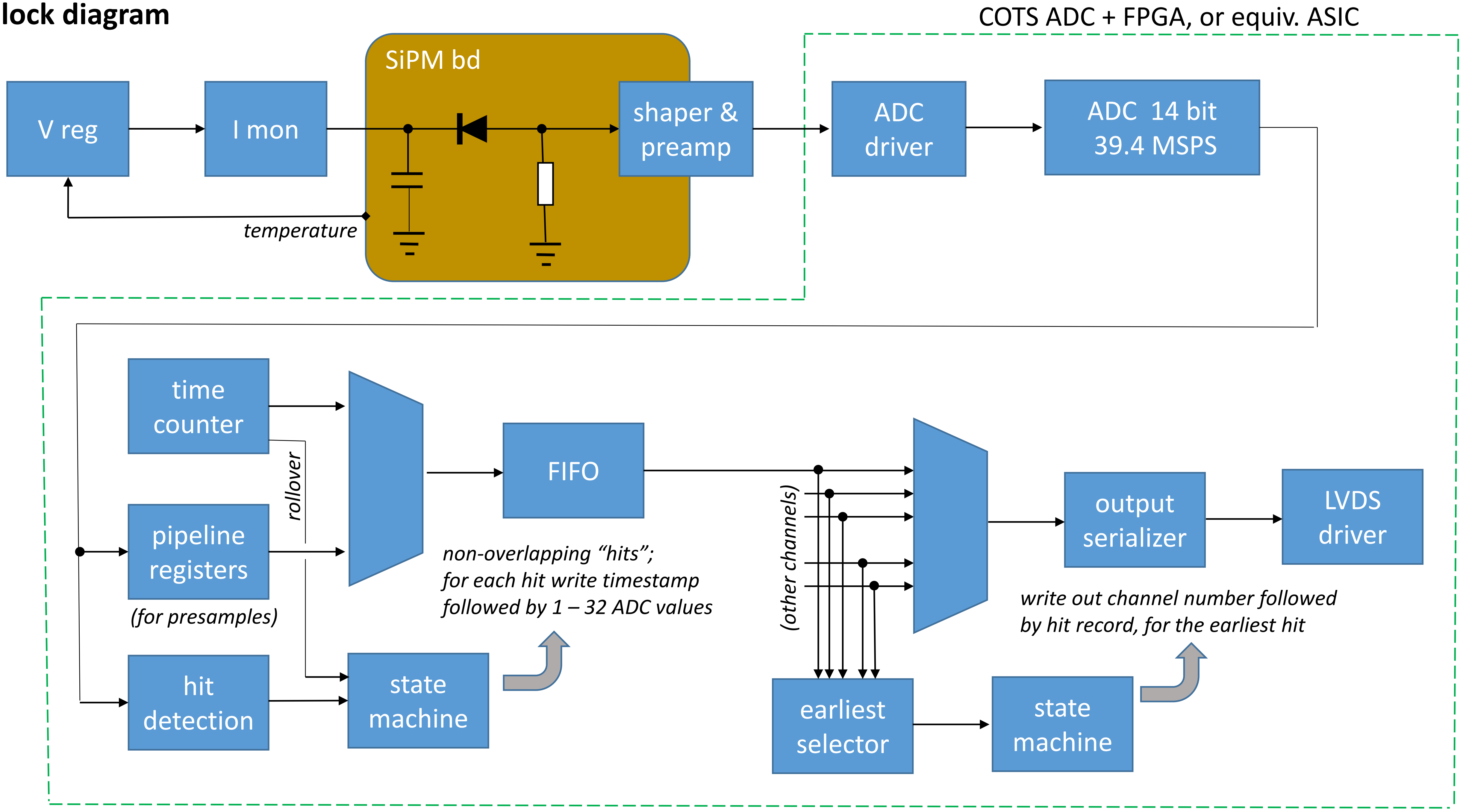
Measured capacitance of 4× S14161-6015PS



42 V, 1.207 uA



Block diagram

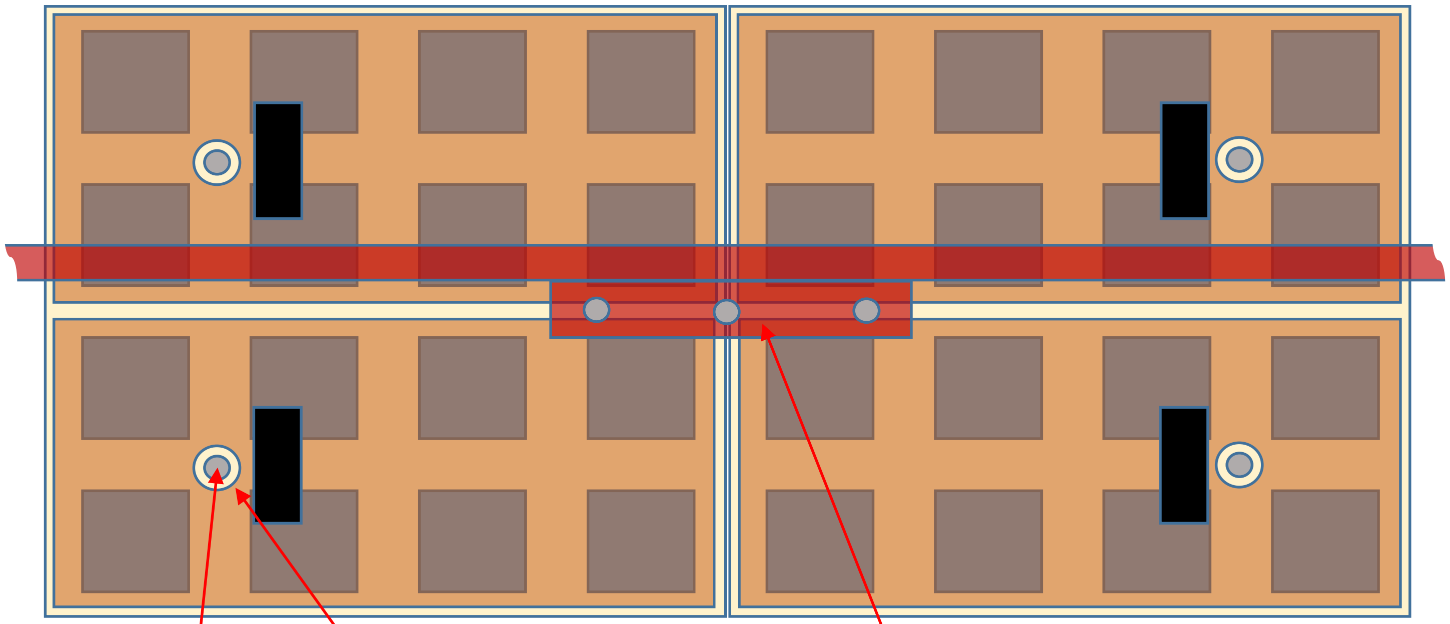


FEB & SiPM carrier mechanical cartoons (dimensioned sketches will be made later)

2-block (32 tower) FEB

This was sketched with old lightguide (one pyramid per tower). This is out of date (see Oleg's presentation). No impact on FEB, so for simplicity (or laziness) I'm not updating it here.

FEB not shown (in this view only)
(but see next page)



standoff **clearance hole** through SiPM carrier PCB

6 or 7 4-40 pan head screws to attach FEB on 4 standoffs and 2 or 3 thermal tab nuts

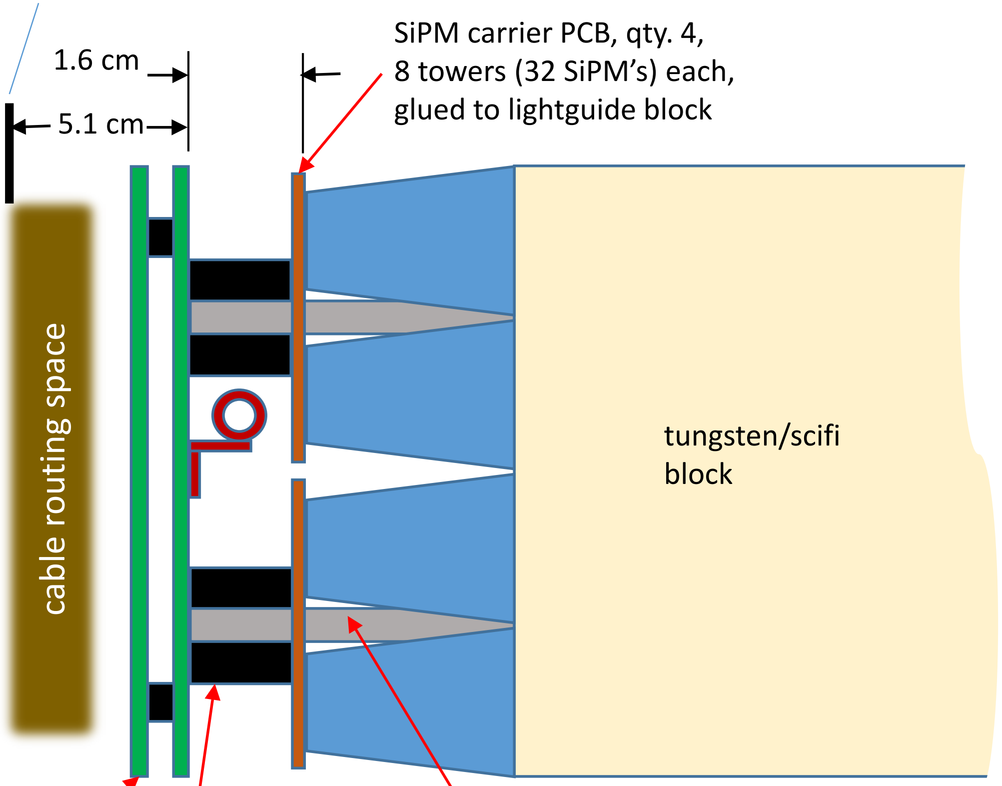
cooling water tubing & small "tab" to PCB
0.19" OD, 0.13" ID
copper "refrigeration tubing"
no fittings inside detector

water tubing connection to FEB is also an electrical ground for FEB (important for noise/EMI and safety)

Integration limit (new)

(forced) air cooling option now ruled out, too difficult to integrate

SiPM carrier PCB, qty. 4, 8 towers (32 SiPM's) each, glued to lightguide block



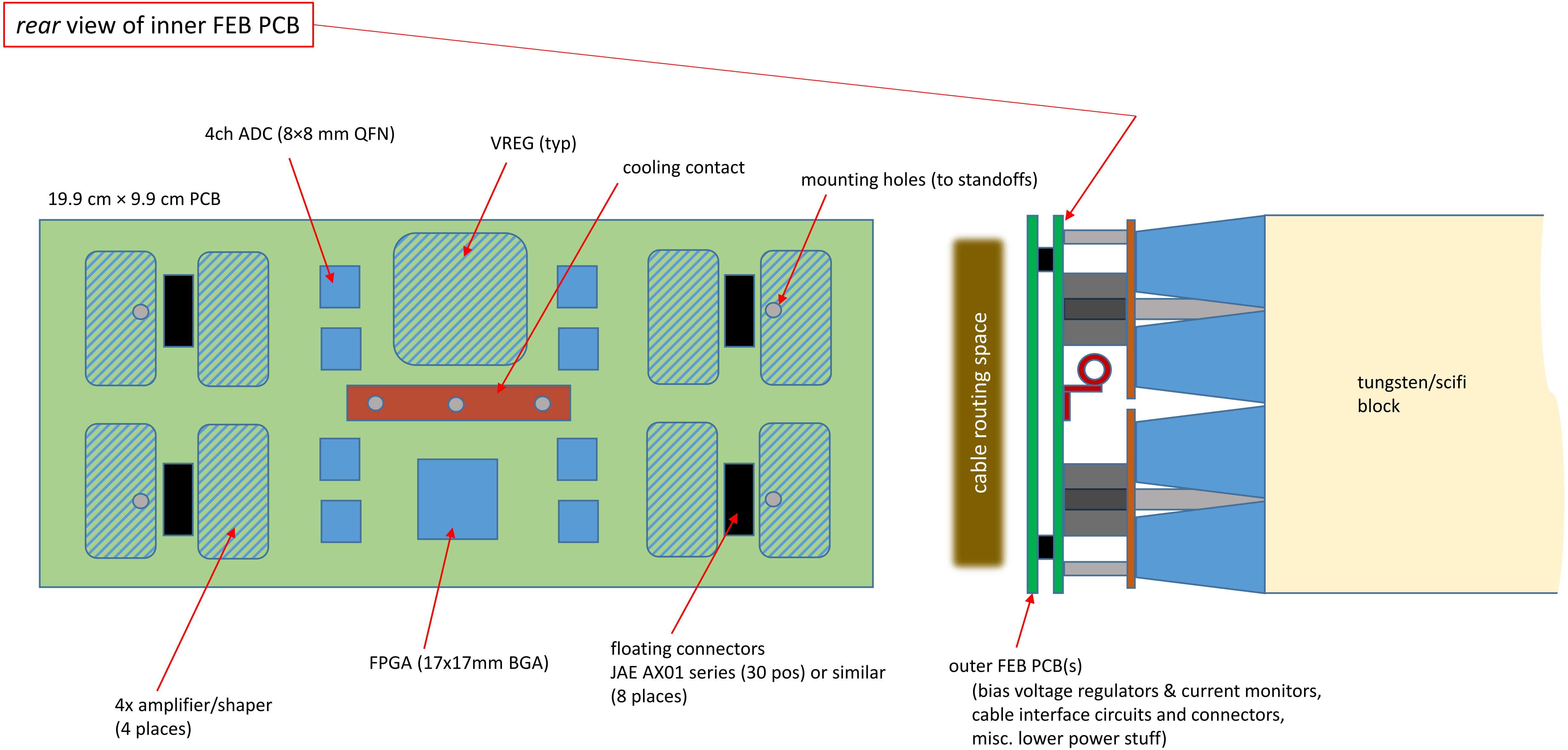
FEB PCB stack
2 – 3 PCB's

4× aluminum 3/16" hex 4-40 standoffs to LG, support FEB **independent of SiPM boards**

floating connectors, 1 per SiPM carrier
JAE AX01 series (30 pos) or similar

prototype FEB mounting standoff

all cables and water tubing route basically *only horizontally* on detector


rear view of inner FEB PCB
4ch ADC (8×8 mm QFN)
VREG (typ)
cooling contact
mounting holes (to standoffs)
19.9 cm × 9.9 cm PCB
cable routing space
tungsten/scifi block
4x amplifier/shaper (4 places)
FPGA (17x17mm BGA)
floating connectors
JAE AX01 series (30 pos) or similar
(8 places)
outer FEB PCB(s)
(bias voltage regulators & current monitors,
cable interface circuits and connectors,
misc. lower power stuff)

fEMCal Integration

(slide from Rahul & Oleg)