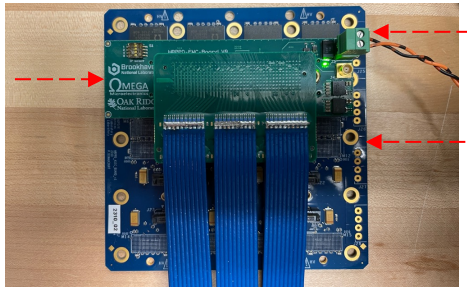
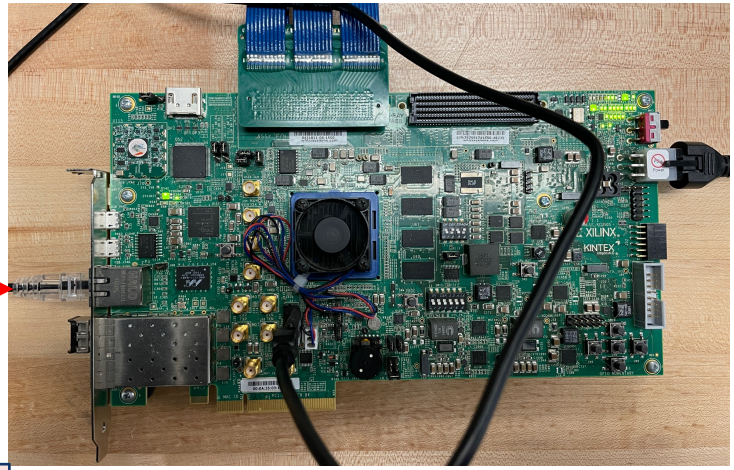
News, discussion & AOB

- HGCROC3 ASIC backplane (V0) debugging started
  - Not much to say yet, though in this configuration (KCU kit instead of an on-board FPGA interface) we just confirmed that a host DAQ PC does indeed see the ASICs
- FPGA board (V0) expected end of February

HRPPD HGCROC3 backplane (V0)



- Beam test in May 2024:
  - No official schedule yet
  - Yet we may start thinking who is coming and when
- Storage & assembly space at BNL
  - But more importantly: what is the assembly procedure?
- TDR contribution planning



KCU105 Xilinx UltraScale FPGA development kit

Mid Jan.24 — Mid Mar.24 — End July 24

process design phase → structuring the effort → Writing (TDR/notes)