On the powering of the ePIC MPGD detector frontends

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Outlook

- Preamble
  - → Power distribution variants reviewed within the context of the VTRX+ use in MPGD FEBs
  - → Several frontend organization options studied for CyMBaL tracker based on system requirements
    - Bandwidth and functional considerations
    - Mechanical, radiation, magnetic field constraints
    - Power needs
      - A back-of-the-envelope python script for rapid estimates of per channel power, power distribution cable cross sections, etc.
  - → Studies applicable to all MPGDs
  - → A lengthy detailed set of transparencies can be shared with interested parties

- Reminder of the MPGD environment
- Power distribution options
- Power requirements of some frontend organizations

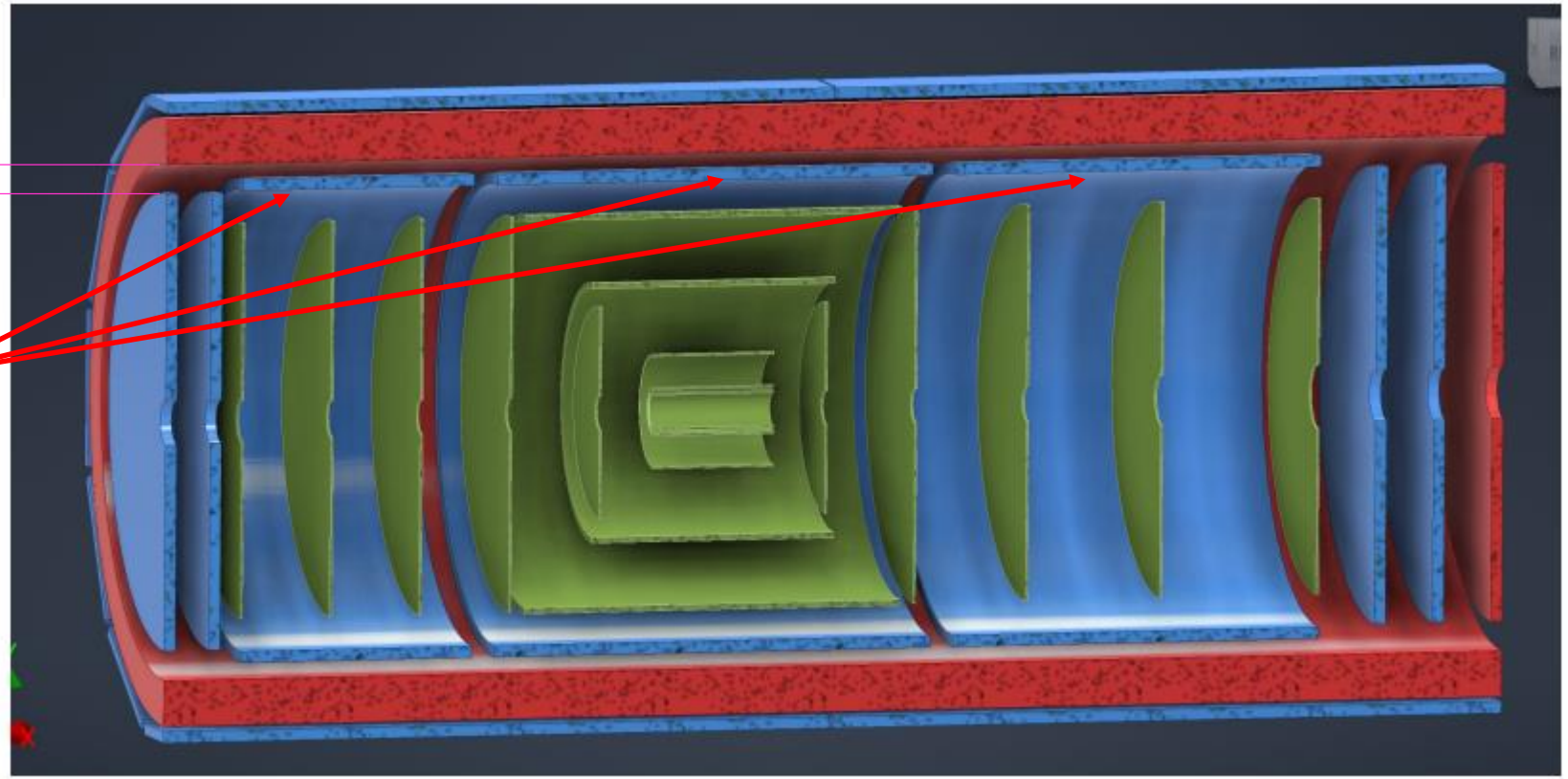
A CyMBaL tracker reminder to illustrate MPGD environment

Spatial constraints for inner barrel cylindrical tracker

- Space is stringent: 6 cm
  → Detectors, gas pipes, HV cables

60

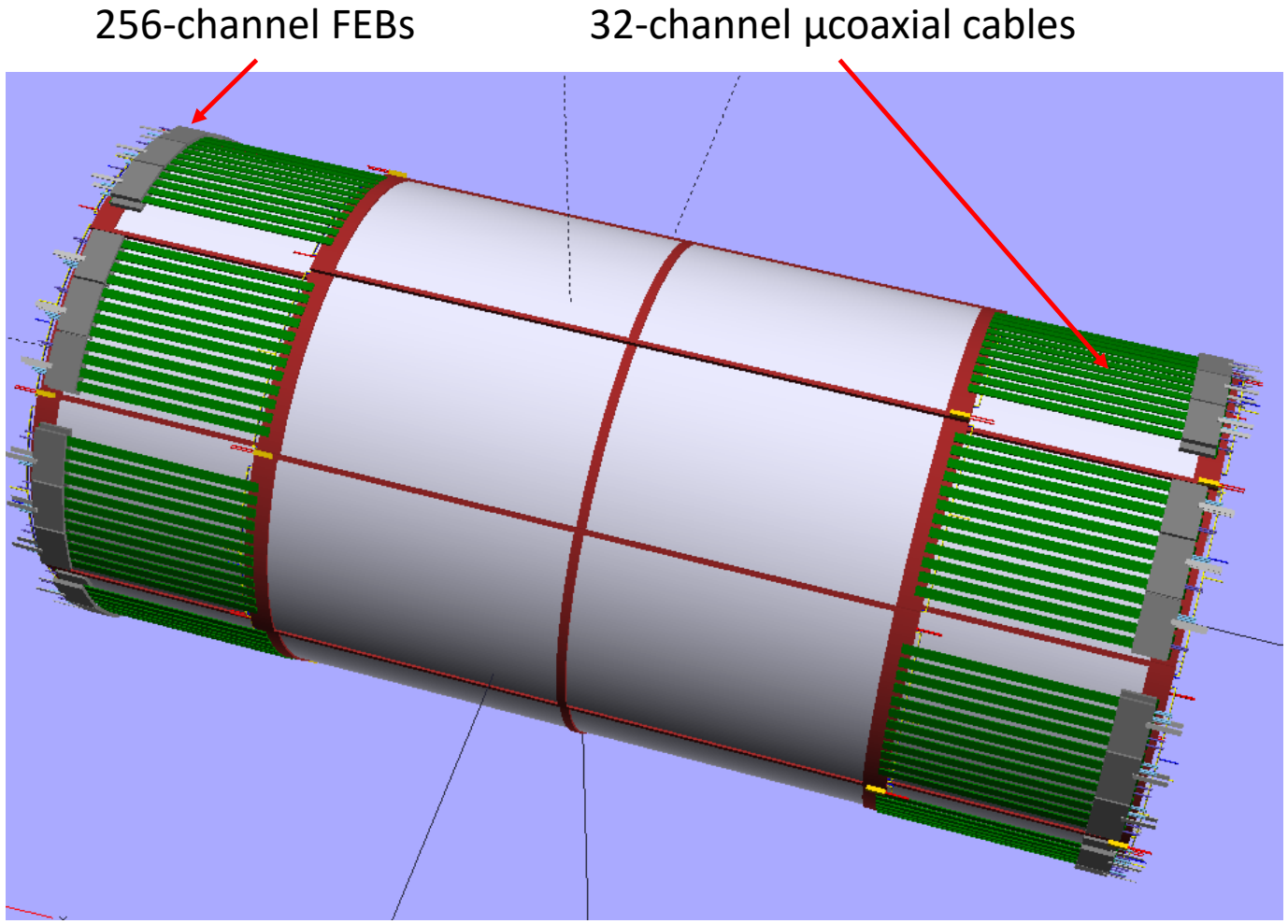
Cylindrical
Micromegas
(Saclay interest)



- On detector frontend electronics
  → FEBs + LV distribution + RDO interface cabling + cooling

Example of CyMBaL: one of the possible configurations under study

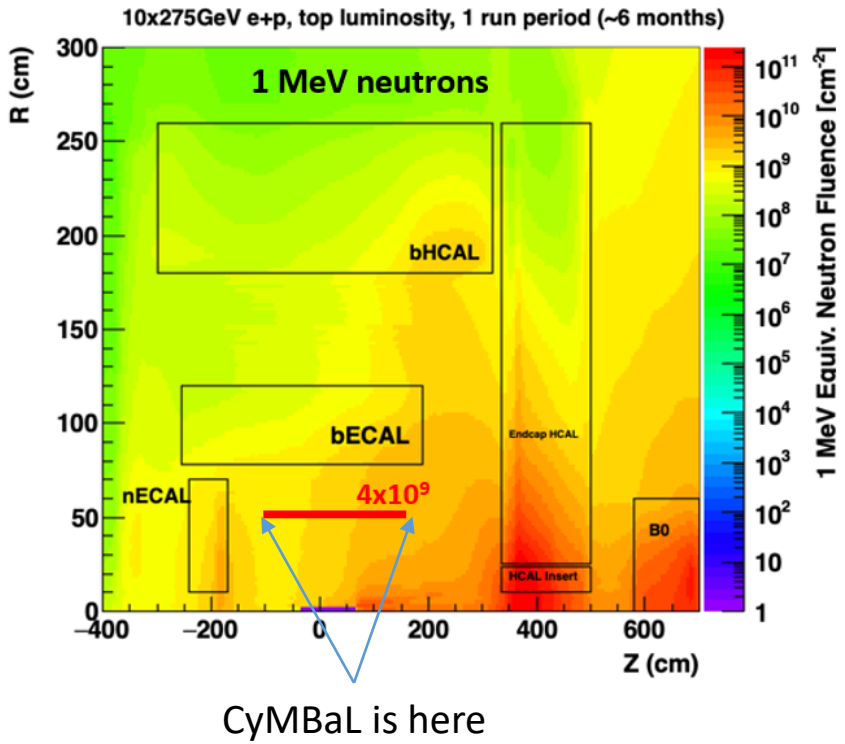
- Still under torment of optimization
  - → Just a snapshot to give an idea
- 32K channels
- 128 256-channel FEBs
  - → Only central detector FEBs visible
    - Peripheral FEBs in a row bellow
    - Or in a second row
- 32 1024-channel RDOs
  - → 4 FEBs per RDO
- Where to place RDOs not really clear
  - → Electrical FEB-RDO interface : 5-6 m
    - 16 on either side of Barrel
    - Can probably be placed further away using driver-buffers but potential issues of ground loops and noise pickup
  - → Optical FEB-RDO interface : no limit
    - Attractive option



Inner detector fronted environment

- Stringent space
- Restricted material budget including for cooling
- Magnetic field
- Radiation

- Example of CyMBaL tracker environment
  - → TID after 10 years : 10 krad
  - → Neutron fluence after 10 years: 10^{11} n_{eq} / cm^2
  - → 20 MeV proton flux: 100 particle / cm^2 / s
  - → Magnetic field: 1.9 T



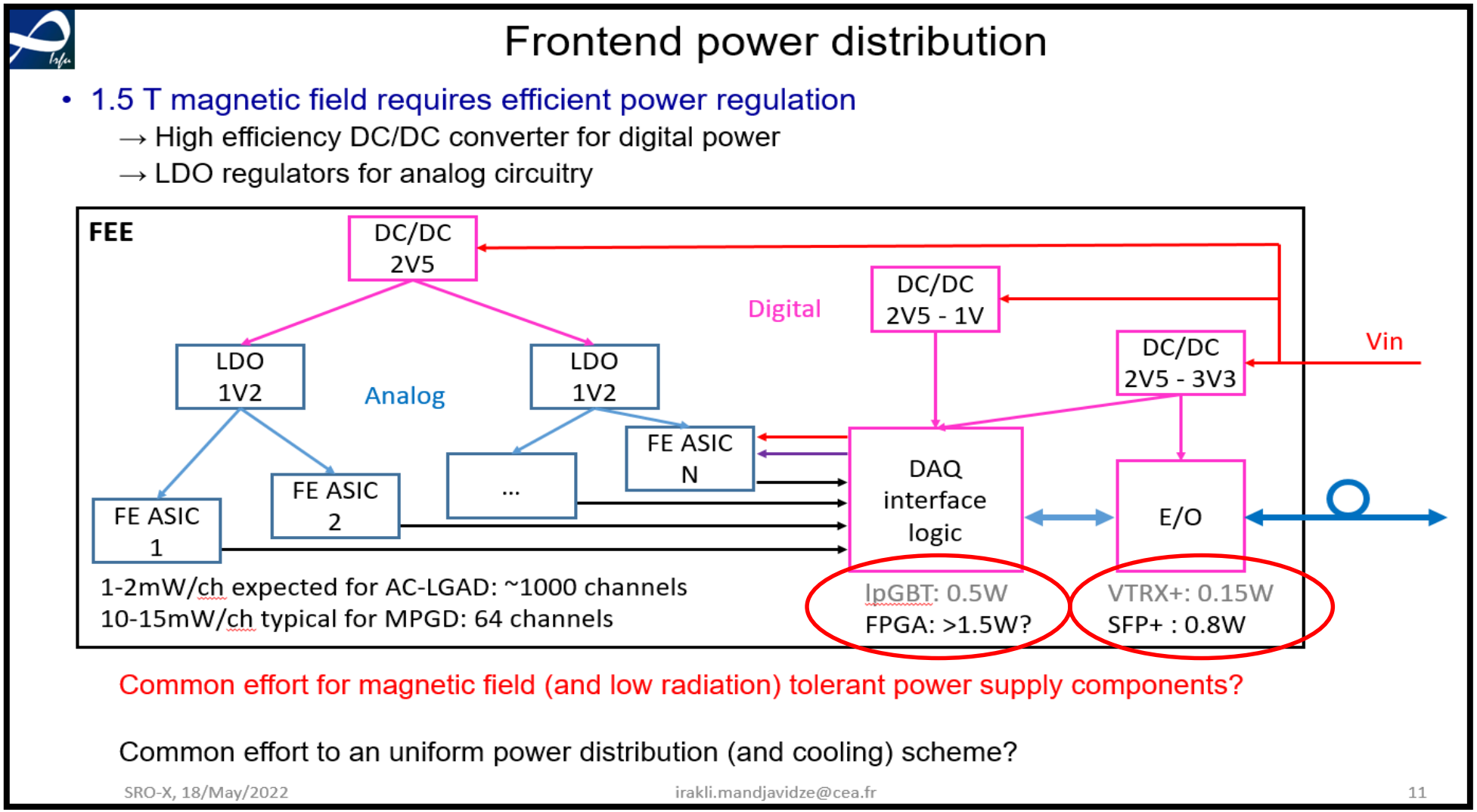
- Similar radiation and magnetic field environment for other MPGD detector frontends

Power distribution options considered

(Note: serial power option has not been studied)

Power distribution: a reminder from the past

- Just for fun: presented on 18 may, 2022, during SRO-X workshop
  → https://indico.jlab.org/event/519/contributions/9563/attachments/7748/10855/220518_SroX_FrontEnd_IM.pdf

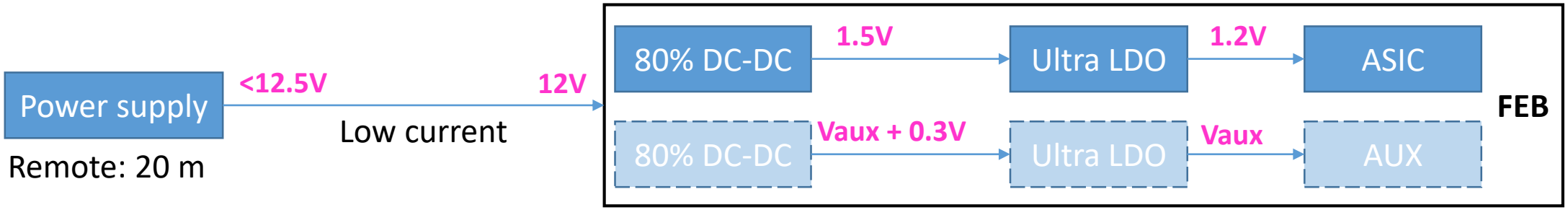


FEB power distribution options : DC-DC

- DC/DC-based LV distribution: to be magnetic field tolerant

→ Remote power supply distributes 12V with a low voltage drop over 20 m cables

- Say less than 0.5V
  - The lower the drop the lower the power dissipation in cables but the large is their cross-section



→ Higher efficiency

→ Low cross-section power cables

→ Less overall* mW/ch

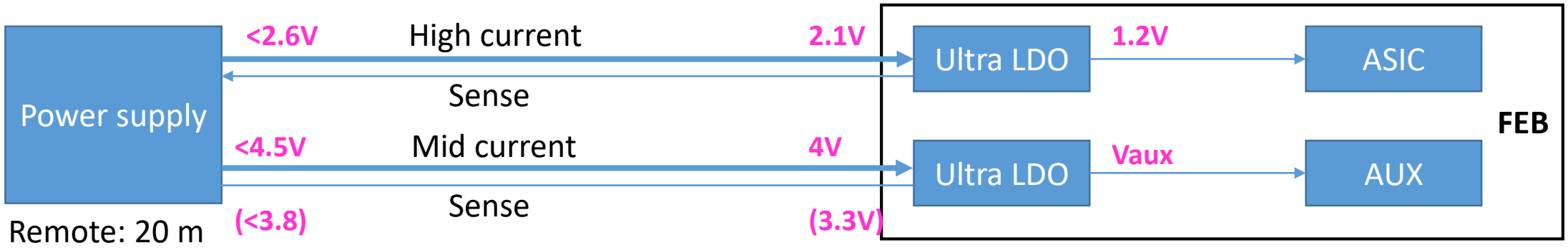
*Overall : Power supply W / nb of channels
includes loses in cables, regulator inefficiencies

→ DC/DC regulators might be bulky and a source of EMI

- Space + extra material for shielding
- Not clear if 80% efficiency can be really achieved

FEB power distribution options : LDO

- LDO-based LV distribution
  - → Remote power supply distributes 2.1V and any auxiliary voltages with a low voltage drop over 20 m cables
    - Say voltage drop is < 0.5V
      - The lower the drop the lower the power dissipation in cables but the large is their cross-section
  - → Low cross-section sense wires for remote power regulation

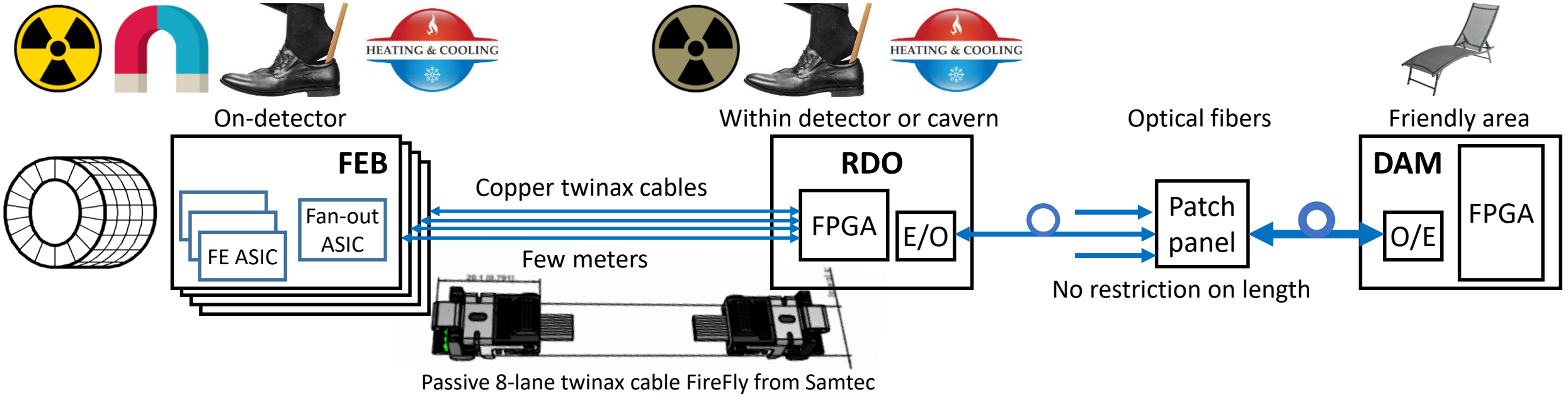


- → Lower efficiency
- → High cross-section power cables
  - Space due to thick cables
- → High overall* mW/ch

*Overall : Power supply W / nb of channels
includes loses in cables, regulator inefficiencies

Examples of power requirements of some MPGD FE organization options

FEB with no on-board intelligence and electrical interface



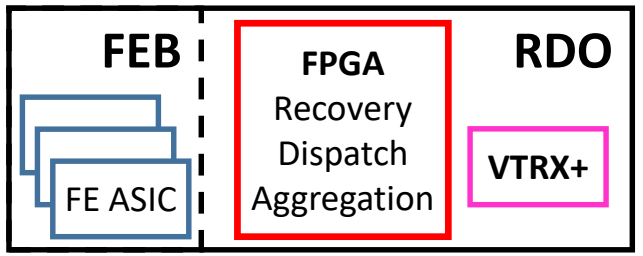
- FEB
  - → Radiation hardened ASICs
  - → Low active component count: minimal power consumption
    - ~30-35 mW / channel
    - 1 mm^2 (DC/DC + LDO) or 5.6 mm^2 (LDO only) wires to power a FEB

- RDO : most probably MPGD specific hardware
  - → No buffer-drivers: is there any suitable place within 5-6 m?
  - → Buffer-drivers: space constraint relieved with some extra power consumption but
    - Ground loops with noise pickup over 20 m long signal cables

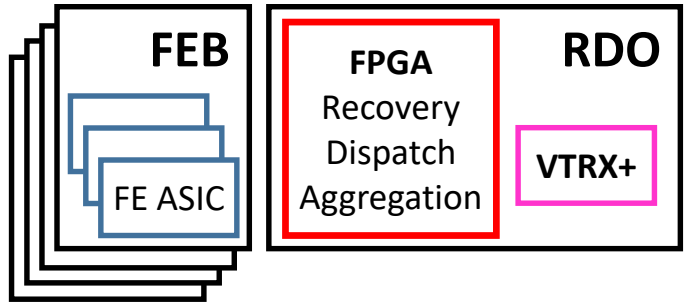
Merged FEB / RDO with optical VTRX+ interface

- On-FEB RDO in a harsh environment

- Merged FEB / RDO : Worst power consumption scenario
  - → 50% increase compared to a FEB with electrical RDO interface
    - 45-50 mW / channel
    - 1.5 mm^2 (DC/DC + LDO) or 8 mm^2 (LDO only) wires to power FEB

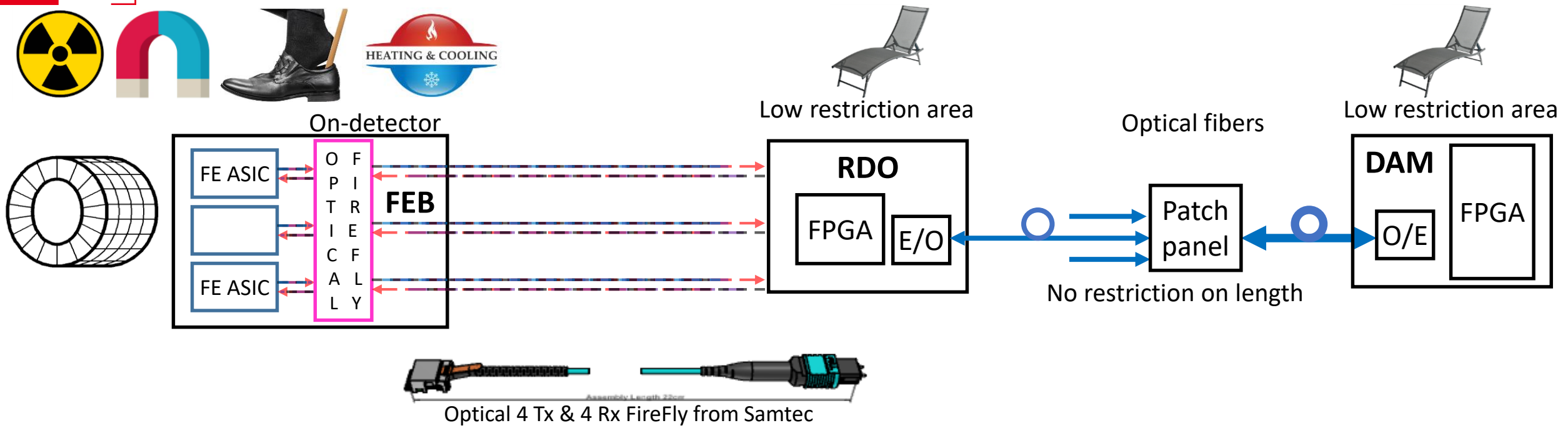


- An RDO per detector module : 4 FEBs / RDO
  - → ~11% more power compared to a FEB with electrical RDO interface
    - 33 – 37 mW / channel
    - 1 mm^2 (DC/DC + LDO) or 6 mm^2 (LDO only) wires to power FEB



- Cooling and its additional infrastructure !
- SEU effects need to be understood, acceptable failure rates to be agreed on
- Powering FPGA requires “whole lotta” different voltages : (3V3), 2.5V, (1.8V), 1.2V, 1V, (0.9V)
  - → Deriving them from a single auxiliary power source may be inefficient
  - → Avoid mixing analog digital power sources

FEB with optical interface: COTS optical FireFly



- FEB
  - → ASICs directly connected to 4-lane bidirectional parallel optic FireFly transceivers
    - Single Rx line encoding clock, sync run-control and asynchronous slow control and monitoring commands
  - → Low active component count: low power consumption
    - ~35-37 mW / channel - 15% increase compared to a FEB with electrical RDO interface
    - 1 mm^2 (DC/DC + LDO) or 6 mm^2 (LDO only) wires to power FEB
- RDO : common hardware

Few examples of MPGD FE powering

- ASICS:
  - → 32-channel Sampa: 10-20 mW/ch
    - Depending on sampling rate (5-10 MSPS) and DSP activity (*e.g.* off-on)
  - → 64-channel VMM: 16 mW/ch

- Frontends
  - → 160-channel FEC of ALICE TPC 16W / 100 mW/ch
    - 5 SAMPAs, 2 GBTx, 2 VTRx, LDOs
    - In magnetic field
  - → 256-channel FEE of sPHENIX TPC/TPOT 19W / 75 mW/ch
    - 8 SAMPAs, FPGA, 2 optical transceivers, LDOs
    - In magnetic field
    - Power distribution to be checked
  - → 512-channel MMFE8 of ATLAS NSW 16W / 31 mW/ch
    - 8 VMMs, ROC ASIC, SCA, FEAST DC/DCs
      - Electrical interface
    - Out of magnetic field
    - 11V distributed – no need for large cross-section cables
  - → 512-channel FEU of Clas12 MVT/FTT/Bonus 20W / 40 mW/ch
    - 8 Dreams, ADC, Virtex6 FPGA, 1 optical SFP, 1 GE SFP, LDOs
    - In magnetic field
    - 4.5V distributed to 8 FEUs over 5m with 16 mm^2 wires

Characteristics of the low-voltage supply system.

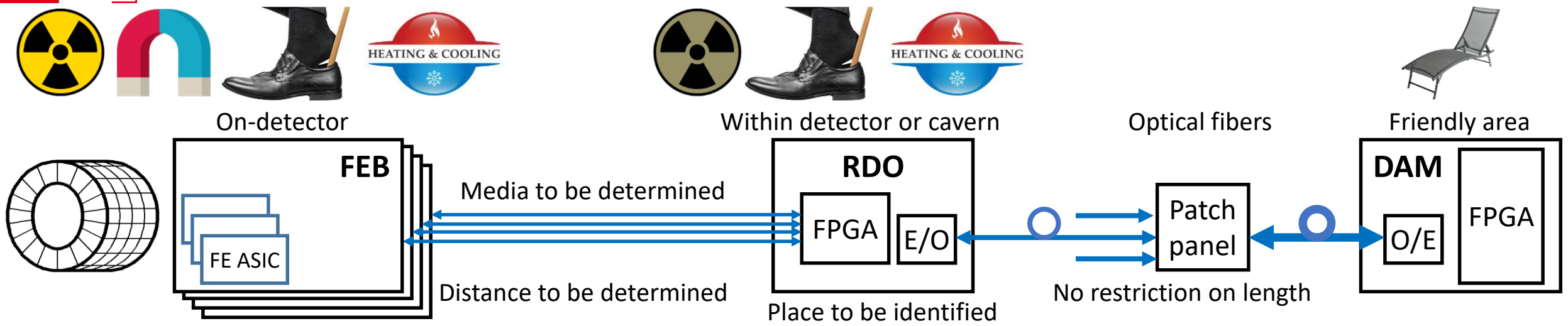
Parameter	Analog supply	Digital supply
Supply voltage (V)	4.9 (5.2)	4.1 (4.4)
Cable cross-section (mm^2)	150	300
Current (A)	83	133
ΔU in cables (V)	0.65 (0.92)	0.9 (1.2)
Total power per sector (W)	407 (432)	545 (585)

Discussion

- Frontend power distribution in magnetic field is challenging
- The use of magnetic field tolerant high efficiency DC-DC regulators is an attractive option
  - → Assuming they have a low form factor and represent low EMI source
  - → Possibility to cascade regulators in a step-down chain having last stage close to frontend
- Direct distribution of low voltage may require bulky cables in a limited space
  - → Shielding of the cables will make them even more thicker and rigid
- COTS power regulators may still suffer from SEUs even in mild radiation environment
  - → Especially errors in “Enable” circuitry may result in temporary power-cut of some parts within a frontend
- Additional complexity may come from FPGAs with their diversity of power sources
- Some numbers :
  - → MPGD frontends : ~600
    - Risk mitigation MPGD disks : ~200 FEBs
  - → Assume 256-channel FEBs
  - → Assume 30 mW/channel
  - → 4.5 kW
    - 6 kW with risk mitigation
- Common approach is more than welcome
  - → Including common procurement

Backup

FEBs and RDOs



- FEB
  - → Number of rad-hard FE ASICs
  - → As low power consumption as possible
  - → ~2 T magnetic field

- RDO
  - → Middle to low-end FPGA
  - → Distribute clock and synch commands to FEBs
  - → Configure and monitor of FEBs
  - → Receive data from several FEBs, format them and convey to DAMs

- RDO ↔ FEB link
  - → Downstream: clock & sync commands, configuration and monitoring requests
  - → Upstream: data, configuration and monitoring responses

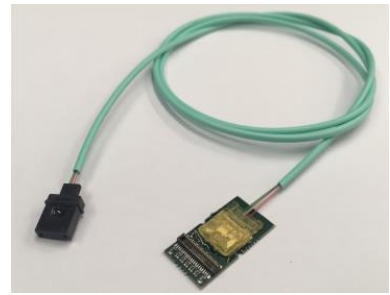
  - → Over copper: 5-6 meters
    - RDO is in a restricted area inside the detector
      - Size / place / power / cooling
      - Ground loops

  - → Over fiber: no limit
    - RDO in a low restriction area in cavern

FEB with optical interface: VTRX+

- FE ASICs are directly interfaced to VTRX+
  - → Downlink with embedded clock / sync / async data distributed with high fidelity fan-out
  - → Requires an “innovative” ASIC interface
    - Working on CDR circuitry for Salsa

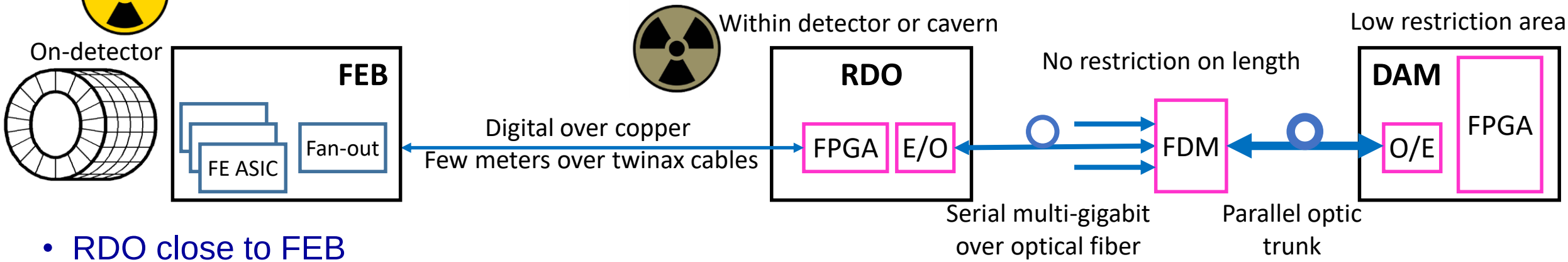
CERN VTRX+



- FEB
  - → Radiation hardened ASICs
  - → Minimal power consumption after electrical interface option: only VTRX+ consumption added
    - ~ 32-35 mW / channel - 8% increase compared to a FEB with electrical RDO interface
    - 0.9 mm^2 (DC/DC + LDO) or 5.8 mm^2 (LDO only) wires to FEB
- RDO : common hardware

Example: powering of a FEB with passive electrical RDO interface

FEB with no on-board intelligence and electrical interface



- RDO close to FEB
  - → Moderate radiation environment, space & power stringent

FDM – fiber distribution module (patch panels, etc.)

- RDO ↔ FEB
  - → Clock & synch commands – on FEB fan-out or multi-drop
  - → I2C – daisy chain
  - → Data – single or several uplinks per ASIC

RDO ↔ FEB

Rafael

65nm PLL

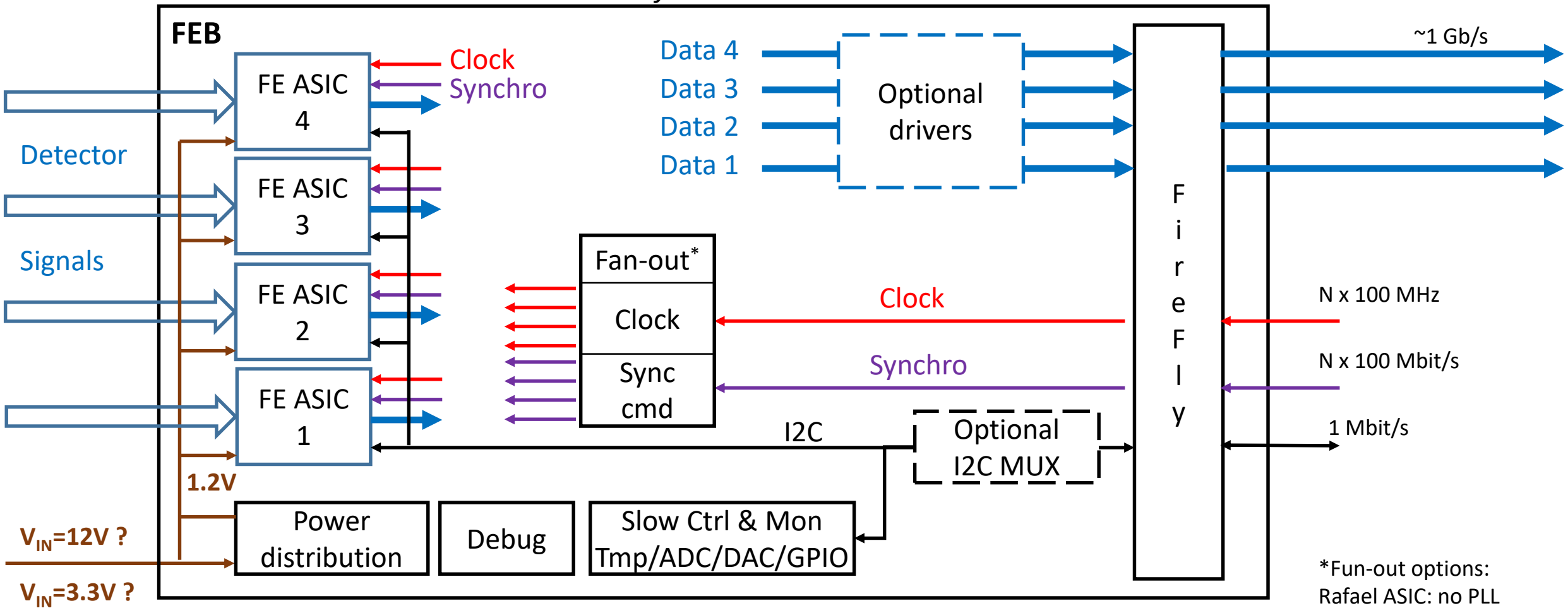
- FEB
  - → No on-board intelligence, no board-level data aggregation
  - → High fidelity fan-out candidates: Rafael ASIC or a development based on EICGENR&D_2022_06
    - Used solely for clocks and commands; not for I2C

- On detector FEB: best option for S/N
  - → Difficult for all the rest

FEB with electrical RDO interface and no on-board intelligence

- Number of ASICs per FEB can be adapted according to detector modularity and space constraints

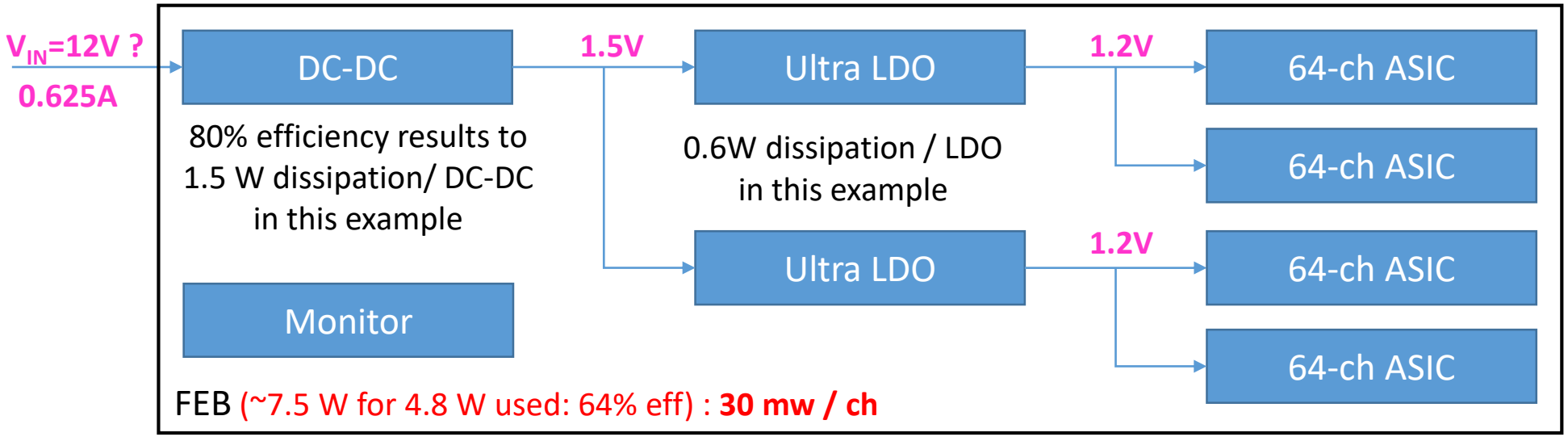
  → As well as lanes of the electrical FireFly interface



- FEB to RDO distance limited to 5-6 m : where to place RDOs in this range?

Powering within magnetic field

- Assuming 64-channel Salsa with ~1 W power consumption @ 1.2 V
  → For simplicity, 1 A per ASIC
- Clean power will require a radiation tolerant ultra LDO linear regulator
  → *e.g.* commercial TPS7H1101A-SP from TI - https://www.ti.com/product/TPS7H1101A-SP - space grade
  → *e.g.* community LDO used for CMS HgCal frontends - https://cds.cern.ch/record/2797683 - HL LHC grade
  → Or whatever proposed by other subsystems
- Power distribution may require magnetic field tolerant high efficiency DC/DC regulators
  → *e.g.* community bPOL12V from CERN – HL LHC grade and 4T tolerance
    - Microsoft Word - bPOL12V_V6 datasheet V1.6.docx (cern.ch)

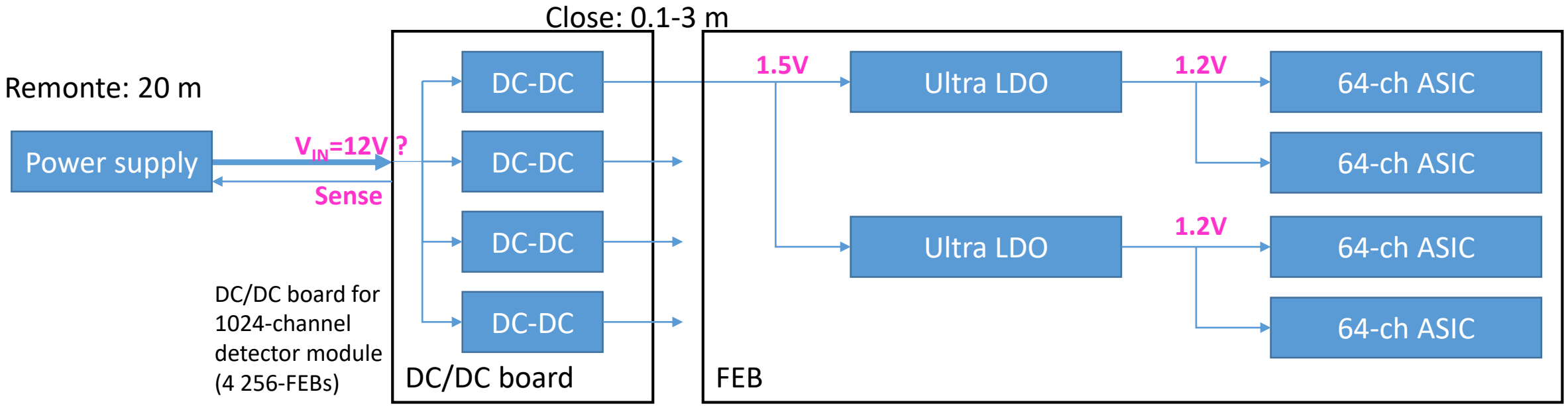


- Question: is there a common effort for LV distribution?
  → A centralized group taking care to provide V_{IN} in a “uniform” way wherever possible
  → And in case CERN components will be the choice, for their inventory and procurement

Power distribution: about DC/DC regulators

- The use of magnetic field tolerant DC/DC converters is attractive for efficient powering
- However, they might be bulky
  → One of the designs integrating bPOL12V from CERN requires ø12 mm and *H* 3mm coils
- And they might be a source of EMC noise requiring a special shielding
  → Extra material budget in the vicinity of trackers if DC/DC converters sit directly on FEBs

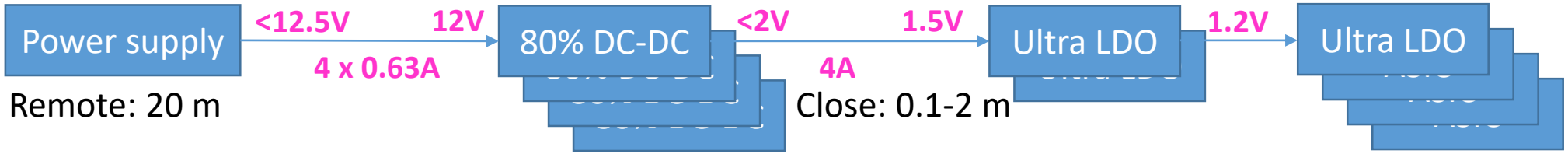
- Shell they be placed on dedicated boards not too far from FEBs?



- Next page

Power distribution option for a 1024-channel CyMBaL module: 4 FEBs

- A 256-channel FEB with passive electrical RDO interface consumes 7.5 W
  - → With on-board or close-to-board DC-DC converters
    - 12V is distributed to DC-DC converters to produce 1.5V for LDOs to produce 1.2V for ASICs



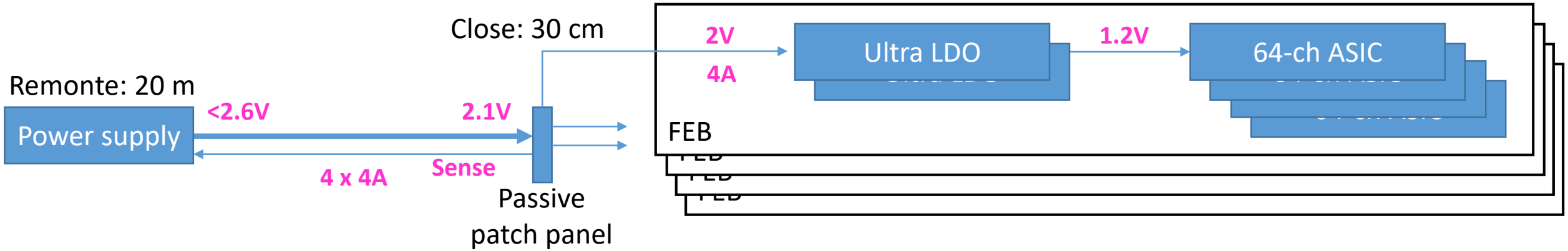
  - → Assume DC/DC – LDO connection induces no more than 0.5V drop: DC/DC output set @ 2V
    - Power dissipation in wires: max 0.5 x 4 = 2 W: what should be the wire cross-section for a given length?

DC-DC to LDO Distance m	Wire cross section mm^2	Comment
0.3	0.1	Not clear if there is a place for DC/DC power board
1	0.3	Noise pickup on 1 m long cables
2	0.6	Not reasonable: usually needs active regulation

- A 1024-channel Module consumes 30W
  - → Assume PS – DC/DC connection induces no more than 0.5V drop: PS output set @ 12.5V
  - → If PS is 20 m away the cross section of the power wires should be 2 x 3.5 mm^2

Power distribution for a 1024-channel CyMBaL module w/o DC/DCs

- If DC-DC converters cannot be placed on FEBs or in a close vicinity, can they be dropped off at all?
  → Low voltage is distributed directly from remote power supply?



- A 256-channel FEB with passive electrical RDO interface consumes 8.4W
  → With DC-DC converter dropped
  - 2.1V is distributed to LDOs to produce 1.2V for ASICs
    - 1.5V distribution with sense wire regulation on a long distance might be problematic; increased to 2.1V

- A 1024-channel detector module consumes 33W

- Assume PS – LDO connection should not induce more than 0.5V drop: PS output set @ 2.6V
  → If PS is 20 m away the cross section of the power wires should be
  - 2 x 5.5 mm^2 if FEBs are individually powered
  - 2 x 22 mm^2 if a common power is delivered to a 1024-channel detector module

To summarize on FEB with passive electrical RDO interface

- Low active component count: minimal power consumption

- Clock and synchronous command distribution via a high fidelity radiation hardened fan-out
  → Rafael : no internal PLL; Exists
  → Prisme : internal PLL with phase adjustment; Under development

- No on board aggregation: ASIC data links interfaced directly with the RDO receivers

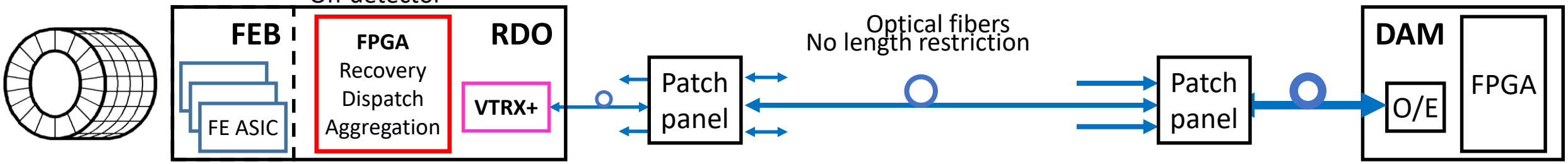
- FEB to RDO distance limited to 5-6m
  → Active driver-repeater-buffers can be used to increase the distance
  → Attention should be paid to ground-power return passes and pickup noise

- Expected power consumption of a 256-channel FEB
  → 7.5 W with on-board or closely coupled DC/DC : 30 mW / channel
    - 3.5 mm^2 wires would be appropriate to distribute required power to entire 1024-channel detector module
    - Location of the magnetic field tolerant bulky DC/DC converters will most probably be problematic
  → 8.4 W without DC/DC regulators : 33 mW / channel
    - !!! 5.5 mm^2 if FEBs are individually powered
    - !!! 22 mm^2 if a common power is delivered to a 1024-channel detector module

Example: powering of a merged FEB / RDO

Merged FEB / RDO with optical VTRX+ interface

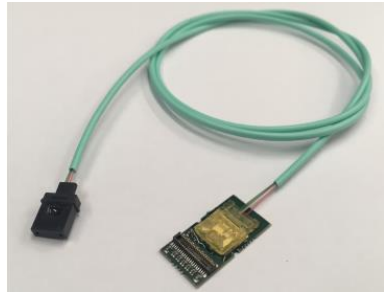
Low restriction area



- On-FEB RDO in a harsh environment

- FE ASICs are thought with “lpGBT / CERN” interfaces
  - → Separate lines for downstream interfaces: clock, synchronous commands, asynchronous configuration commands
  - → VTRX+ needs to be coupled with an on-RDO “intelligence” to recover this imbedded information
  - → CERN has lpGBT; ePIC counts on FPGAs

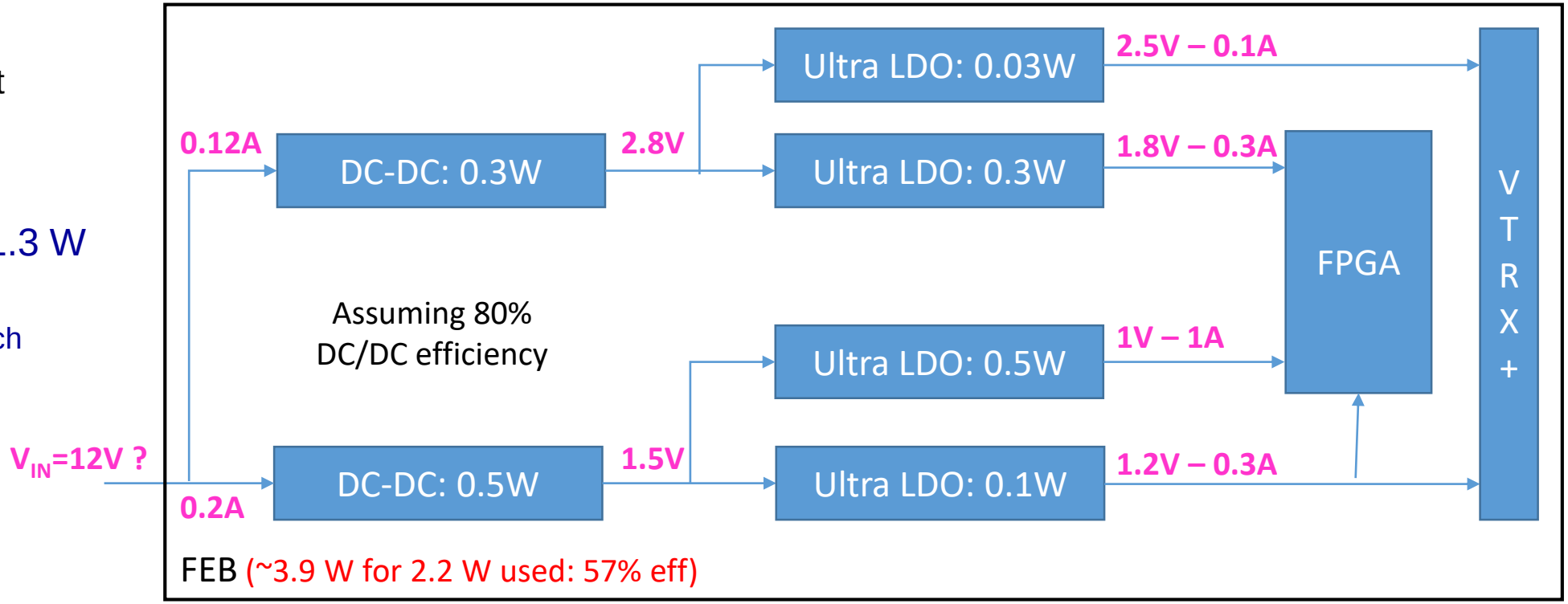
CERN VTRX+



- On FEB FPGA / VTRX+ combination
  - → SEU effects need to be understood, acceptable failure rates to be agreed on
    - Estimation: 8h MTBF for entire CyMBaL with a low cost low profile Latice Nexus radiation tolerant FPGA
  - → Worst power consumption scenario
    - Estimation: 45-50 mW / channel - 50% increase compared to electrical interface
    - 1.5 mm^2 (DC/DC + LDO) or 8 mm^2 (LDO only) wires to power FEB
  - → Cooling and its additional infrastructure !

An extra power load from FPGA (and VTRX+): local DC/DC option

- Guess for Lattice LIFCL-40-9BGA400 FPGA power rails : inspired from evaluation kit design
  - → Core: 1.0V – 800 mA 0.8 W
  - → Analog VCC for SER-DES: 1.0V – 200 mA 0.2 W
  - → Digital VCC for SER-DES, ADC, VCCAUX: 1.8V – 300 mA 0.6 W
  - → IO VCC: 1.2V – 250 mA 0.3 W
- VTRX+
  - → Supply voltage 1V2 1.2V – 4 + 12 mA / ch Max 55 mA 0.07 W
  - → Supply voltage 2V5 2.5V – 44 + 13 mA / ch Max 100 mA 0.25 W
- Extra 2.2 W
  - → Needs refinement
  - → 3.9 W
- 256-channel FEB: 11.3 W
  - → 44 mW / channel
    - 14 extra mW/ch



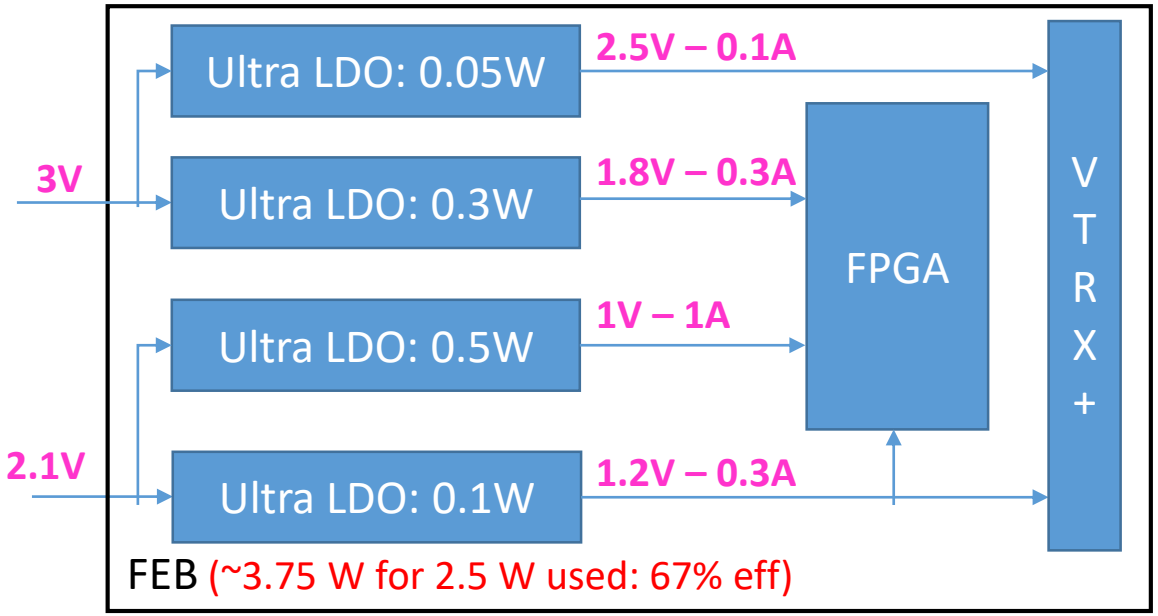
On power distribution: LV to FEB without DC-DC regulators

- Distribute 3V and 2.1V from remote power supplies to FEBs
  - → Assume 2.1V is distributed to FEB LDO to produce 1.2V for ASICs / VTRX+ and 1V for FPGA
  - → Assume 3V is distributed to FEB LDO to produce 2.5V for VTRX+ / FPGA and 1.8V for FPGA
  - → Low cross-section sense wires to ensure on-load regulation

- Power consumption of a 256-channel FEB with passive electrical RDO interface: 8.4W
  - → *e.g.* copper FireFly
  - → 1.2V – 4A : 2.1V x 4A = 8.4W — 33 mW/ch

- VTRX+ add-on: ~0.4W — 1.6 mW/ch
  - → 1.2V – 0.05A : 2.1V x 0.05A = 0.1W
  - → 2.5V – 0.1A : 3V x 0.1A = 0.3W

- FPGA add-on: ~3.6W — 14 mW/ch
  - → 1V – 1A : 2.1V x 1A = 2.1W
  - → 1.2V – 0.25A : 2.1V x 0.25A = 0.63W
  - → 1.8V – 0.3A : 3V x 0.3A = 0.9W

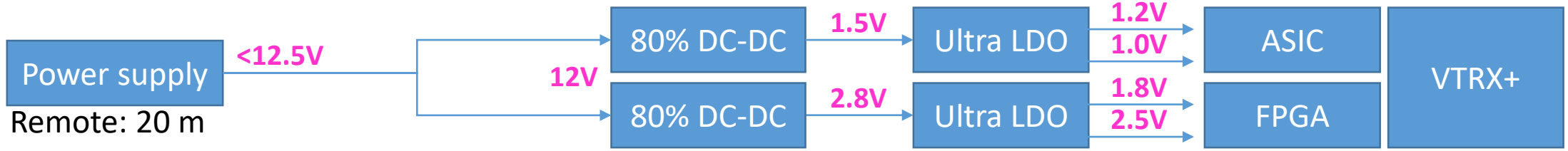


- Power consumption of a 256-channel FEB with FPGA & VTRX+ : 12.5W — 48 mW/ch
  - → Extra 15 mW/ch

Power distribution summary

- DC/DC-based LV distribution

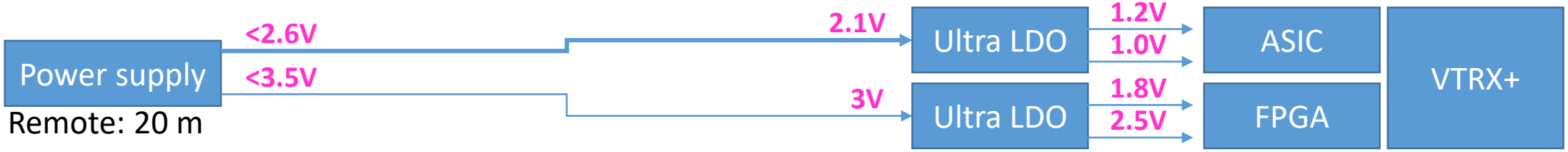
  → Remote power supply distributes 12V with voltage drop over 20 m cables < 0.5V



Channel mW	256-ch FEB W	FEB LV wire mm²	1024-ch detector module W	Module LV wire mm²
44	11.6	1.3	46	5.2

- LDO-based LV distribution

  → Remote power supply distributes 2.1V and 3V with voltage drop over 20 m cables < 0.5V



Channel mW	256-ch FEB W	FEB LV wire mm²	1024-ch detector module W	Module LV wire mm²
48	12.3 (**11.1** + 1.2)	**7.3** and 0.6	50 (**45**+5)	**29** and 2.2

To summarize on FEB with VTRX+ optical RDO interface

- Due to detector partitioning, VTRX+ upstream bandwidth will be largely underused
  → Not a big deal

- Requires a local on-board “intelligence”
  → Clock recovery, downstream data separation, upstream data aggregation

- Local intelligence can be implemented on a low end – low cost FPGA
  → Low to moderate rate SEU effects to be taken into account
  → If case differential IO pins are limited, use high fidelity fan-out for clock and fast commands
    - Rafael, Prisme
  → Requires a dedicated R&D

- FEB to RDO distance unlimited

- Expected power consumption of a 256-channel FEB
  → 11.6 W with on-board or closely coupled DC/DC : 44 mW / channel – extra 14 mW/ch from FPGA / VTRX
    - 5.2 mm^2 wires would be appropriate to distribute required power to entire 1024-channel detector module
    - Location of the magnetic field tolerant bulky DC/DC converters will most probably be problematic
  → 12.3 W without DC/DC regulators : 48 mW / channel – extra 14 mW/ch from FPGA / VTRX
    - !!! 7.3 mm^2 if FEBs are individually powered
    - !!! 29 mm^2 if a common power is delivered to a 1024-channel detector module

Example: powering of FEB with COTS e/o interface

FEB with optical interface: COTS optical FireFly

- FE ASICs are directly interfaced to 4-lane bidirectional parallel optic FireFly transceivers
  - → Requires an “innovative” ASIC interface: Rx line encoding clock and data (sync & async commands)
  - → Plus extra handy features:
    - A low speed embedded ADC for environmental monitoring
    - A GPIO outputs for on-board control

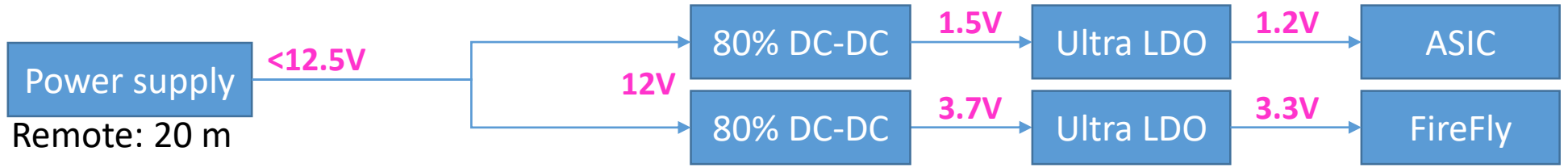
Optical 4 Tx & 4 Rx FireFly from Samtec

- FEB
  - → Radiation hardened ASICs
  - → Low active component count: minimal power consumption
    - ~35-37 mW / channel - 15% increase compared to pure electrical interface
    - 1 mm^2 (DC/DC + LDO) or 6 mm^2 (LDO only) wires to power FEB

Power distribution with bi-directional optical 4-lane FireFly

- DC/DC-based LV distribution

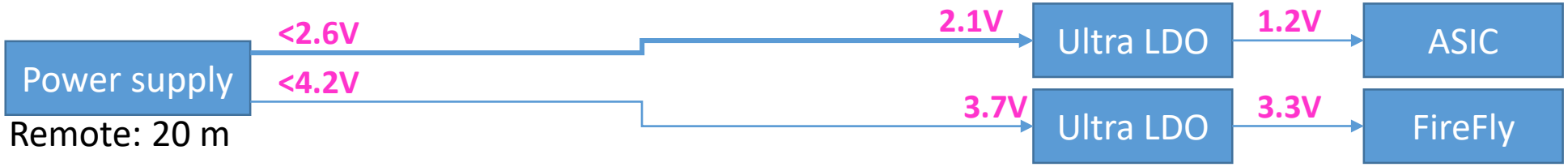
  → Remote power supply distributes 12V with voltage drop over 20 m cables < 0.5V



Channel mW	256-ch FEB W	FEB LV wire mm²	1024-ch detector module W	Module LV wire mm²
35	9	1	36	4

- LDO-based LV distribution

  → Remote power supply distributes 2.1V and 3V with voltage drop over 20 m cables < 0.5V



Channel mW	256-ch FEB W	FEB LV wire mm²	1024-ch detector module W	Module LV wire mm²
38	9.6 (**8.6** + 1.2)	**5.5** and 0.5	39 (**34**+5)	**22** and 1.8

To summarize on “alternative” FEB with FireFly optical RDO interface

- Close to minimal active components: FE ASICs and a bi-directional optical 4-lane FireFly
  - → No on-board intelligence, no aggregation, no clock-fast command distribution
  - → ASIC is seen as a “DAQ unit” – a direct bi-directional connection with RDO
  - → Fastest configuration

- FEB to RDO distance unlimited

- Expected power consumption of a 256-channel FEB
  - → 9 W with on-board or closely coupled DC/DC : 35 mW / channel – extra 5 mW/ch due to FireFly
    - 4 mm^2 wires would be appropriate to distribute required power to entire 1024-channel detector module
    - Location of the magnetic field tolerant bulky DC/DC converters will most probably be problematic
  - → 9.6 W without DC/DC regulators : 39 mW / channel – extra 5 mW/ch due to FireFly
    - !!! 5.5 mm^2 if FEBs are individually powered
    - !!! 22 mm^2 if a common power is delivered to a 1024-channel detector module