Serial powering for the ePIC Silicon Vertex Tracker

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ePIC Electronics & DAQ WG meeting

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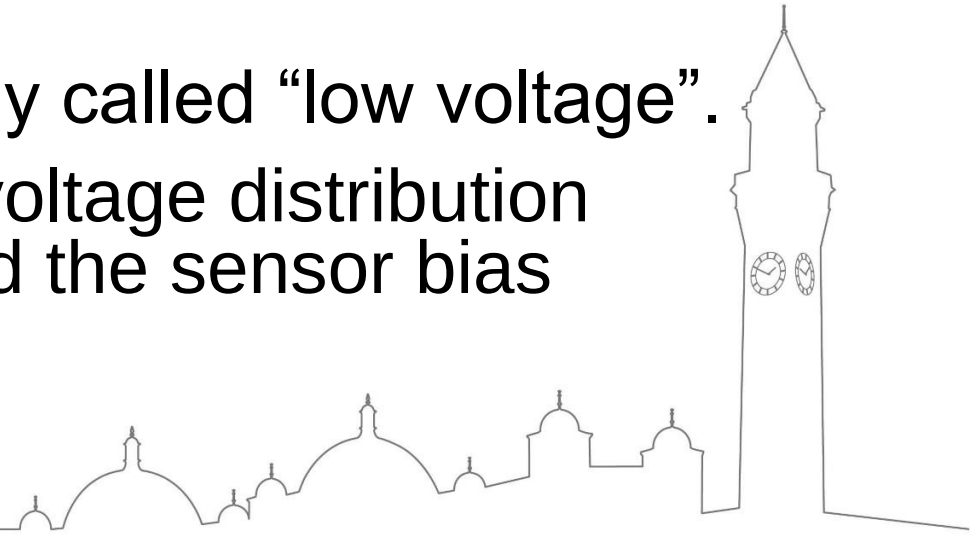
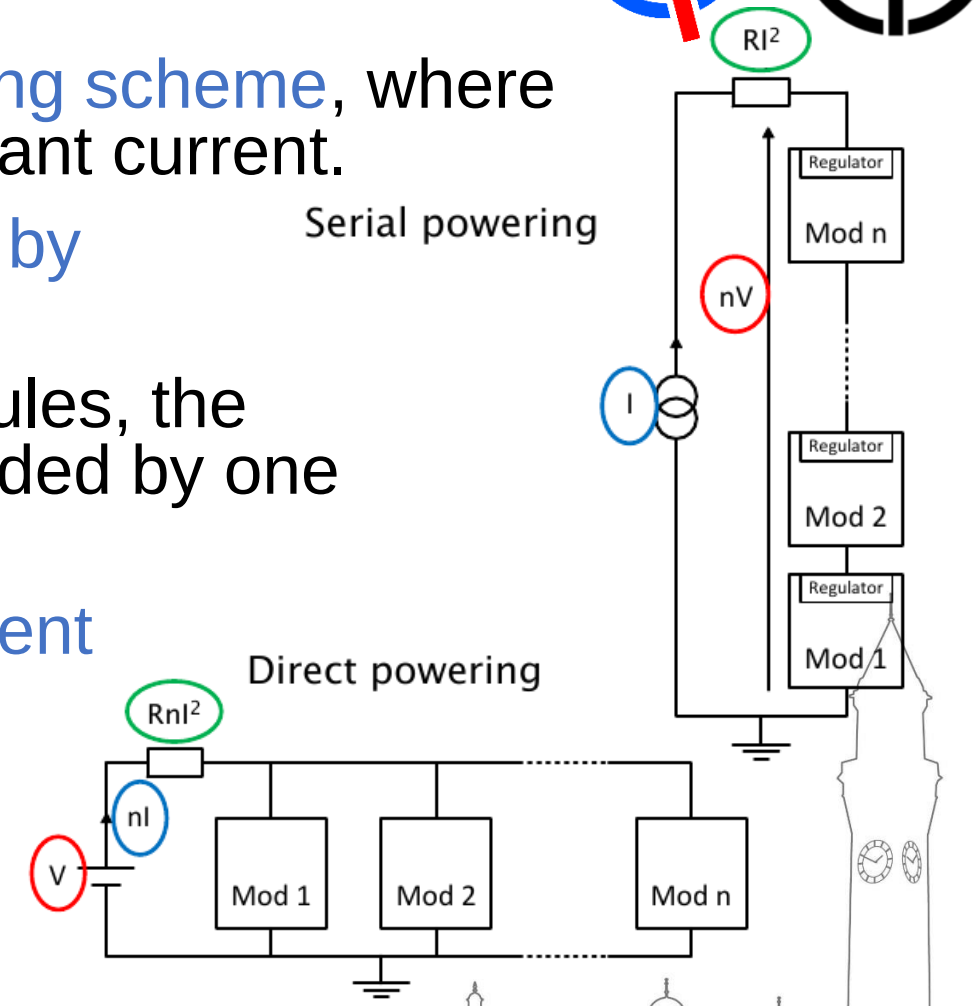
Introduction

- In the following slides a module is the detector's active element, that is the sensor with its readout electronics.
  - It can be a hybrid pixel detector where sensor and readout electronics are two separate entities bump bonded together, or a MAPS detector where sensor and readout electronics are integrated in the same substrate.
- Serial powering is used to power the readout electronics, not to bias the sensor.
- Power to the readout electronics is typically called "low voltage".
- The choice of serial powering for the low voltage distribution impacts the data transmission scheme and the sensor bias scheme.



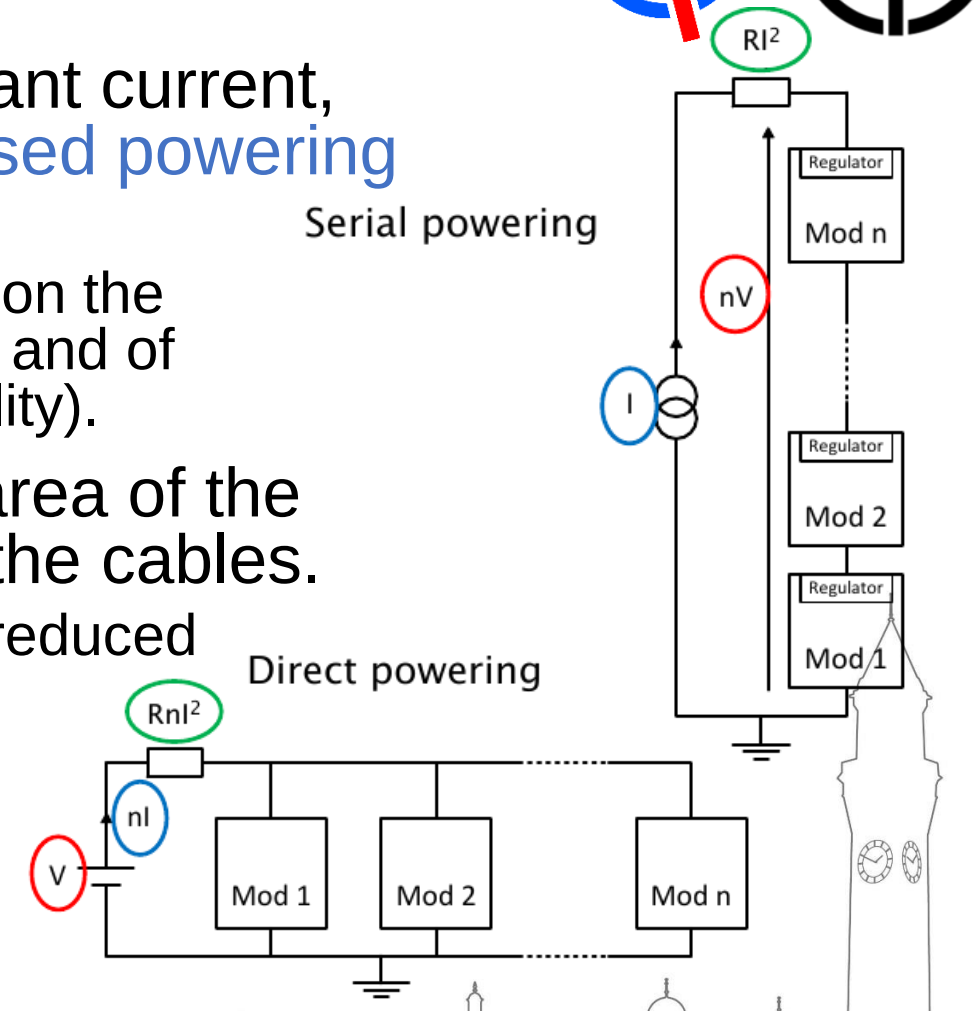
Serial powering basics

- Serial powering is a current based powering scheme, where modules are powered in series by a constant current.
- The current to voltage conversion is done by regulators close to/on module.
- In a serial powering chain made of n modules, the transmitted current is only the current needed by one module, I.
- For n modules powered in series, the current is reduced of a factor n with respect to a direct powering scheme → Higher power efficiency and reduced cable volume.
  - Cable cross-section and the power losses on the cables scale by the same factor.



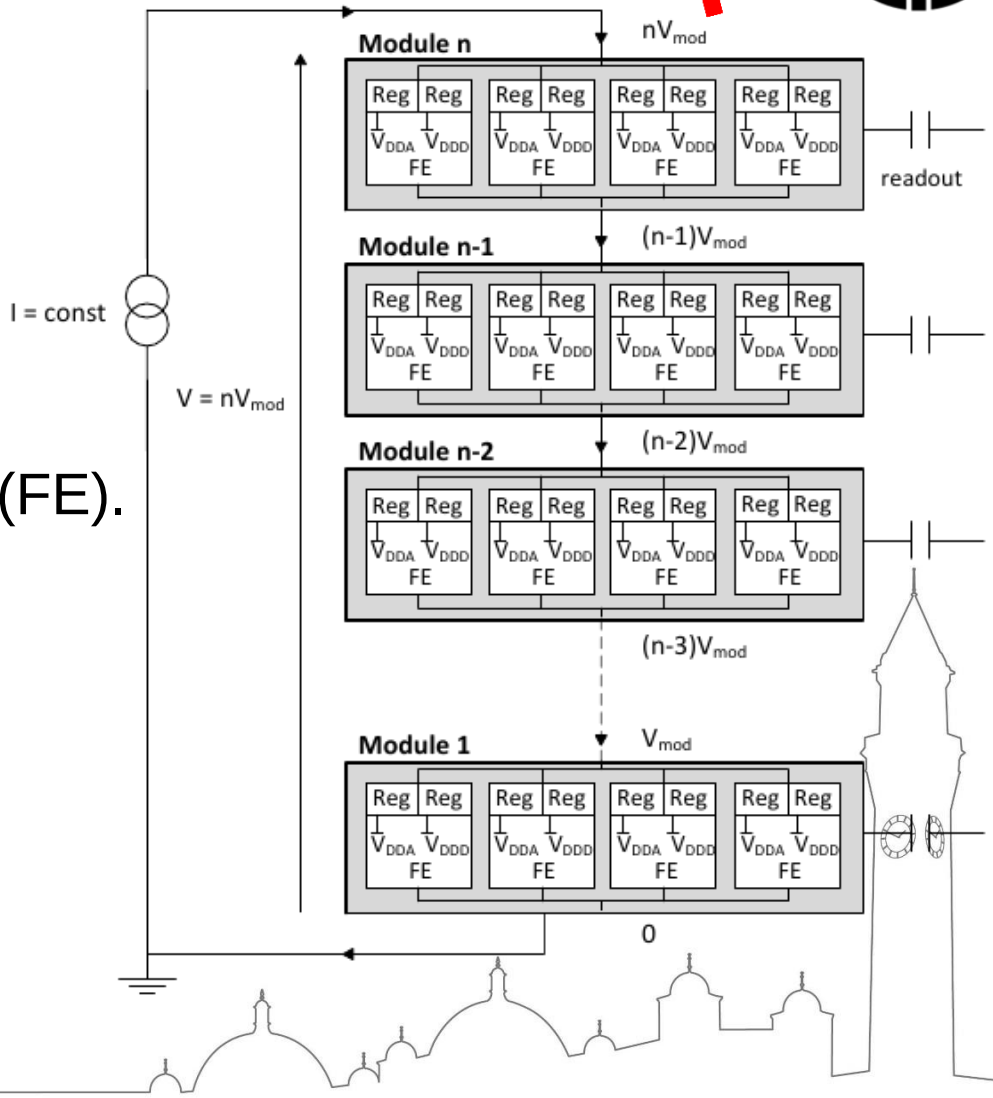
Serial powering basics

- As the modules are powered with a constant current, V_{drop} is not constrained as in a voltage-based powering scheme.
  - It can, in principle, be chosen only depending on the output voltage capability of the current source and of the allowed power density (i.e. cooling capability).
- Higher V_{drop} can be allowed in the active area of the detector to reduce the material budget of the cables.
  - Outside the detector the voltage drop can be reduced to lower the power losses.
- With respect to voltage-based powering schemes (incl. DC-DC), serial powering allows more flexibility in the optimization of material and power efficiency.



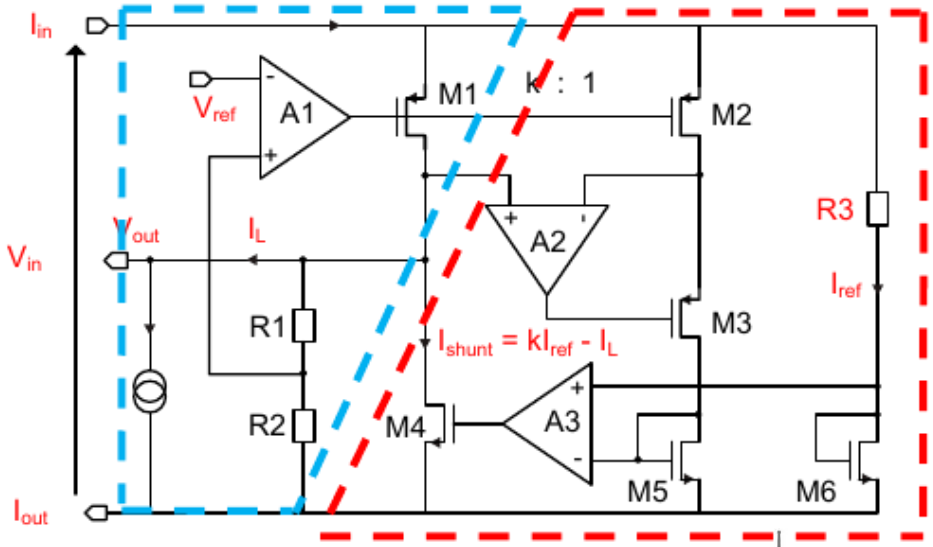
Example: ATLAS ITk detector

- The ATLAS pixel detector at the HL-LHC adopted serial powering (also the CMS pixel detector).
- Each module is made of a sensor bump bonded to a certain number of readout chips.
  - In the sketch, four readout chips per module (FE).
- The current flows in series between modules and in parallel between readout chips on a module.
- In each chip, two shunt-LDO regulators generate the analogue (V_{DDA}) and digital (V_{DDD}) voltages.



Shunt-LDO regulator

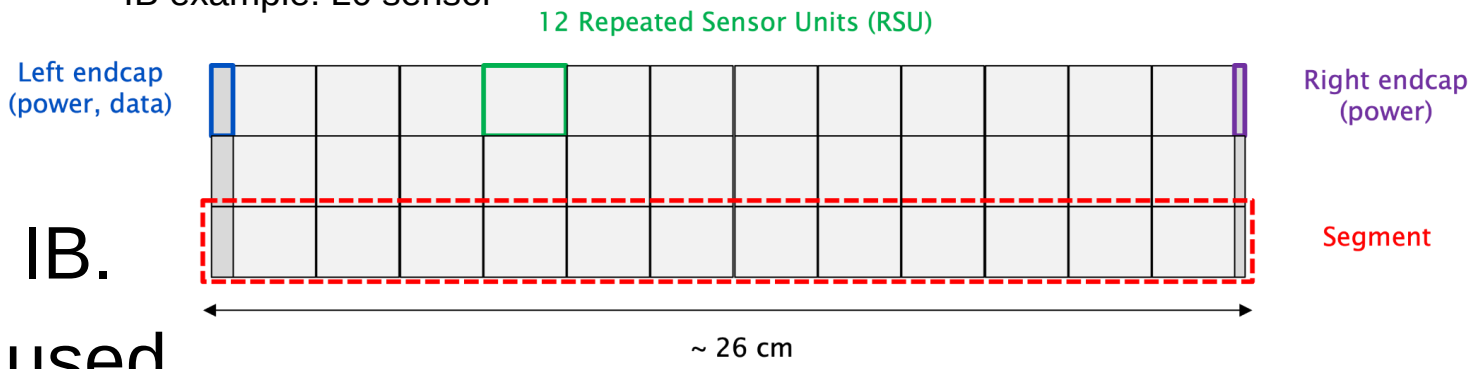
- For this powering scheme, on-chip regulators are needed that can:
  - Operate in parallel
  - Generate different output voltages out of the current supply
  - Shunt additional current in case of device failure.
- The Shunt-LDO regulator was designed to match these requirements.
  - First prototype version in the ATLAS pixel FEI4 chip (180 nm process).
  - Full SP version in the RD53 chip (65 nm process).
- It combines two regulation loops.
  - Shunt regulation circuitry → regulates the current to the chip.
  - LDO (Low Drop Out) regulation loop → generates the voltage for the chip.



Reminder and prerequisites

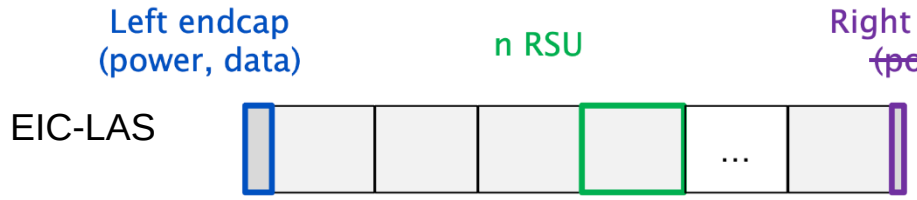
- EIC-LAS is name of MAPS to be used for OB, EE, and HE of SVT. Longer, wafer-scale sensor used in IB.
- Serial powering (SP) to be used for OB, EE, and HE (not IB).

IB example: L0 sensor



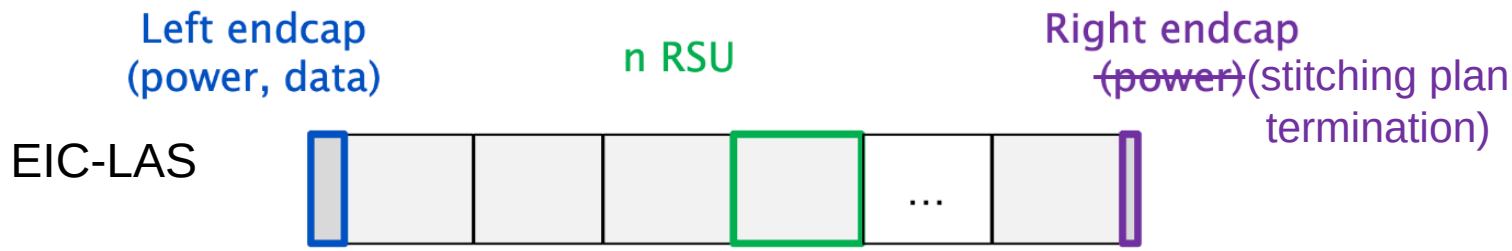
From: https://wiki.bnl.gov/EPIC/index.php?title=Si_Vertex_Tracker

OB	–	Outer Barrel
IB	–	Inner Barrel
EE	–	Electron (going) Endcap
HE	–	Hadron (going) Endcap
SVT	–	Silicon Vertex Tracker



Reminder and prerequisites

- Multiple EIC-LAS needed in a SP chain (reduces material).
- Some redundancy required (e.g. don't want a whole stave in one SP chain, in case chain is lost).
- SP chains need to fit in with flexible printed circuit (FPC) design requirements.
  - FPC needs to be designed with connections for data readout and slow controls (not just powering).



From: https://wiki.bnl.gov/EPIC/index.php?title=Si_Vertex_Tracker

EIC-LAS expected power domains

Power Domains and Currents

Supply purpose	Nets	Voltage [V]	Current [mA]	Pads on LEC	Pads on REC
Services	SDVDD-SDVSS	1.2 to 1.32	227	Yes	Yes
Global analog	GAVDD-GAVSS	1.2 to 1.32	540	Yes	Yes
Global digital	GDVDD-GDVSS	1.2 to 1.32	1369	Yes	Yes
Serializers	TXVDD-TXVSS	1.8	200	Yes	No
Substrate bias	PSUB	−1.2 to 0			

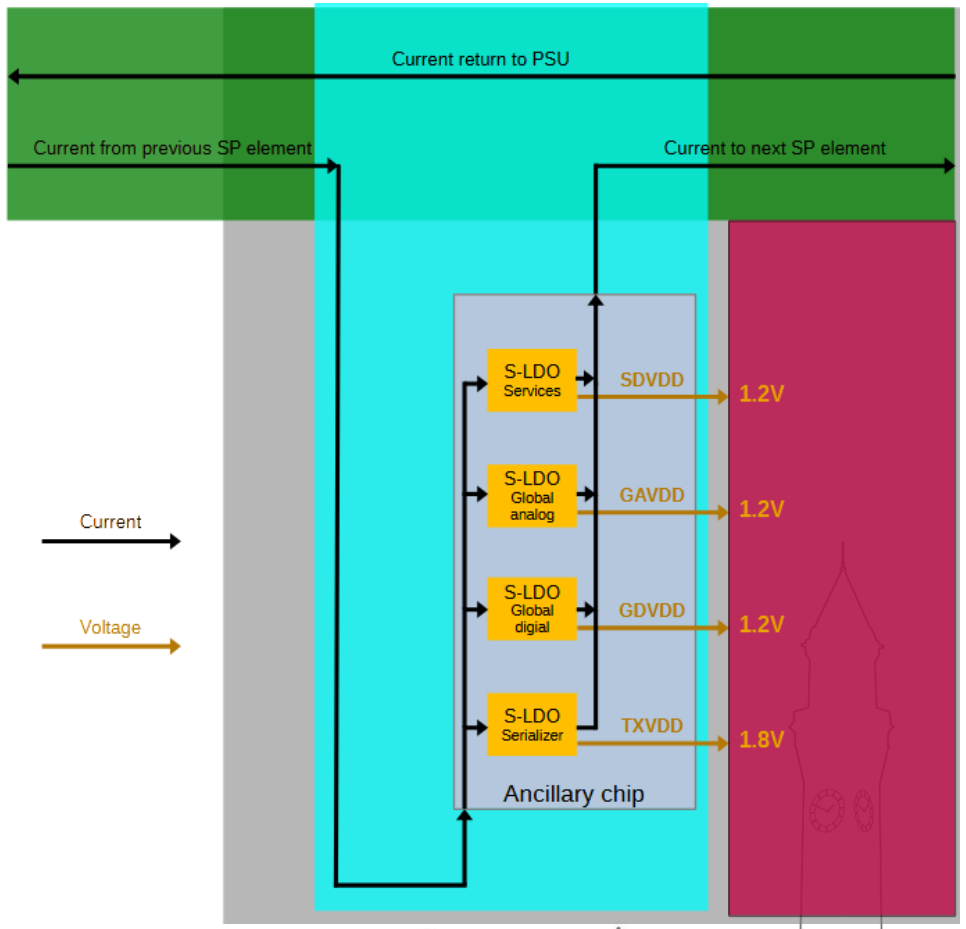
Table 3.11: Power domains of one sensor segment. The substrate bias is common to all the segments composing a sensor. The nominal operating voltage are referred to the potential of the GAVSS input net. The input currents are obtained assuming the maximum estimated power consumption of the LEC and RSU circuits at 25 °C.

From: 20th Nov '23, EP R&D WP 1.2 – G. Rinella, "Design of MOSAIX - ER2 Stitched Sensor Prototype", https://indico.cern.ch/event/1339888/contributions/5680443/attachments/2755393/4797584/20231120-ER2-Stitched-Sensor.pdf

- 3 domains all around +1.2 V.
  - Services
  - Global analog
  - Global digital
- 1 Serializers domain at +1.8 V.
- 1 Substrate bias domain at -1.2 V.

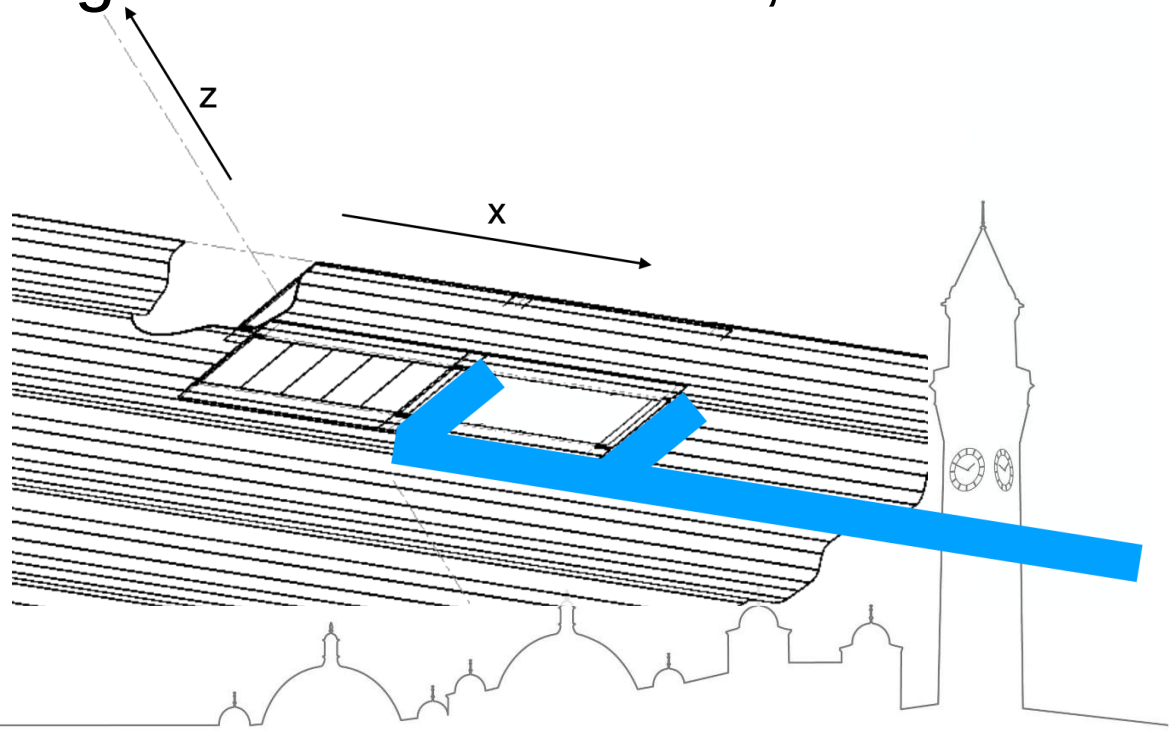
1 S-LDO per (+ve) domain

- Located with an ancillary chip.
- 4 S-LDOs would be needed (in parallel).
  - Services (up to 1.32 V and 227 mA).
  - Global analog (up to 1.32 V and 540 mA).
  - Global digital (up to 1.32 V and 1369 mA).
  - Serializers (up to 1.8 V and 200 mA).
- A S-LDO would be needed to run at 1.2(to 1.32) or 1.8 V and be able to shunt (O)1.4 A.
- What about redundancy?
  - Per EIC-LAS and per SP chain.

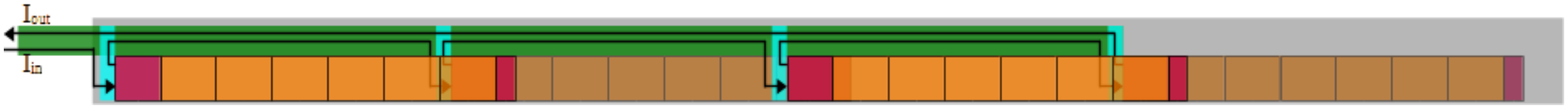


Readout recommends cluster size

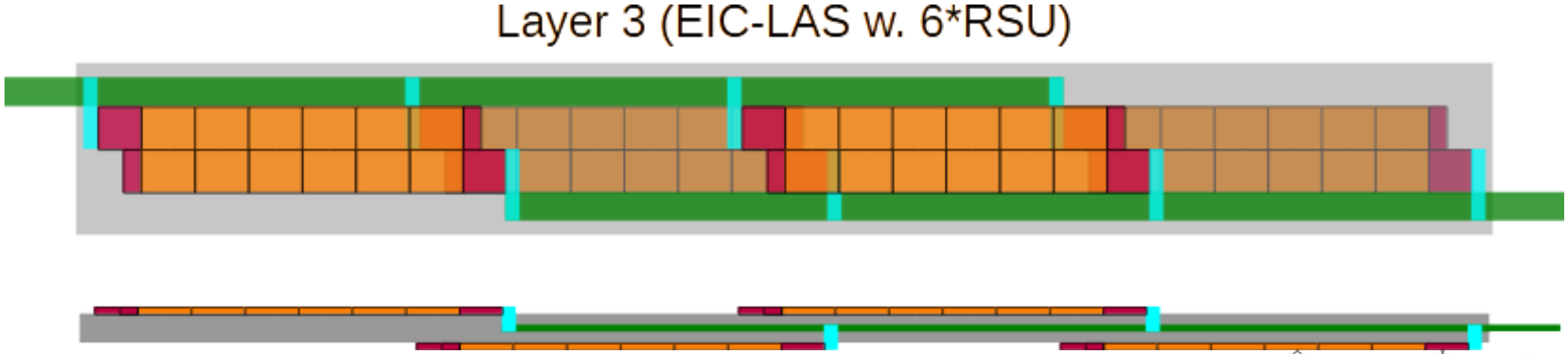
- Recent VTRx+ planning for the readout has showed a preference for clusters of 4 EIC-LAS (each EIC-LAS to have 1 multiplexed data link, for all RSUs, with 4 links available on a single VTRx+).
- (Current) stave designs are considering double-side staves, the width of 2 EIC-LAS.
- FPC designs are preferring clusters 1 EIC-LAS wide (even if interfacing sensors on different sides of the same structure).



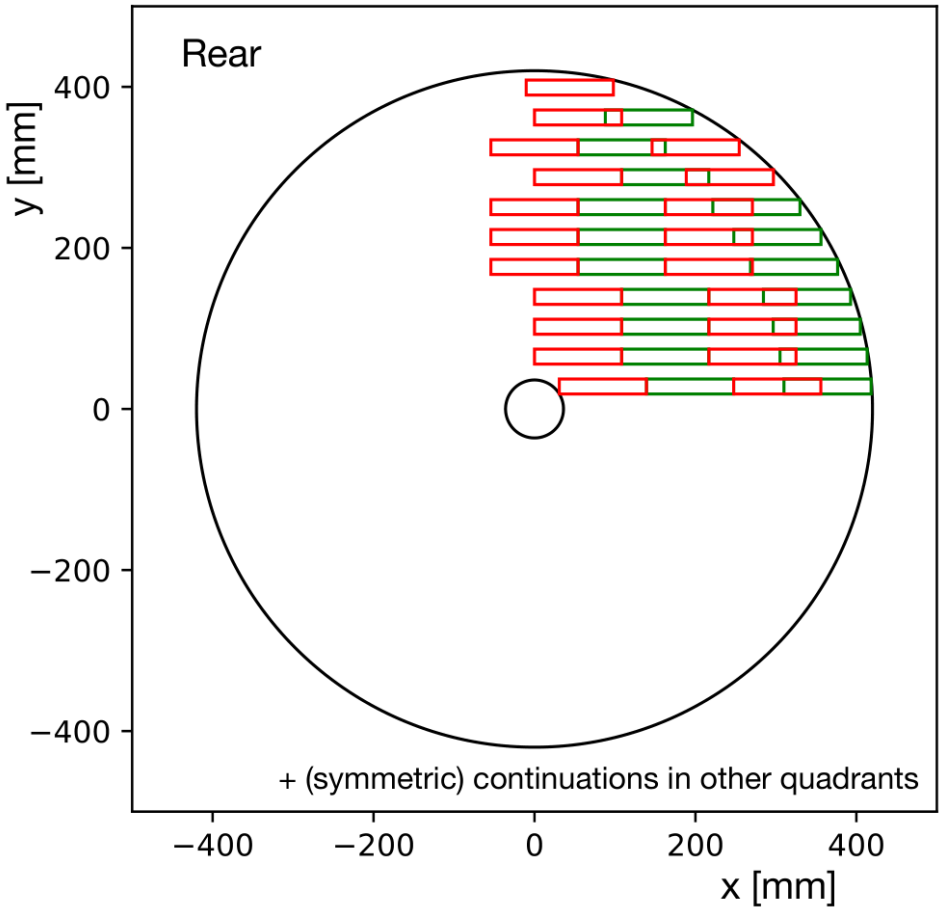
SP in these FPCs



- A serial powering chain could therefore run along a length of a stave (like structure).
- A convenient layout for L3 (with 6 RSUs) could look as follows:



Endcap Disks



Need to consider options when shorter structures are required.

- Larger y coordinates in the plot (←).
- Clusters of < 4 EIC-LAS would be inefficient (less of a benefit from SP).
- Linking neighbouring structures together would increase complexity of the FPC.
  - Multiple FPC designs.
  - Some designs may only be needed in small numbers.

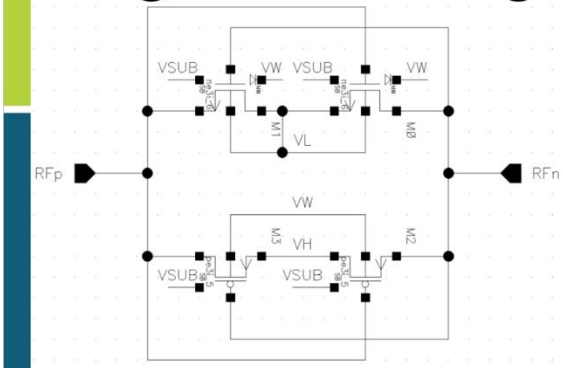
Redundancy options

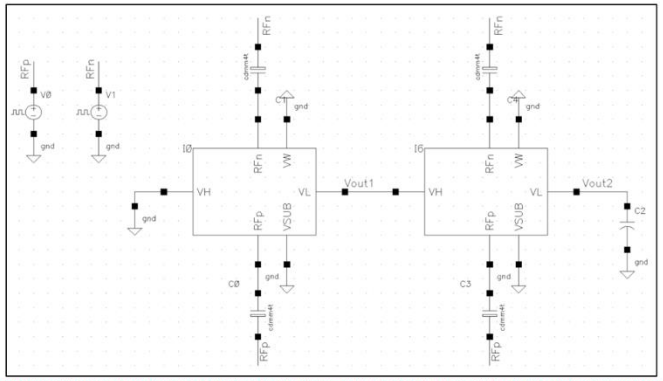
1. 1 S-LDO failure, kills 1 EIC-LAS, but keeps SP chain.
   - 4 S-LDOs per EIC-LAS.
   - If any 1 fails, the EIC-LAS is lost.
   - If all S-LDO can shunt (O)1.4 A, up to 2 (on the same EIC-LAS) can fail before the SP chain is lost.
2. Redundancy for each S-LDO (2 per domain).
   - 8 S-LDOs per EIC-LAS (more material).
   - Master/slave relationship (slave only supplies domain if master has failed).
   - Requires additional circuitry (and material), on top of the additional S-LDO.
   - Any (single) S-LDO failure does not affect the detector performance.
   - 2 S-LDOs (for the same domain) would have to fail before losing an EIC-LAS.
   - Up to 2 domains (on the same EIC-LAS) can fail before the SP chain is lost.

Substrate bias domain

From: 9th Jan ’24, ePIC CM@ANL – G. Deptuch, “EIC-LAS ancillary / support IC”, https://indico.bnl.gov/event/20473/contributions/84985/attachments/51831/88643/ePIC_SVT_MAPS_design_org.pptx

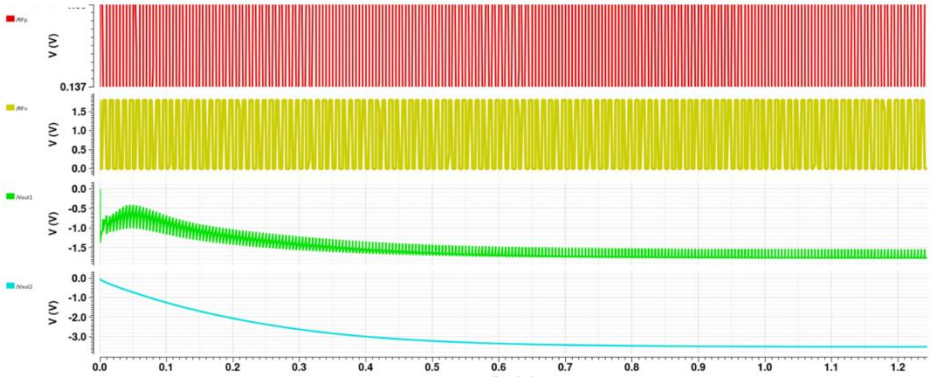
Negative Voltage Generator





Preliminary:

Vout2 = -3.6 V



- The S-LDO configurations only cover the positive voltage power domains.
- A -1.2 V domain is needed for the substrate of the chip.
- Can not be supplied in a parallel powering scheme.
  - Each EIC-LAS in the SP chain will have a difference ground reference.
  - The -1.2 V must be referenced to the specific EIC-LAS’s ground.

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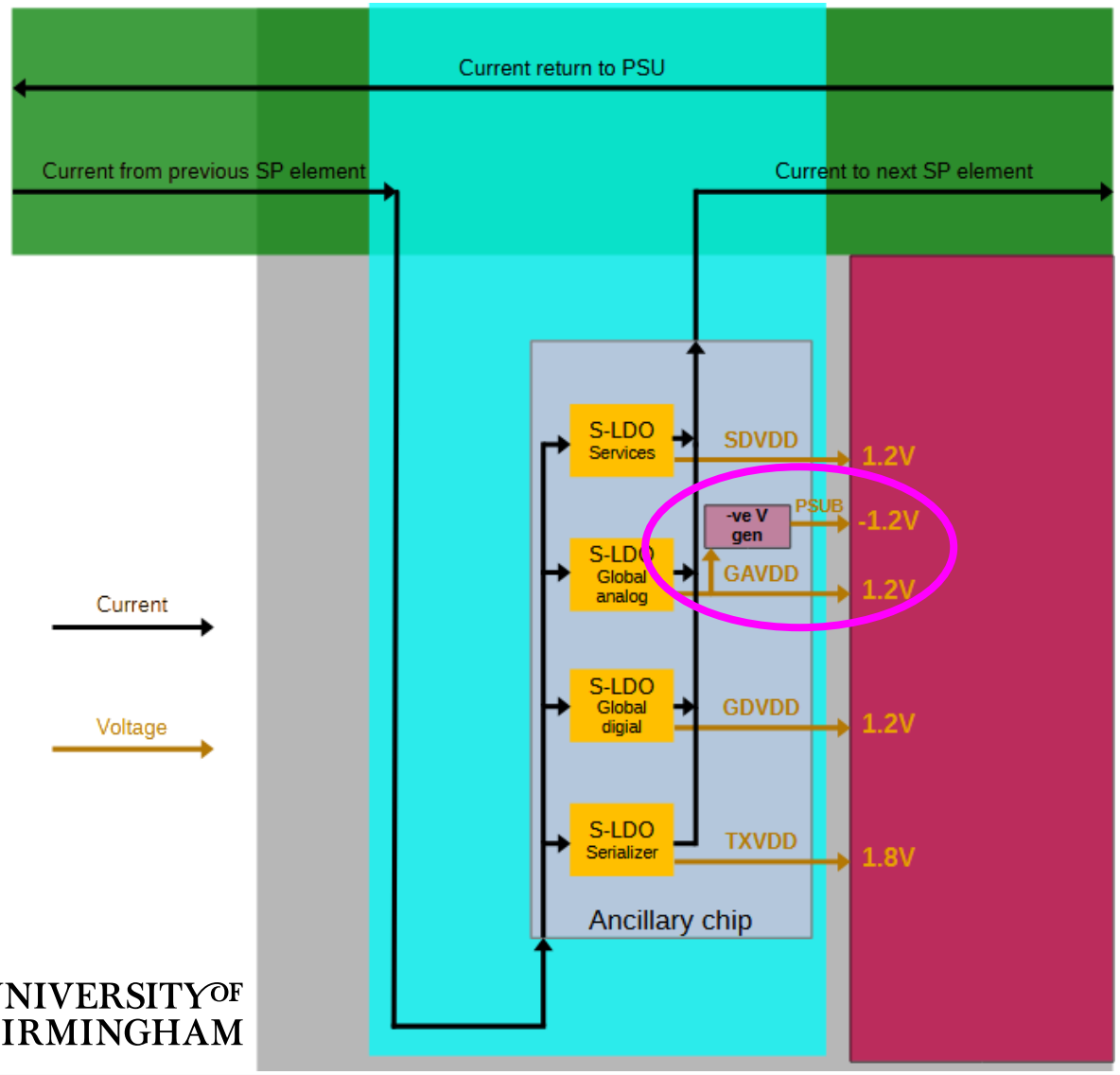
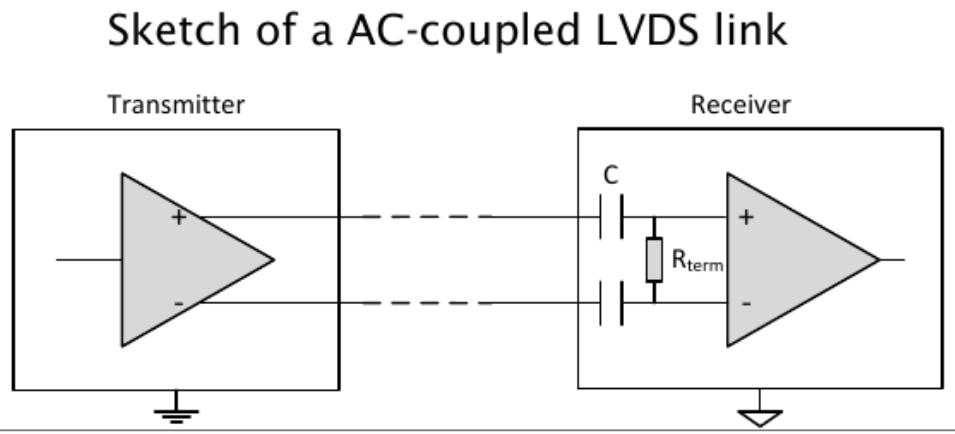
S-LDO config per EIC-LAS

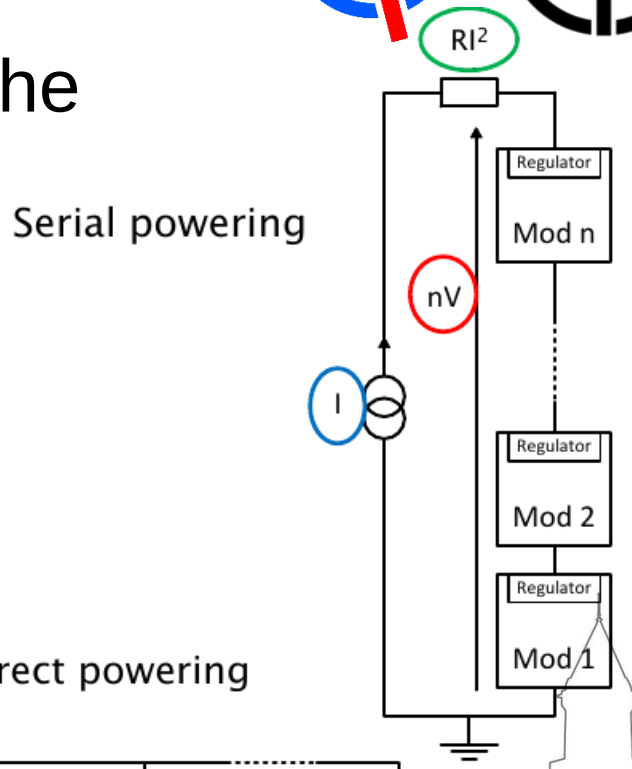


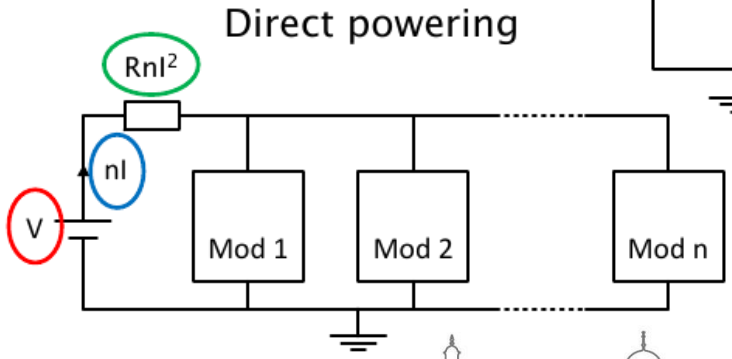
- Basic configuration overview (no redundancy shown).
- Negative voltage generator could (technically) run from any of the 4 S-LDO domain voltages.
  - Shown on Global analog as this is a likely preference.

Serial powering: data transmission

- The voltage across the chain is nV, where V is the voltage on a module.
- Each module sits at a different ground potential.
- AC coupled data transmission required.
  - DC balanced data protocol (e.g. 8b10b).
  - Self-biased receiver inputs to set the common mode voltage.

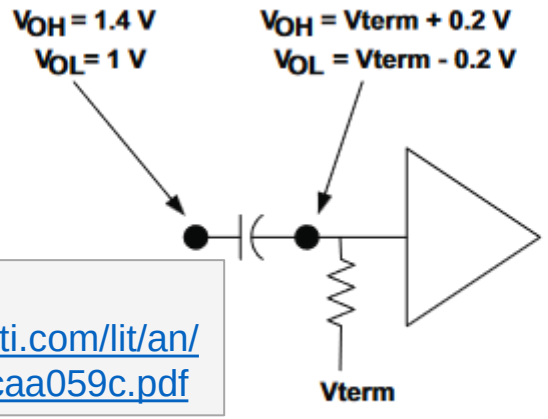






AC-coupled data transmission

- Due to SP (separate ground reference per EIC-LAS), data transmission will need to be AC-coupled (to separate the DC offset from the signal).
- Details of the proposed scheme are still a work in progress and many questions are still to be checked and answered.
- This should only affect the OB, EH, and HH (where the EIC-LAS and SP are used).



From: https://www.ti.com/lit/an/scaa059c/scaa059c.pdf

Figure 1. AC-Coupling to Shift Common-Mode Voltage

Summary

- SP scheme for the ePIC SVT is progressing.
- Many questions still need to be answered.
- Many things need to be balanced with other areas of the SVT:
  - Readout system
  - Chip design.
  - Local mechanics.
  - FPC development.
- The SP requires AC-coupled data transmission.
- IB will not use SP, but direct powering (approximating the ITS3 plan).
  - ITS3 plan to use DC/DCs close to sensor (large material in front of our discs).
  - We are looking for lower material options.

More detail from ePIC CM Jan ‘24

Greater detail can be seen from contributions to the SVT workfest @ the ePIC Collaboration Meeting, Jan ’24 @ ANL (99+% of these slide are from here):

- https://indico.bnl.gov/event/20473/sessions/6736/#20240109
- Specifically, “Basics of serial powering and S-LDO” by Laura Gonella:
  - https://indico.bnl.gov/event/20473/contributions/84989/
- And, “Serial powering for the ePIC SVT” by James Glover:
  - https://indico.bnl.gov/event/20473/contributions/84990/

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Thank you very much!

Any questions?

Additional (support) slides

Background Studies

Brings together material from multiple previous meetings, in particular:

- 30th Jan ’23, SC meeting – L. Gonella, “Powering scheme for the ePIC SVT”, https://indico.bnl.gov/event/18202/
- 29th Mar ’23, UK SVT SP meeting, https://indico.cern.ch/event/1269506/
- 8th Aug ’23, SVT meeting – P. Jones, “Update on outer barrel and endcaps (disks) tiling study”, https://indico.bnl.gov/event/20219/
  - Updated, 22nd Aug ’23, SVT, https://indico.bnl.gov/event/20336/
- 19th Jul ’23, EIC-UK WP1 – J.Glover, “Status and plans for powering studies - updates on sensor design”, https://indico.bnl.gov/event/19981/
- 22nd Aug ’23, SVT meeting – E. Sichtermann, “Update on disks and tiling”, https://indico.bnl.gov/event/20336/
- 14th Nov ’23, SVT meeting – J. Schambach, “SVT Readout”, https://indico.bnl.gov/event/21207/
- 20th Nov ’23, UK EIC-LAS & S-LDO discussion, https://indico.bnl.gov/event/21215/
- 28th Nov ’23, SVT meeting – J. Glover, “Outer Barrel Layout Considerations”, https://indico.bnl.gov/event/21355/
- 28th Nov ’23, SVT meeting – E. Sichtermann, “Update on disks”, https://indico.bnl.gov/event/21355
- 12th Dec ’23, SVT meeting – J. Glover, “Serial powering architecture”, https://indico.bnl.gov/event/21518/
- 9th Jan ’24, SVT workfest @ ePIC CM – L. Gonella, “Basics of serial powering and S-LDO”, https://indico.bnl.gov/event/20473/contributions/84989/
- 9th Jan ’24, SVT workfest @ ePIC CM – J. Glover, “Serial powering for the ePIC SVT”, https://indico.bnl.gov/event/20473/contributions/84990/

Power consumption

- 4 S-LDOs (domains):
  - Services (up to 1.32 V and 227 mA) → ~0.30 W
  - Global analog (up to 1.32 V and 540 mA) → ~0.71 W
  - Global digital (up to 1.32 V and 1369 mA) → ~1.81 W
  - Serializers (up to 1.8 V and 200 mA) → ~0.36 W
- 1 extra domain for substrate bias.
  - -1.2 V at < 1 mA → ~1 mW

Total ≈ 3.2 W

- These power values are assumed to be for an entire ITS3 ER2 segment (12RSUs with both endcaps).
  - How does this fit with power density estimates given so far?
  - How much does this reduce for fewer RSUs (as with the EIC-LAS)?
- Some additional power will be used for our ancillary chip (S-LDOs, negative voltage generator & multiplexer).

Ground reference per EIC-LAS

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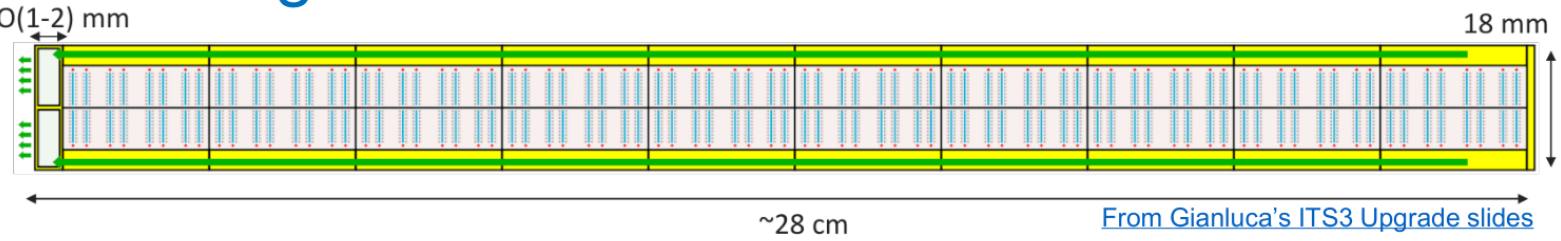
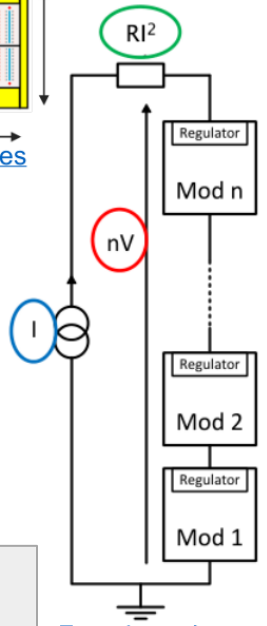
Things to remember.



From Gianluca's ITS3 Upgrade slides

- Serial powering (SP) requires all modules in the SP chain to have a different ground reference to the other modules in the chain (GND of Mod_N becomes V_{in} of Mod_{N+1}), with only the final module in reference to the power supply ground.
- Each RSU in the MOSS is not electrically isolated, therefore the whole MOSS must have the same GND reference.
  - ∴ The 2 endcaps cannot be in series to each other!
  - How do you get power to both endcaps (in a SP scheme)?



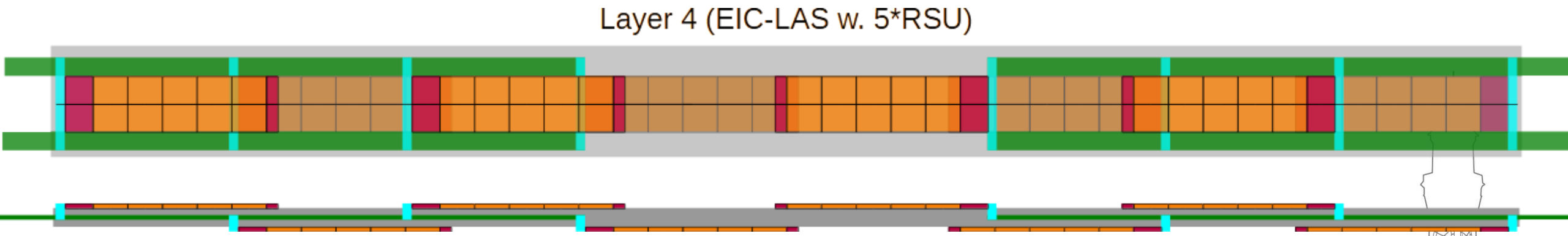
From Laura's EIC SC slides

From: 19th Jul '23, EIC-UK WP1 – J.Glover, "Status and plans for powering studies - updates on sensor design", https://indico.bnl.gov/event/19981/contributions/78770/attachments/48692/82811/23-07-19_Serial_Powering_JGlover_V3.pdf

- 1 of the reasons why EIC-LAS should contain fewer RSUs than ITS3.
- Explains issue of ground reference per Mod (EIC-LAS) in a SP chain.
- Based on information from ITS3's ER1 submission (not ER2).

Longer staves

- To optimise the utilisation of readout links and minimise the material needed for SP chains, lengths of 4 EIC-LAS are optimal.
- This may lead to needing some overlap of RSUs to get to the best stave lengths (even if RSUs per EIC-LAS are reduced).



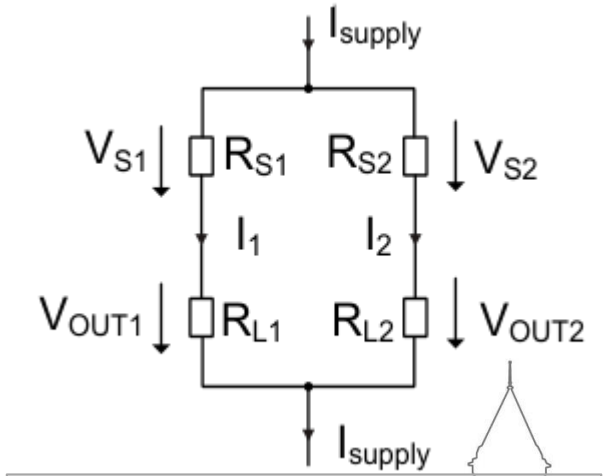
Serial powering: sensor biasing

- The voltage across the chain is nV, where V is the voltage on a module.
- Each module sits at a different ground potential.
- A group of sensors can be powered in parallel, i.e. sharing the same bias line + return, if the difference between operational voltage and breakdown voltage is larger than the total voltage drop in the chain.
- This is the case for planar sensors in hybrids pixel detectors biased to 100s of volts.
- This is not the case for MAPS detectors where the sensor is biased to only a few volts. Therefore, 2 options are available:
  - Direct powering of each sensor, required one floating supply channel per MAPS sensor.
  - Generate the sensor bias from the low voltage.

Shunt-LDO regulators in parallel

- The Shunt-LDO has an ohmic I-V characteristics → safe operation of Shunt-LDO regulators connected in parallel.
  - Even for different values of R_{in}, i.e. different R3
- More robust design against process variation and mismatch.
- Differences in the value of R3 lead to different shunt current values but do not destroy the regulator.
- Shunt-LDO regulators can be placed in parallel even if they generate different output voltages: the difference between their output voltages is compensated by the $V_{dropout}$ across the pass transistor of the LDO regulator, M1.
- Finally, should one of the parallelly placed regulators fail, the extra current can be shunted by the other regulators.

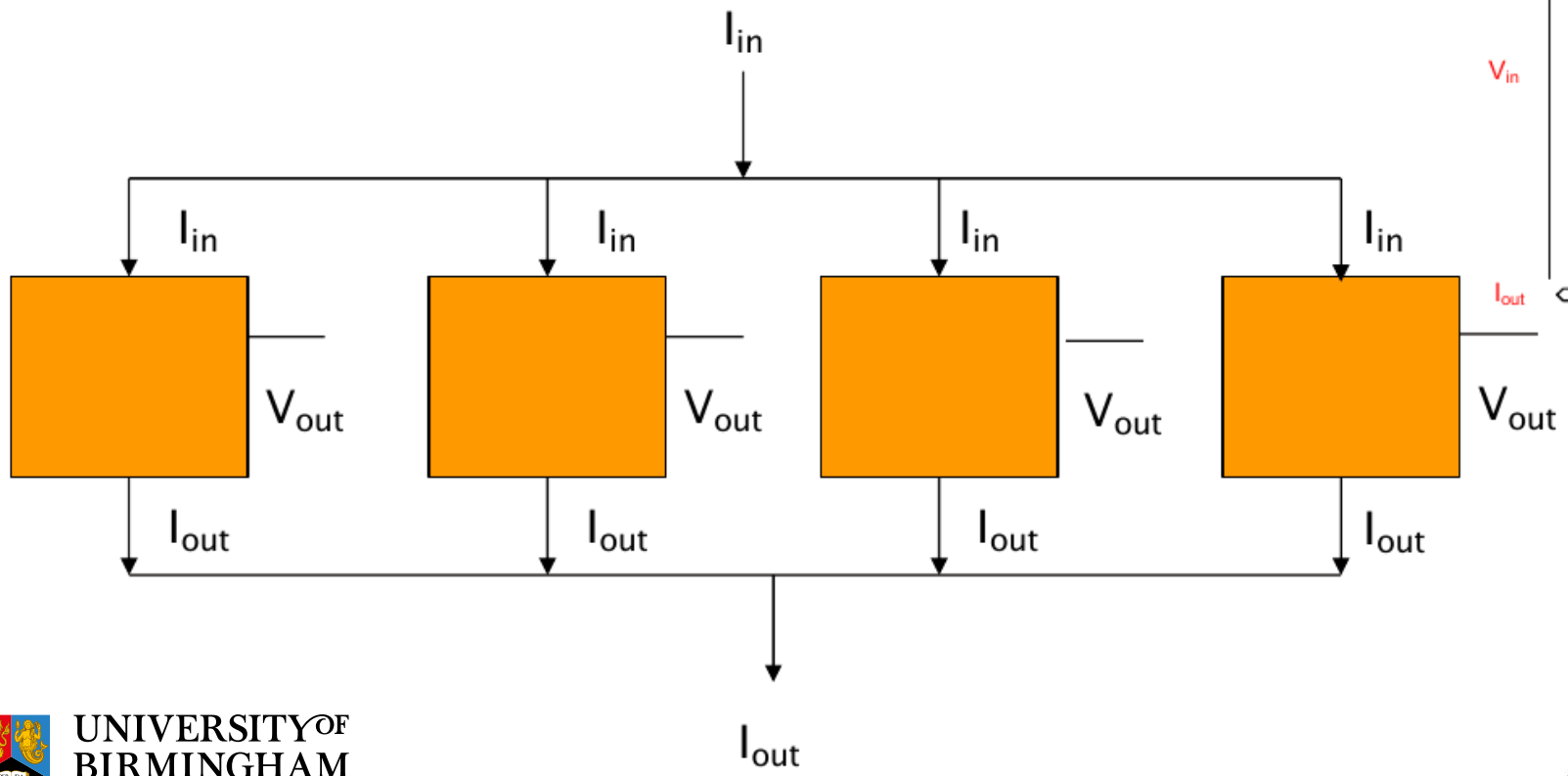
$$R_{in} \approx \frac{V_{in}}{I_{in}} \approx \frac{R3}{k}$$

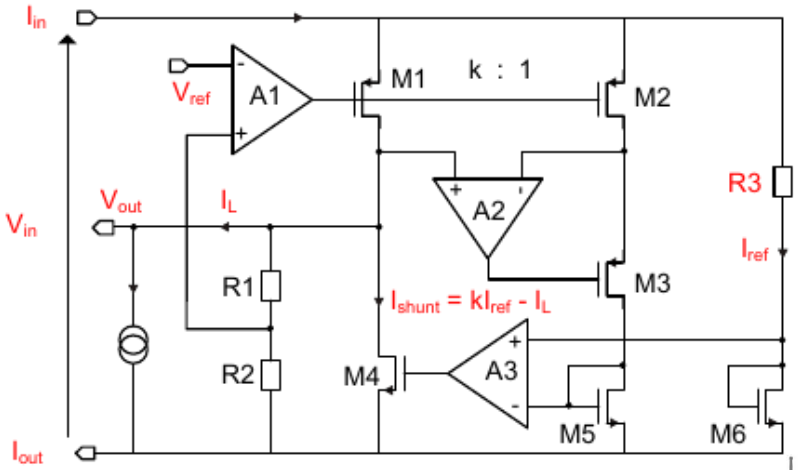


$V_{OUT1} > V_{OUT2}$
$V_{S1} < V_{S2}$
$V_{OUT1} + V_{S1} = V_{OUT2} + V_{S2}$

Shunt-LDO regulators in parallel

- Parallel connection means that I_{in} and I_{out} are in parallel, not V_{out}.





S-LDO Literature

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