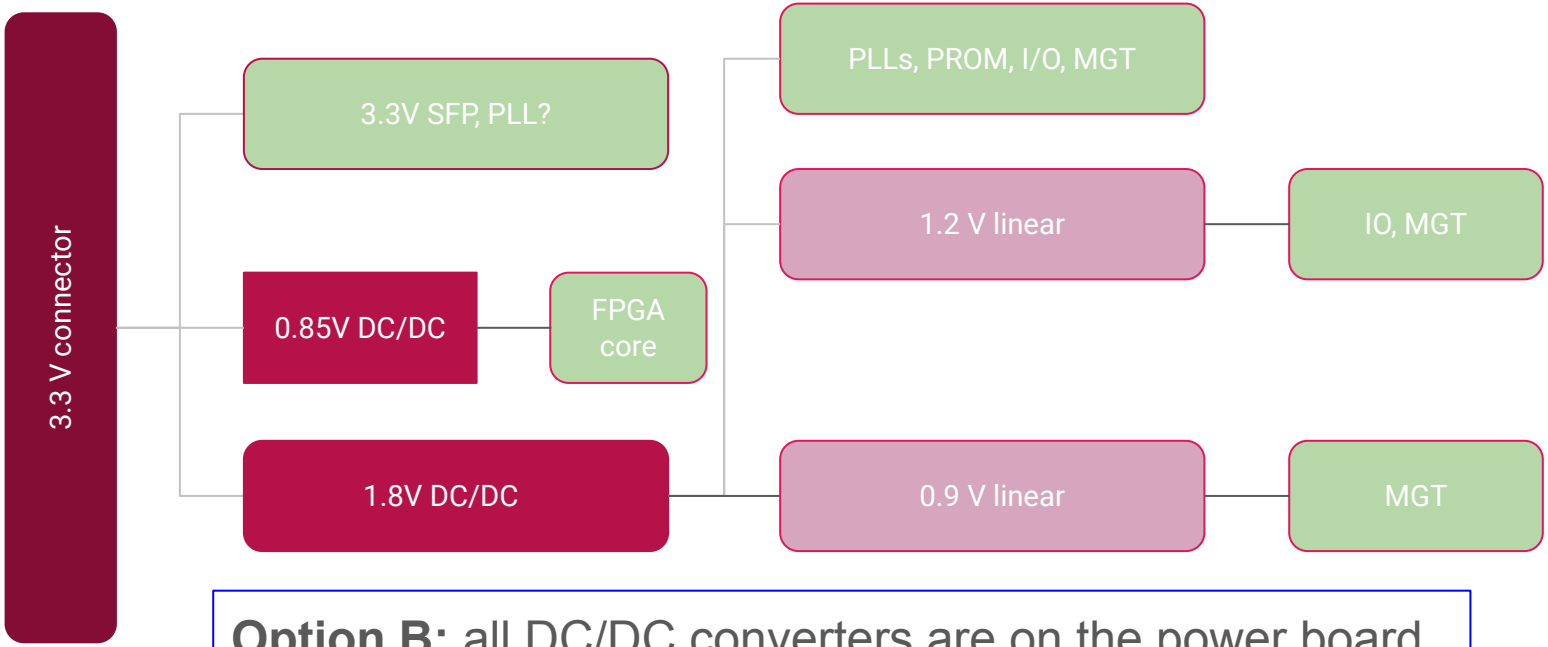
Quick thoughts about the FTOF Power Scheme

- we will have 2 boards (likely on top of each other in a sandwich)
  - Power Distribution Board
    - LV power (1.2V) for the ASICs (DC/DC)
      - 16 ASICs x 1024 x 1 mW/ch ⇒ **16.4 W** (minimum!)
    - LV power for the RDO components
      - don't know yet ⇒ **assume 4-8 W**
      - we'll measure all the currents using the ppRDO so we'll know precisely
  - Readout Board (RDO)
    - LV power for the FPGA and other components
      - 3.3V – SFP, PLL
      - 1.2V – main I/O to ASICs
      - 1.8V – local components, PROM, etc
      - 0.9V – MGT (FPGA transceivers)
      - 0.85V – core FPGA voltage
      - …complicated…
      - BTW, ppRDO project couldn't wait for DC/DC converter decision so we used linear regulators

FTOF RDO Power Distribution Sketches

Option A: 3.3V DC/DC converter on Power Board, ALL others on RDO (as shown)



Option B: all DC/DC converters are on the power board so we supply 3 voltages to the RDO: 3.3, 1.8, 0.85

Comments

- we'll use ppRDO to precisely measure various RDO currents (mid 2024)
- we have other constraints
  - space – DC/DC converters are large due to coils
  - cooling – the biggest problem
    - low mass requirement – no large cooling fins, etc
    - efficient DC/DC converters are hoped for for the largest power needs
      - linear regulators are assumed to be good enough for the low power devices on the FPGA (TBD)
  - radiation tolerance
    - I think this is less of a problem but we need to know/measure the parts
- IR drop on the cable needs to be taken care of
  - especially because all the components (e.g. ASICs vs RDO) won't be powered up at the same time, or they might die, be turned off, etc
- we are hoping for a common EPIC-wide decision
  - and further radiation tolerance testing…