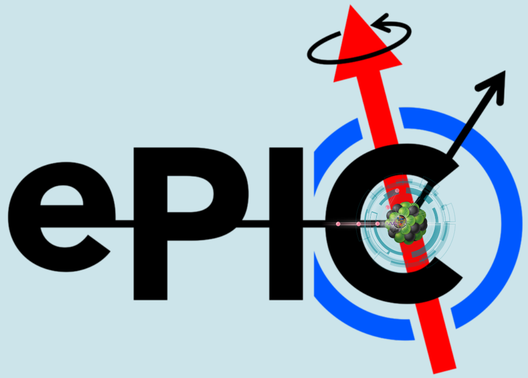


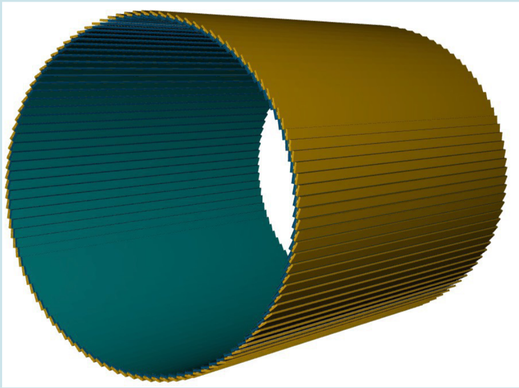
TOF

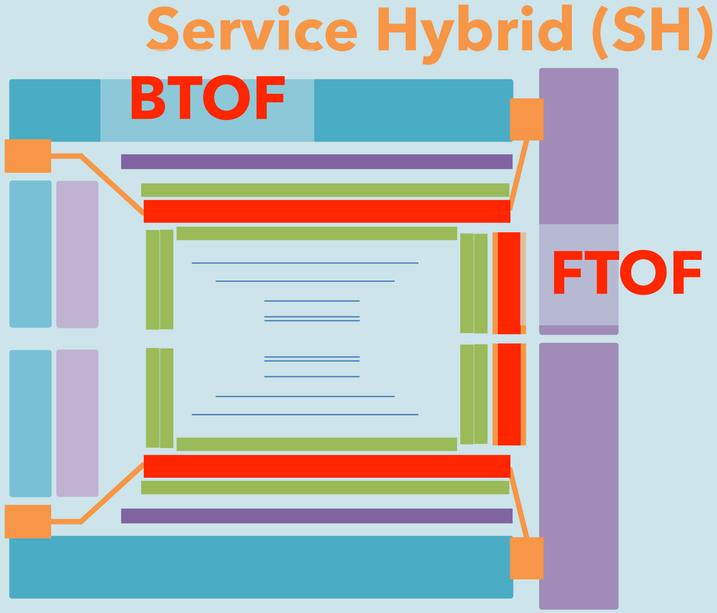
Strategy toward TDR

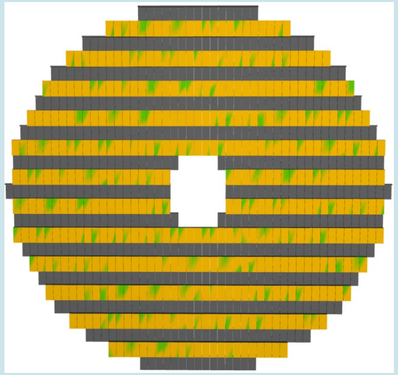
Satoshi Yano on behalf of TOF-DSC

PID meeting on 02/23/2024

Recap of BTOF and FTOF

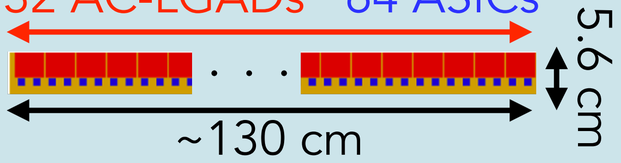


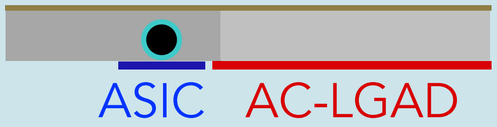




BTOF Module

32 AC-LGADs 64 ASICs

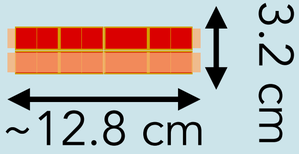


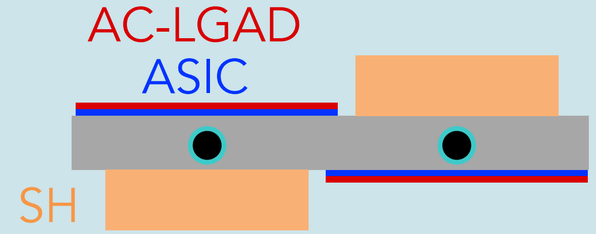


Required performance
Timing resolution ~ 30 ps
Spatial resolution ~ 30 μm

FTOF Module

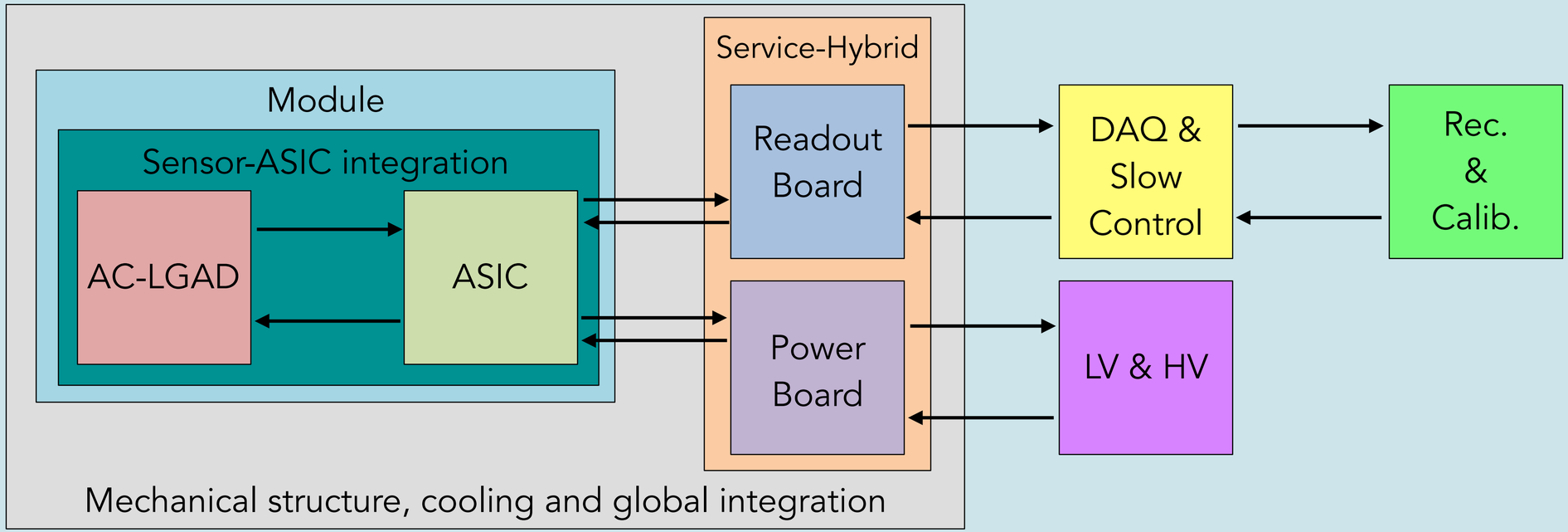
16 AC-LGADs 16 ASICs





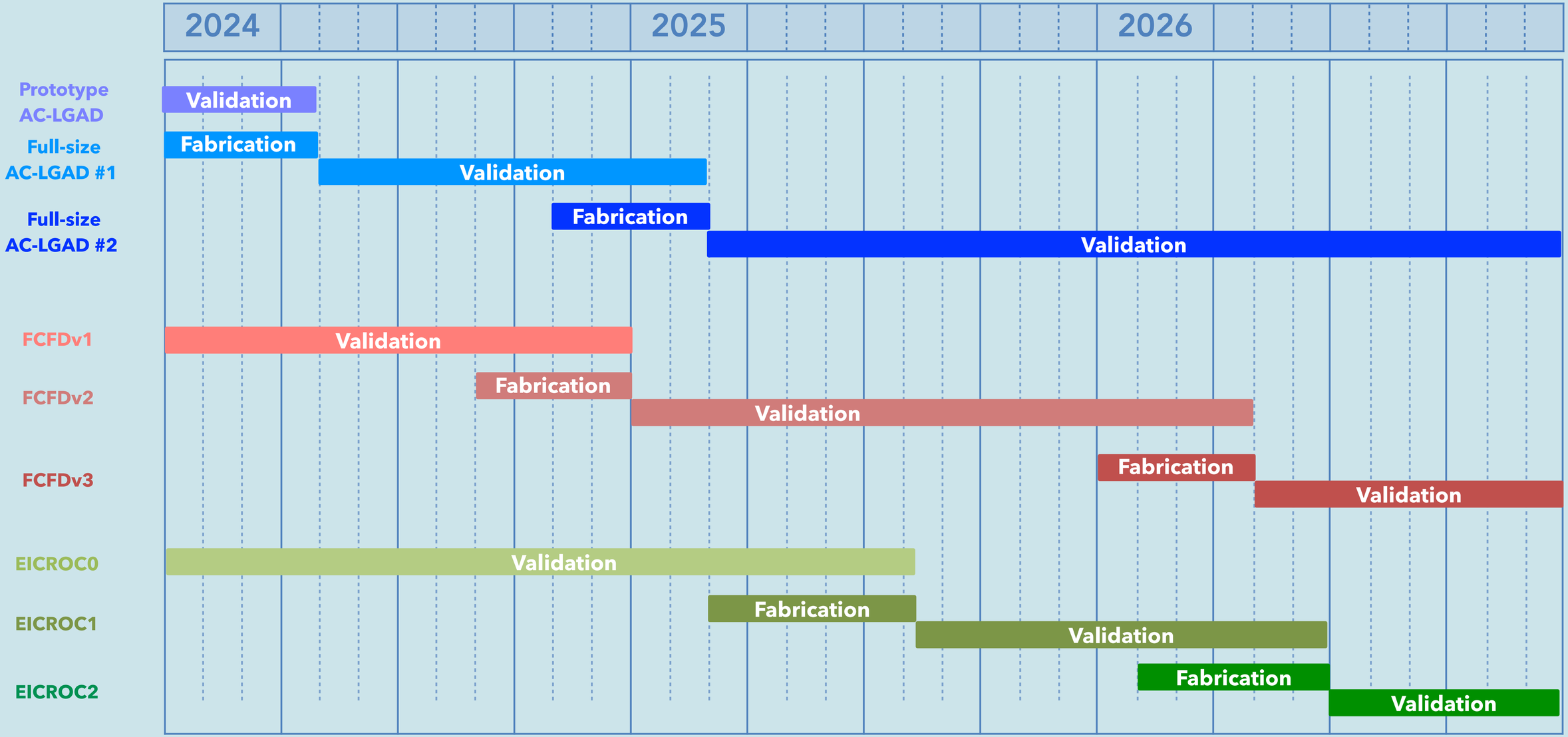
- Strip-type and pixel-type AC-LGAD are used for BTOF and FTOF, respectively
- FCFD and EICROC are used for strip-type and pixel-type AC-LGAD, respectively
- BTOF SH is placed in a different place from sensor+ASICs, but FTOF SH is placed in front of sensor+ASICs

Summary of TOF-DSC TDR

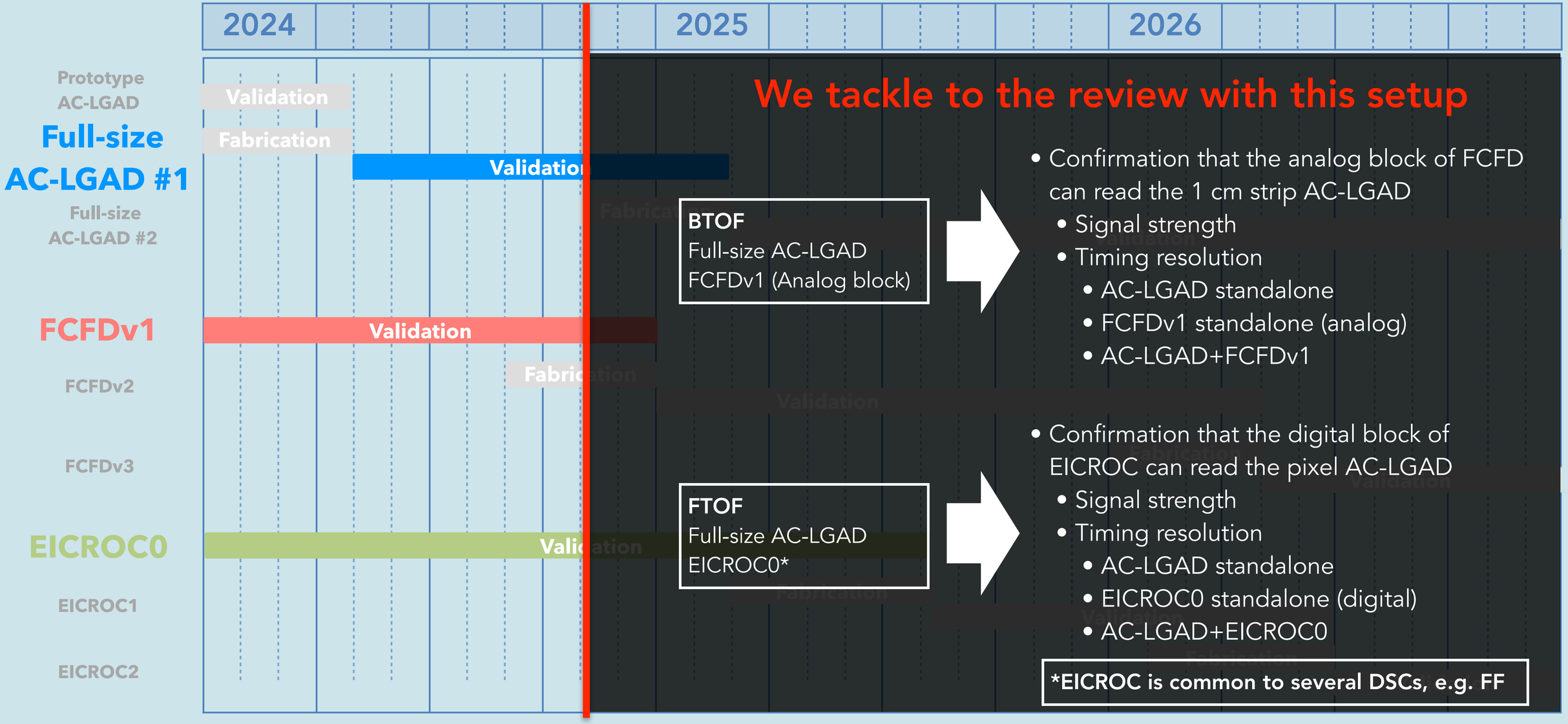


- **Barrel-TOF (BTOF)**
  - Strip-type AC-LGAD
  - ASIC (FCFD)
  - Sensor-ASIC integration
  - Module
  - Service-Hybrid
  - Mechanical structure
  - Global integration
- **Forward-TOF (FTOF)**
  - Pixel-type AC-LGAD
  - ASIC (EICROC)
  - Sensor-ASIC integration
  - Module
  - Service-Hybrid
  - Mechanical structure
  - Global integration
- **Common system**
  - DAQ
  - Cooling
  - Software (Rec. & Calib.)
  - HV & LV
  - Slow control

Schedule of sensor and ASIC



Schedule of sensor and ASIC



Strategy for the TDR (ASIC)

- BTOF digital block demonstration is in need (a concern)
  - It is important to show that "we can't show it now, but we will be able to do it shortly”
  - It is necessary to fully understand and demonstrate the individual characteristics in pre-TDR
    - Characteristics of sensor, FCFD's analog block, and the combined performance
  - The FTOF study will help to corroborate that the BTOF readout is possible
    - Successful signal readout of FTOF means "the AC-LAGD → analog → digital chain is understood and it is under control"
  - Investigating the availability of other ASICs (e.g. HGCROC) is also important

- The beam test at DESY is scheduled for June
  - It is a good opportunity to study the performance of the sensors and ASICs in a realistic environment
  - MIP beam is mandatory to evaluate realistic performance
  - Before the beam test, the lab tests, e.g. radiation source and IR laser, are necessary
    - Gain uniformity, temperature dependence of gain, timing resolution, spatial resolution, and power consumption

Strategy for the TDR (Module Assembly)

- Manufacturing a long (~1.3m) FPC for the BTOF stave is a concern
  - This is an important element to introduce in the TDR because there are not many examples of such a long FPC being utilized in HEP
  - It is necessary to specify the required performance and demonstrate that we have the experience/technology to make it
  - FPC R&D is covered by eRD109 (Nara Women's University and RIKEN, which have experience in developing 1.3m FPC with a low-mass (O(1%) X/X0) for sPHENIX, have agreed to support the development)

- Sensor-ASIC integration
  - Several bonding strategies are planned, e.g. bump bonding, wire bonding, and interposer
  - It is important to introduce that these methods can be applied to TOF from several points of view
    - It is needed to understand the application limits of each method, e.g. bump bonding capability
  - At least the first design of the interposer is required in pre-TDR

- Modules
  - It is necessary to show how each component is attached and the total amount of material budget is acceptable

Strategy for the TDR (Cooling+Service Hybrid)

- Cooling system
  - It is necessary to finalize the evaluation of power consumption and the tolerable temperature range of each component
  - It is necessary to determine the cooling method of BTOF SH (water cooling is used for Sensor + ASIC)
  - A long and a long-winding cooling pipe are used for BTOF and FTOF, respectively, so it is needed to check the difference in cooling capacity between the inlet and outlet

- SH design
  - Data rate and power distribution scheme should be designed
  - It is necessary to show the data rate and the processing power
  - If possible it is nice to show the data stream results of AC-LGAD→EICROC→FPC→FPGA data chain

Strategy for the TDR (Software)

- Tracking reconstruction
  - Realistic TOF structure has been implemented in the current simulation
  - FTOF material budget will be modified to a more realistic one
  - Realistic positioning resolution will be implemented with the coming beam test results (June)
  - Support structure for the wiring between modules to SHs of BTOF will be implemented

- Particle Identification
  - TOF PID LUT is under preparation and its first version will be ready in a few weeks
  - Realistic timing resolution will be implemented with the coming beam test results (June)
  - Hit positioning dependence of the PID performance will not be in time for pre-TDR, but we hope in the TDR

Summary of Pre-TDR Planning

- **Simulation and reconstruction:**
  - Tracking
  - PID

- **R&D:**
  - Sensor: new HPK production and Characterization, simulation, irradiation
  - Sensor-ASIC integration: interposer for BTOF, hybridization for FTOF pixel sensor-ASIC
  - ASIC: EICROC0/1, FCFDv1, HGCROC
  - PCB: Low-mass flexible Kapton
  - Service Hybrid: Readout board + Power board
  - Module structure: Low-mass CF structure for BTOF module

eRD112 (286k$ in FY24) for 60%

eRD109 (390k$ in FY24) for 60%

- **PED:**
  - BTOF and FTOF support structure
  - BTOF and FTOF module preconstruction

Backup

AC-LGAD FY24 R&D Proposal

- Optimized sensor design and final prototypes that meet ePIC requirements, including timing and spatial resolution, irradiation tolerance, and reasonably large size for module assembly
- Prototypes of interposer for mechanical/electrical connections between strip sensor and ASIC
- ~~Prototypes of light-weight module mechanical structures for forward TOF~~
- Prototypes of frontend ASICs
- Functional and full size low-mass Kapton PCB
- Low-cost interconnect for sensor-ASIC hybridization
- Service hybrid prototype

- **eRD112 ($286k)**
- Sensor R&D ($261k)
  - BNL/HPK/FBK productions
  - TCAD, lab/beam/irradiation tests
- Sensor/ASIC integration ($15k)
  - Interposer
- ~~Mechanical structure ($53k)~~
  - ~~Light-weight structure w/ cooling~~

- **eRD109 ($390k)**
- Frontend ASICs
  - EICROC ($85k)
  - FCFD ($40k)
  - 3rd Party ASICs ($45k)
- Frontend electronics
  - Low-mass Kapton PCB ($30k)
  - Low-cost hybridization ($15k)
  - Service hybrid ($220k)

- **ePIC simulation**
  - Geometry model, digitization and reconstruction
  - Requirements on spatial, timing resolutions, and material budget

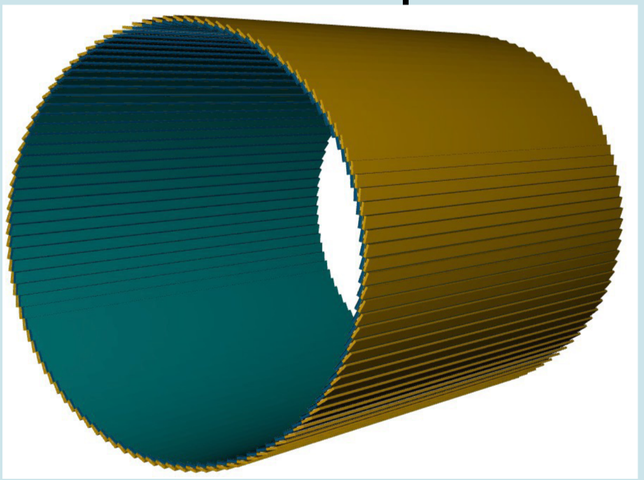
- **Project Engineering Design**
  - Engineering design for pre-TDR
  - Integration & services

Sensor **Electronics** **Sensor-ASIC integration** **Mechanics**

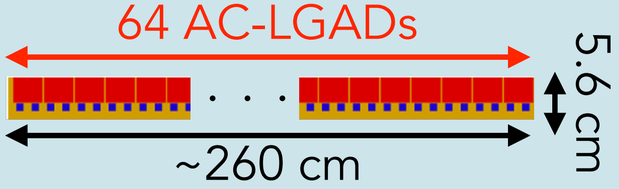
Detector Layout of BTOF

- BTOF is composed of 144 modules to make a cylindric
- 64 AC-LGAD strip sensors are attached to one module
  - ASIC place is under discussion (depending on the ASIC pixel geometry)
- Radius is 60 - 63 cm from the beam pipe covering $-1.42<\eta<1.77$
- Total material budget in acceptance is ~0.01 X/X_0

BTOF shape



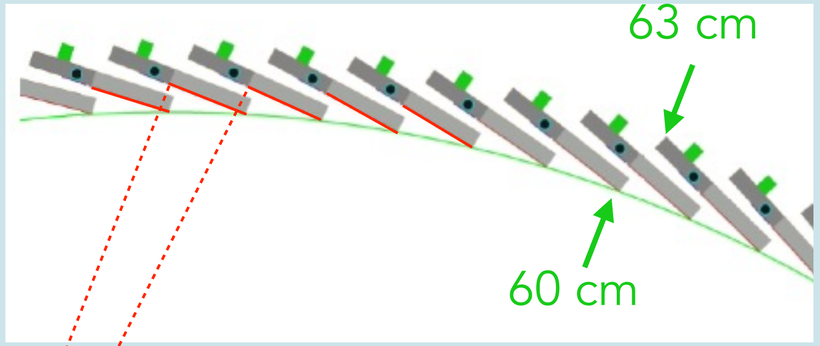
Module top view



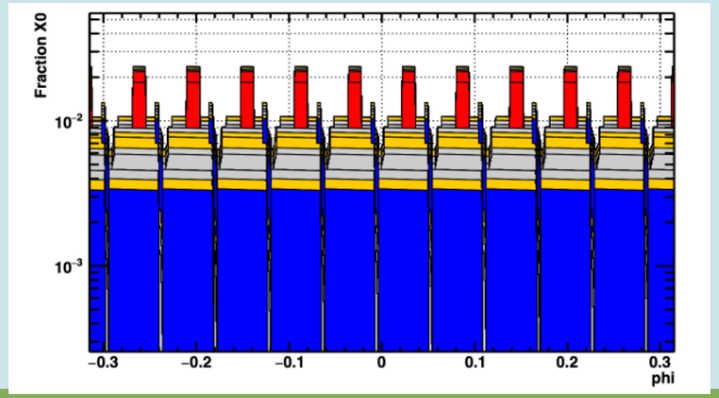
Module cross section

Cylindrical structure by modules

3 mm overlap in Φ



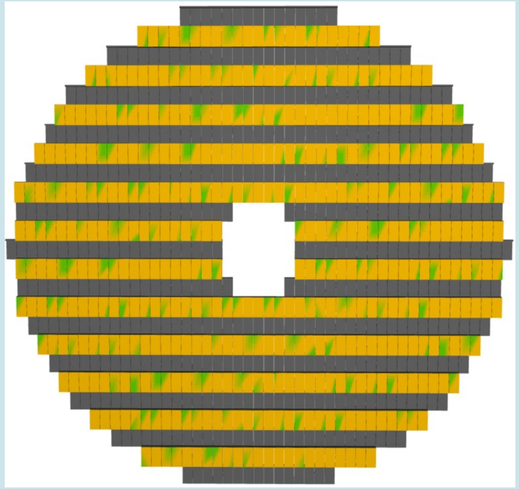
Material budget



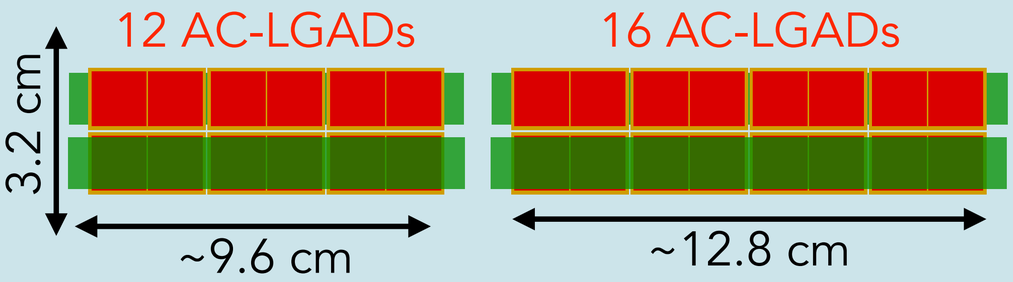
Detector Layout of FTOF

- FTOF is composed of 1816 modules to make a disk
- 12 or 16 AC-LGAD pixel sensors are attached to one module
- Radius is 8 - 60 cm from the beam pipe covering $1.86<\eta<3.85$
- Service hybrid, readout board + power board, is placed in front of sensors
- Total material budget in acceptance is ~0.025 X/X_0
- Service hybrid and cooling system design is important for FTOF

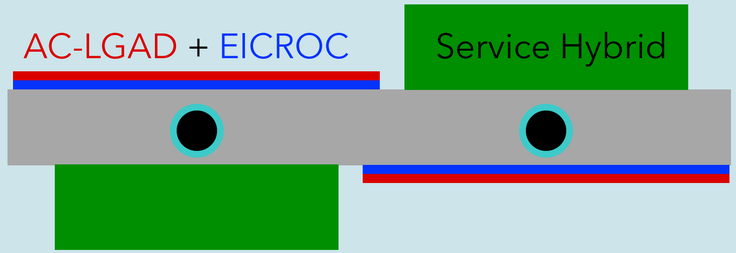
BTOF shape

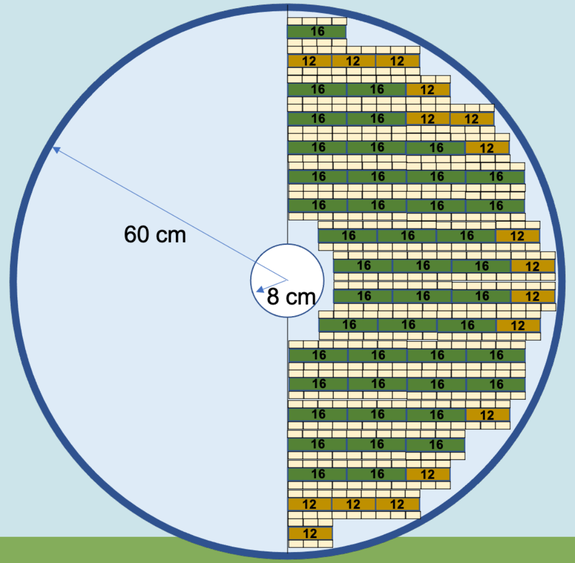


Module top view



Module cross section



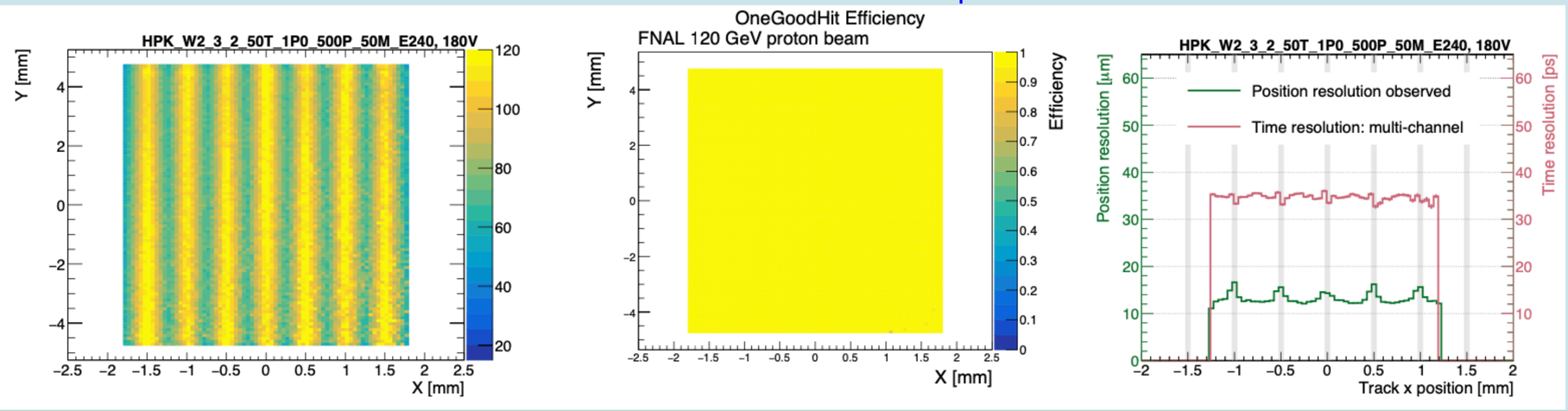


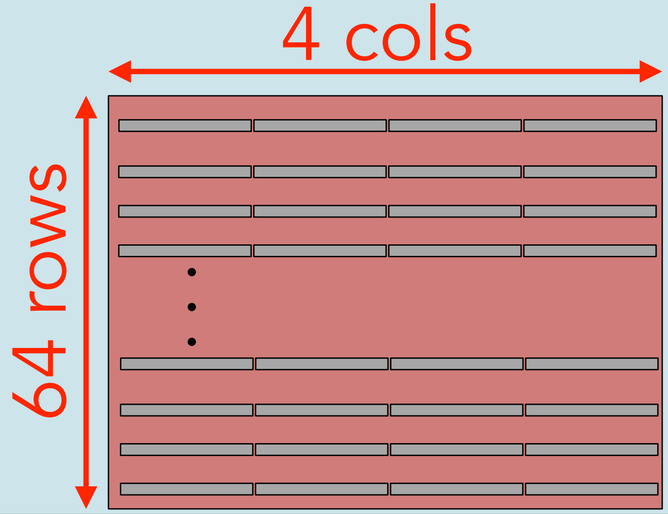
BTOF AC-LGAD sensor

- AC-LGAD technology meets the strict spatial and time resolution requirements
- Strip-type sensor, 3.2 x 4 cm^2 sensor size with 0.05 x 1 cm^2 metals, is used in BTOF
  - The readout metal geometry in a sensor is 64 x 4 and 256 channels each
- 2 ASICs are attached for each with wire bonding

- Total information
  - **9216 sensors**
  - **10 m^2**
  - **2.4 M readout channels**

[eRD112 FY24 Proposal]



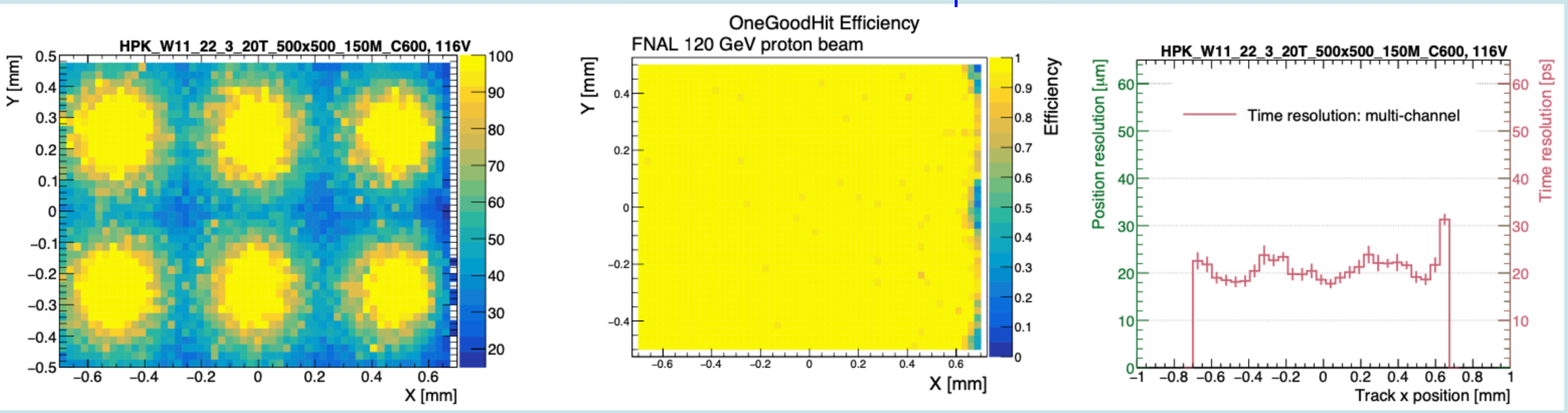


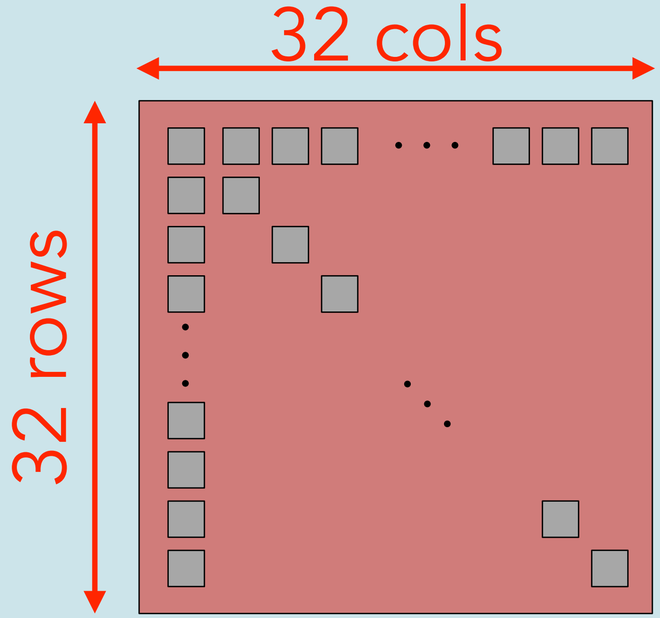
FTOF AC-LGAD sensor

- Pixel-type AC-LGAD sensor, 1.6 x 1.6 cm^2 sensor size with 500 x 500 μm^2 pitch, is used in FTOF
  - The readout metal geometry in a sensor is 32 x 32 and 1024 channels each
- One ASIC (2D 32x32) is attached to the one sensor
- Bump bonding is planned for soldering to ASIC

- Total information
  - **3632 sensors**
  - **1.4 m^2**
  - **3.6 M readout channels**

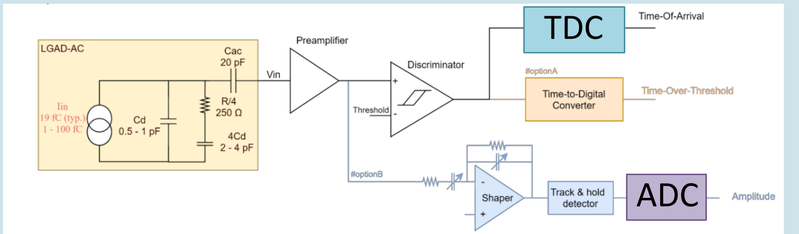
[eRD112 FY24 Proposal]





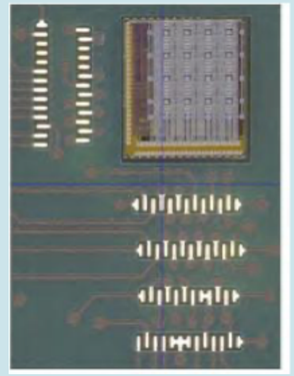
TOF ASIC

- Not only high-time resolution TDC (TOA) but also ADC must be measured
- Due to the large capacitance and readout geometry characteristics caused by the strip type, care must be taken when selecting an ASIC

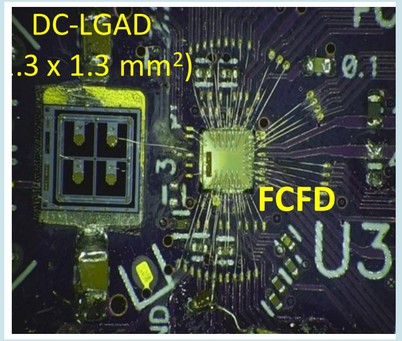


- EICROC (32x32) is one of the common ASICs used in ePIC
  - Design focuses on pixel AC-LGAD readout (tuned for low capacitance)
  - 10-bit TDC and 8-bit ADC is now available (EICROC0)
  - Modification is necessary to read higher capacitance sensor (strip AC-LGAD)

EICROC0



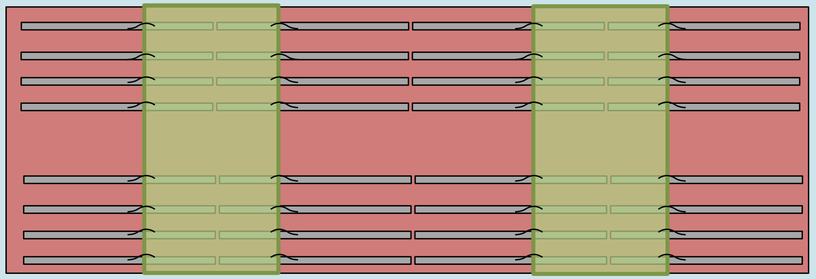
FCFDv0



- FCFD is a new ASIC to use strip AC-LGAD readout
  - FCFD can read higher capacitance AC-LGAD sensor
  - Multiple-channel analog is available for FCFDv1

- The possibility of HGCROC has begun to be discussed
  - It can measure ADC, TOA, and TOT
  - We have to investigate the possibility of the chip as soon as possible and make collaboration with the experts

ASIC



Power budget of TOF

- BTOF power consumption is larger than the FTOF due to the size difference
- Sensors+ASICs and SH of FTOF are placed on the same board, so the cooling power is designed for the sum of the consumption
- SH of BTOF is located in a different place than sensors + ASICs

BTOF

	Power
Sensors	4kW
FCFD	9.4kW
DC-DC	3.3kW
FPGA	1kW
Total	17.7kW

SH = 4.3kW

FTOF

	Power
Sensors	0.3kW
EICROC	3.6kW
DC-DC	2.5kW
FPGA	1kW
Total	7.4kW

Institutes in TOF tasks (official)

- Brookhaven National Laboratory (USA)
- Fermi National Accelerator Laboratory (USA)
- Rice University (USA)
- Oak Ridge National Laboratory (USA)
- Ohio State University (USA)
- Purdue University (USA)
- University of California Santa Cruz (USA)
- University of Illinois at Chicago (USA)
- Hiroshima University (JP)
- RIKEN (JP)
- Shinshu University (JP)
- Nara Woman University (JP)
- National Chen-Kung University (TW)
- National Taiwan University (TW)
- IJCLab, OMEGA, CEA-Saclay (FR)

Tasks in BTOF

- **AC-LGAD sensor**
  - BNL
  - ORNL
  - Univ. of California, Santa Cruz
  - Univ. of Illinois, Chicago
  - Hiroshima University
  - Shinshu University
- **Frontend ASIC**
  - Fermilab
  - Rice University
  - ORNL
  - Hiroshima University
  - National Taiwan University
  - IJCLab/OMEGA/CEA-Saclay
- **Sensor-ASIC integration**
  - BNL
  - ORNL
  - Univ. of California, Santa Cruz
  - Univ. of Illinois, Chicago
  - National Taiwan University
- **Module structure**
  - Purdue University
  - National Cheng-Kung University
- **Module assembly**
  - BNL
  - ORNL
  - Ohio State University
  - Univ. of California, Santa Cruz
  - Hiroshima University
  - RIKEN
  - Nara Woman University
  - National Taiwan University
- **Flex PCB**
  - ORNL
- **Service Hybrid**
  - Rice University
- **Backend electronics**
  - BNL