News – 2/13/2024

- **Incremental Design and Safety Review on ePIC PID detectors conducted on July 5-6:**
  - Presentations; Review report**; answers in preparation (p3/4)**
  - PDR2: Particle Identification Detectors – Summer 2024?
- **EIC Project Detector R&D**
  - FY24 proposals; Decision (p5); **contracts in progress, mid-year report due Feb 29**
  - **Detector R&D Day:** March (?) 2024; **Detector R&D annual review** – August 2024 with deadline for submission July 1, 2024
- **ePIC TOF Project Engineering Design**
  - **Mechanical engineering :** support structure and cooling submitted on **June 27**: Mechanical PED
  - **BTOF (and FTOF?) module prototyping in preparation**
- **ePIC TOF DSC**
  - Working with CAMs on schedule and cost, identify institutional responsibilities and L5/L6 contacts (p6-7):

  BTOF: Mathew Gignac/Satoshi Yano/Zhenyu Ye, FTOF: Mathieu Benoit/Wei Li, Common System: Andreas Jung/Zhangbu Xu
  - **Forming new TOF DSC leadership team in preparation for TDR and CD2/3 reviews (discussion at next week's TOF meeting)**
- **ePIC TOF Simulation**
  - Updated geometry database on 9/29 – Zhenyu**: updated in DD4HEP #564 (p11)**
  - TOF in tracking – Nicolas et al.: Re-check FTOF material budget impact
  - TOF PID reconstruction – Oskar et al.: TOF PID LUT, reconstruction, validation plots
  - TOF digitization – Souvik/Adam: charge sharing and detector noise
  - TOF service in simulation – TBD: implement the missing material for mechanical support structure, cooling and cabling

FY24 Plan

- Simulation
- R&D:
  - Sensor: new BNL+HPK production and Characterization, simulation, irradiation
  - Sensor-ASIC integration: interposer for BTOF, hybridization for FTOF pixel sensor-ASIC
  - ASIC: EICROC0/EICROC1, FCFDv1/v2
  - Module PCB: Low-mass flexible Kapton for BTOF
  - Module structure: Low-mass CF structure for BTOF module
  - Service Hybrid: RDO + Power board
- PED:
  - BTOF and FTOF (5%X_0) support structure
  - BTOF (and FTOF?) module in preparation
- TDR

News

- **Incremental Design and Safety Review on ePIC PID detectors conducted on July 5-6:** Review presentations; Final review report

Detector

- (AC-LGAD) 35ps Barrel/ 25ps FW timing resolution seems to be almost the best performance without safety margin. Under these circumstances, a bias voltage scheme should be more flexible than only one pair of cables for each board, because the temperature gradient and the position-dependent radiation fluence require different operation voltages.
- (AC-LGAD) The type of interconnection to the sensors (like wire bonding or bump bonding) must be clearly specified. If a detector uses a bump bonding connection, we would advise to start testing the flip-chipping process since it takes longer to develop a stable procedure.

✓ Fluence: Wei/Xiao
- Power for Service Hybrid: Tonko/Wei
- Thermal: Yi/Andy

- eRD109: ORNL
- eRD112: UCSC/UIC

Electronics

- The initial requirements for the EICROC were specified mostly for the Roman Pot detector and not for all detectors which use EICROC. We advise summarizing the requirements for all detectors and making a single EICROC specification before submitting further prototype chips.
- A specification on the tolerable clock drift and the robustness to phase irregularities should be defined and will help to ensure that these parameters are measured and controlled in the architecture from the beginning of the design phase. The DAQ design should include a backup solution for a directly distributed clock to the RDO boards to provide the clock precision required by each subsystem.

- BTOF: Draft
- FTOF: ?

✓ Tonko: 5ps jitter

News

- **Incremental Design and Safety Review on ePIC PID detectors conducted on July 5-6:** Review presentations; Final review report

Tracking

- Recent progress has been made in ePIC's cross-cutting PID WG to understand tracking requirements for PID detectors. Requirements documents should capture the bi-directional interface between tracking and PID detectors: e.g., translation between extrapolated track impact point and angle resolution requirements for PID detectors. It could be evaluated where the PID subdetectors can contribute to improving the tracking performance and how in the reconstruction algorithms this could be integrated.
  - ZY: (recommendation)
- Encouraging track momentum resolution improvement was achieved by including the AC-LGAD in reconstruction. The reviewers suggest extending this study to understand the impact on the extrapolated track impact point and angle at the radius of the DIRC.
  - Nicholas (NCU?)

Recommendations

1. Capture the bi-directional interface between tracking and PID detectors: e.g., translation between position and angular resolution requirements for PID detectors.
   - ZY: draft

AC-LGAD FY24 R&D Proposal

- Optimized sensor design and final prototypes that meet ePIC requirements, including timing and spatial resolution, irradiation tolerance, and reasonably large size for module assembly
- Prototypes of interposer for mechanical/electrical connections between strip sensor and ASIC
- ~~Prototypes of light-weight module mechanical structures for forward TOF~~
- Prototypes of frontend ASICs
- Functional and full size low-mass Kapton PCB
- Low-cost interconnect for sensor-ASIC hybridization
- Service hybrid prototype

eRD112 (414k->286k$)

- Sensor R&D (346k->261k$)
  - BNL, HPK~~/FBK~~ productions
  - TCAD, lab/beam/irradiation tests
- Sensor/ASIC integration (15k$)
  - Interposer
- ~~Mechanical structure ($53k)~~
  - ~~Light-weight structure w. cooling~~

eRD109 (435k->390k$)

- Frontend ASICs
  - EICROC (85k$)
  - FCFD (40k$)
  - ~~3rd Party ASICs (45k$)~~
- Frontend electronics
  - Low-mass Kapton PCB (30k$)
  - Low-cost hybridization (15k)
  - Service hybrid (220k)

EPIC Simulation

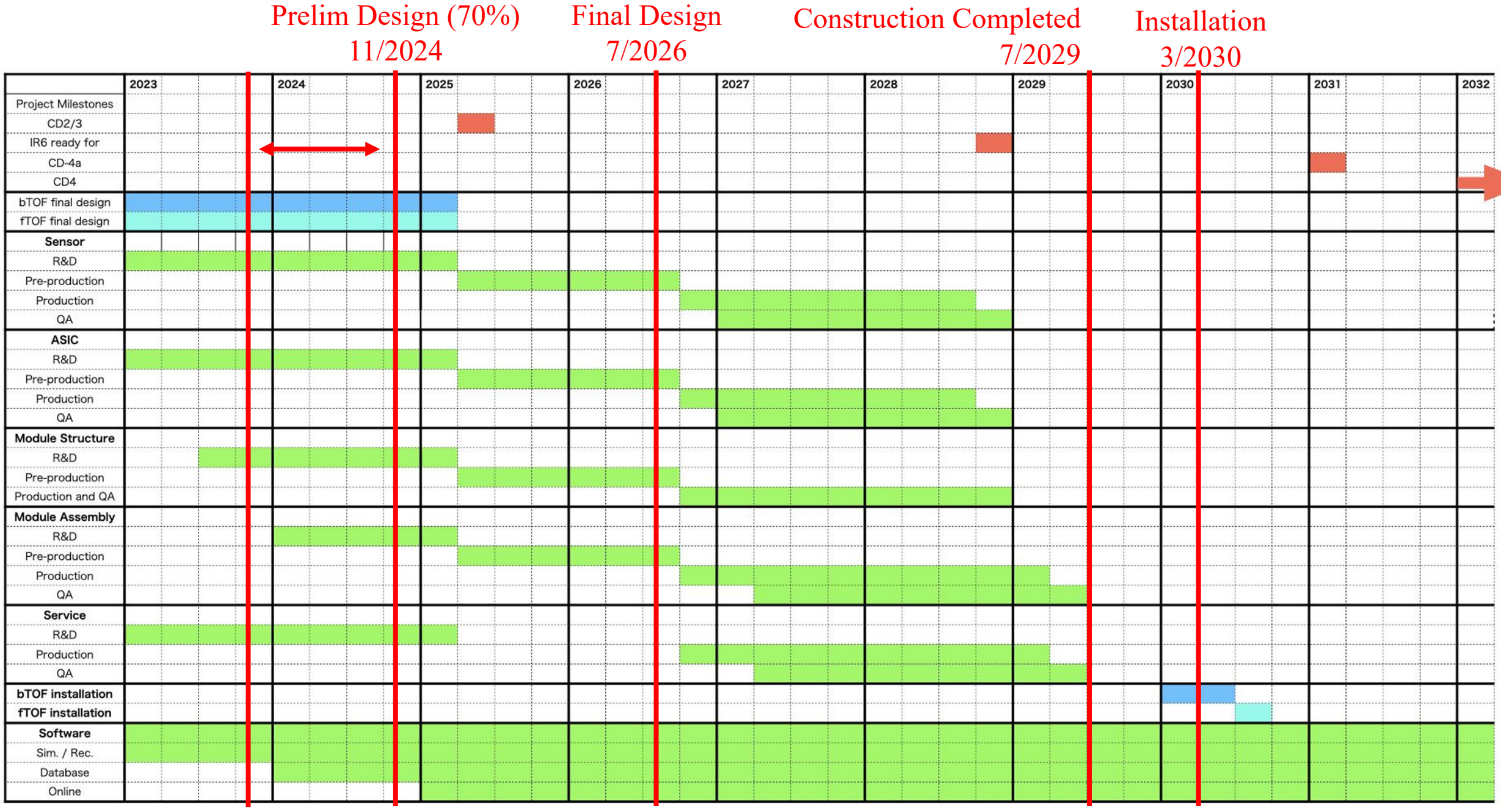
- Geometry model, digitization and reconstruction
- Requirements on spatial, timing resolutions, and material budget

Project Engineering Design

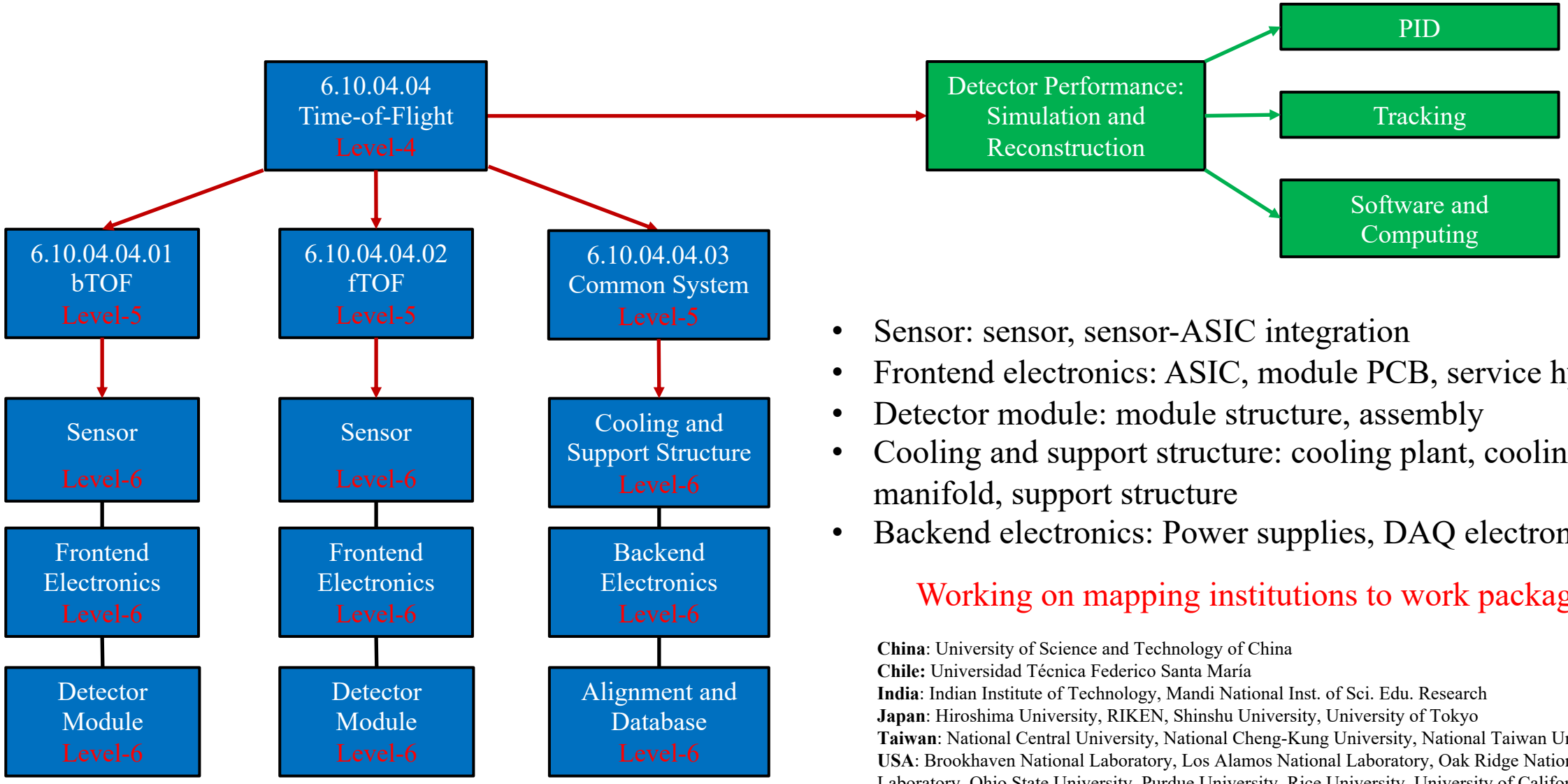
- Engineering design for pre-TDR
- Integration & services

Sensor **Electronics** **Sensor-ASIC integration** **Mechanics**

Schedule and Timeline



Proposed Working Package Structure



- Sensor: sensor, sensor-ASIC integration
- Frontend electronics: ASIC, module PCB, service hybrid
- Detector module: module structure, assembly
- Cooling and support structure: cooling plant, cooling manifold, support structure
- Backend electronics: Power supplies, DAQ electronics

Working on mapping institutions to work packages

China: University of Science and Technology of China
Chile: Universidad Técnica Federico Santa María
India: Indian Institute of Technology, Mandi National Inst. of Sci. Edu. Research
Japan: Hiroshima University, RIKEN, Shinshu University, University of Tokyo
Taiwan: National Central University, National Cheng-Kung University, National Taiwan University
USA: Brookhaven National Laboratory, Los Alamos National Laboratory, Oak Ridge National Laboratory, Ohio State University, Purdue University, Rice University, University of California - Santa Cruz, University of Illinois at Chicago