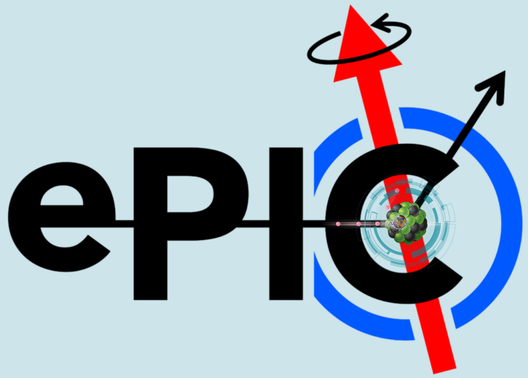


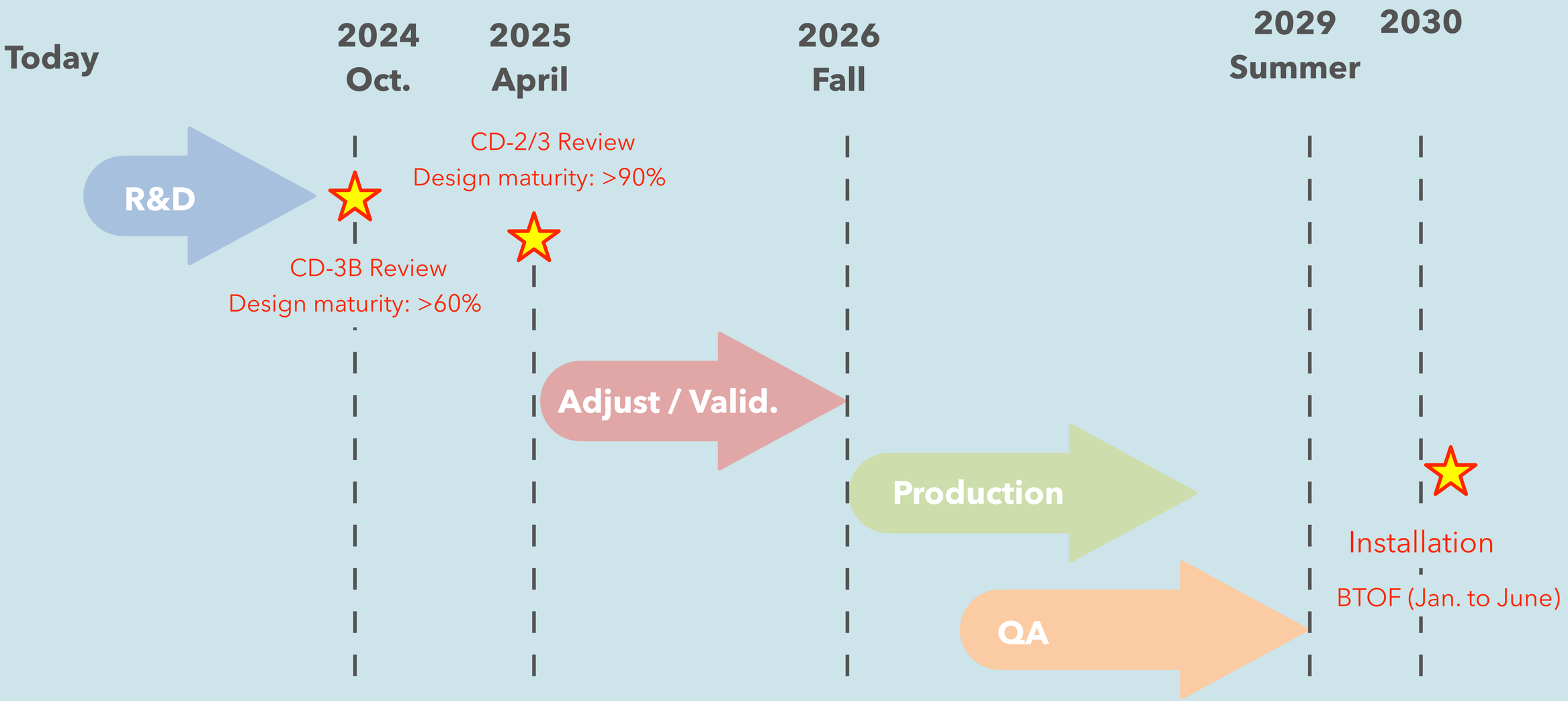
TOF

Strategy toward CD-3B review (v0)

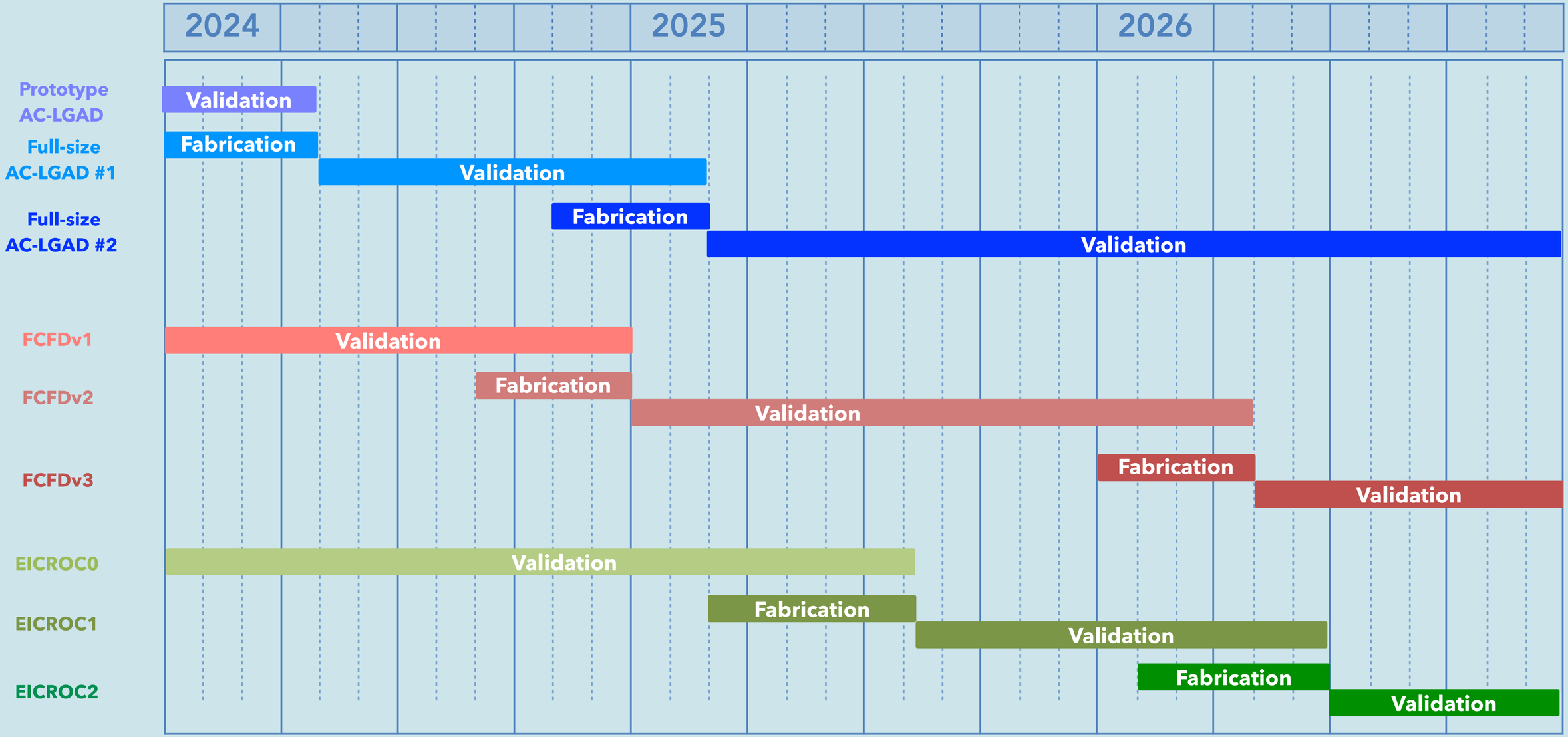
Satoshi Yano

Hiroshima University SKCM²

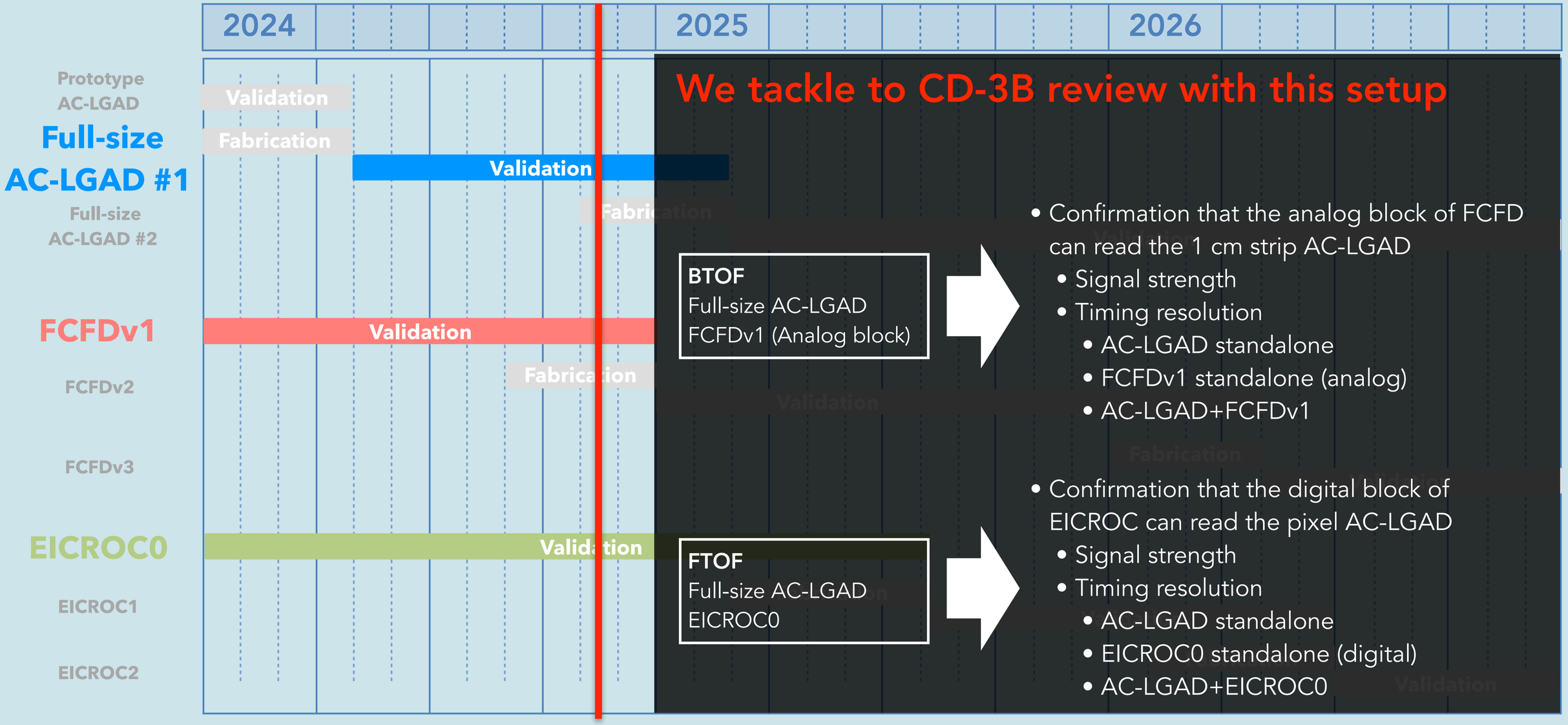
ePIC schedule



Schedule of sensor and ASIC



Schedule of sensor and ASIC



Idea of strategy for the CD-3B review (1)

- Absence of the BTOF digital block demonstration is a concern
  - It is important to show that "we can't show it now, but we will definitely be able to do it shortly”
  - It is necessary to fully understand and demonstrate the individual characteristics of the sensor, the characteristics of the FCFD's analog block, and the combined performance
  - In addition to sensor and FCFD performance, the EICROC study will help to corroborate the story
    - Successful signal readout by EICROC means "complete understanding of the AC-LAGD → analog → digital signal chain"
    - This knowledge shows that we have the technology to extend analog blocks to digital blocks while keeping a good timing resolution
  - Perhaps showing that EICROC does not read out the strip AC-LGAD "as expected" may help to show that this situation is under control
  - Investigating the availability of other ASICs is also important

- The beam test at DESY is scheduled for June
  - It is a good opportunity to fully understand the sensors and ASICs, except for the digital part of the FCFD
  - Real MIP beam is mandatory to understand each performance
  - Before the test, items that are not yet fully understood need to be identified in the lab tests, e.g. radiation source and IR laser
    - Gain uniformity, temperature dependence of gain, timing resolution, spatial resolution, and power consumption
  - Development of a board capable of putting a full-size sensor is essential

Idea of strategy for the CD-3B review (2)

- Manufacturing a long (~1.3m) FPC for the BTOF stave is a concern
  - This is probably the most problematic R&D element except the ASIC because there are not many examples of such a long FPC being utilized in HEP
  - Nara Women's University and RIKEN, which have experience in developing approximately 1.3m FPC with a low material budget (O(1%) X/X0) for sPHENIX silicon strip sensor detectors, have agreed to support the development
  - It is necessary to specify the required performance and demonstrate that we have the experience/technology to make it
  - However, it is not clear if it can be used in this case, so this is an urgent item to be clarified

- Sensor-ASIC integration
  - Several bonding strategies are planned, e.g. bump bonding, wire bonding, and using interposer
  - Adjustments are needed, but these are established techniques
  - It is important to show that these methods can be applied geometrically to sensors and ASICs bonding
  - Need to understand the application limits of each method (feedback to the ASIC R&D)
  - At least the first design of the interposer is required

- Modules
  - It is necessary to show how each component is attached and the total amount of material budget is acceptable

Idea of strategy for the CD-3B review (3)

- Cooling system
  - It is necessary to finalize the evaluation of power consumption and the tolerable temperature range of each component
  - In the case of FTOF, the service hybrid (SH) is cooled at the same time as the sensor + ASIC, but in the case of BTOF, the SH is installed in a separate location from the sensor + ASIC.
  - It is necessary to determine the cooling method of BTOF SH (water cooling is used for Sensor + ASIC)
  - A long and a long-winding cooling pipe are used for BTOF and FTOF, respectively, so it is needed to check the difference in cooling capacity between the inlet and outlet

- SH design
  - Data rate and power distribution scheme should be designed
  - BTOF SH position and cooling method are not finalized yet
  - It is necessary to show the data rate and the processing power
  - If possible data stream of AC-LGAD→EICROC→FPC→FPGA is tested

Summary

- I started thinking about what to show at the CD-3B review
- Today’s presentation is the v0, so it matures gradually

Backup

Summary of the confirmation items (v0)

- Sensor + ASIC
  - BTOF: Fully understand the behavior of the sensor and FCFDv1 and the analog block to which they are attached
  - FTOF: Fully understand the behavior of the sensor and EICROC0 and the digital block to which they are attached

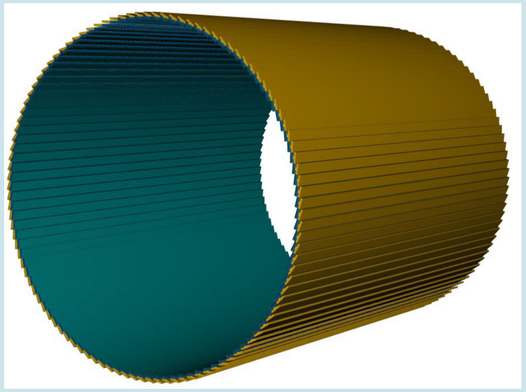
- FPC of BTOF
  - Identifying the required performance
  - Clarifying whether the technology developed in sPHENIX can be used

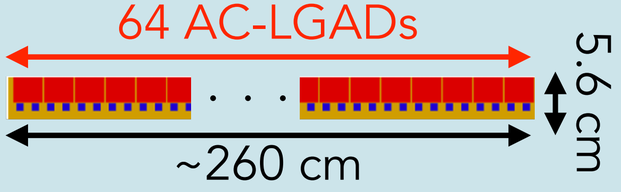
- Sensor-ASIC integration
  - Understanding the application limits of each method
  - Starting the design of the interposer

- Cooling
  - Finalizing evaluation of the power consumption and tolerable temperature range
  - Determining of the method for BTOF SH cooling
  - Understanding the position dependence of water temperature and demonstrating the ability to operate at tolerable temperatures

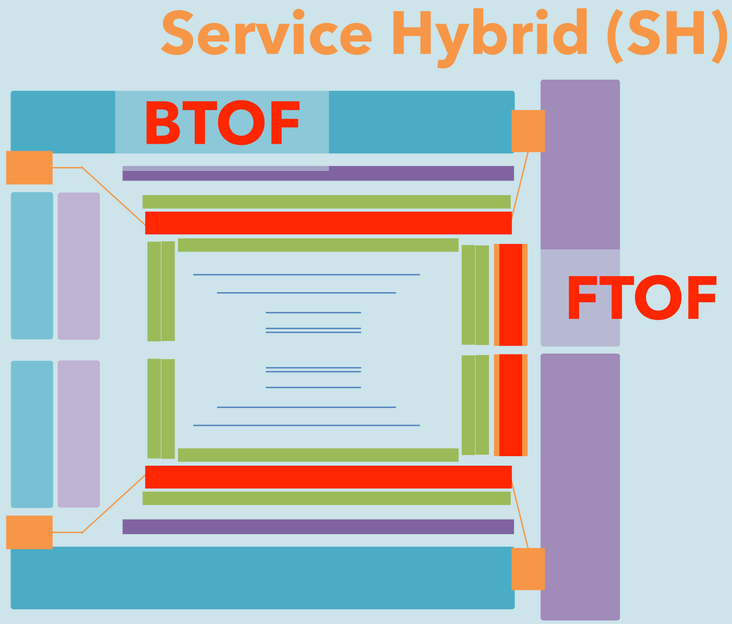
- Service Hybrid
  - Identifying the required performance (power consumption and data processing)

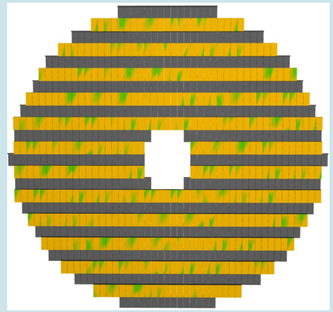
Structure of BTOF and FTOF

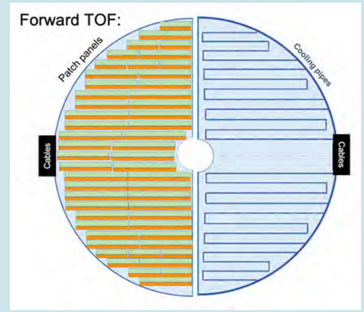


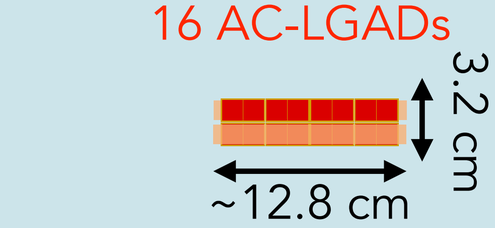


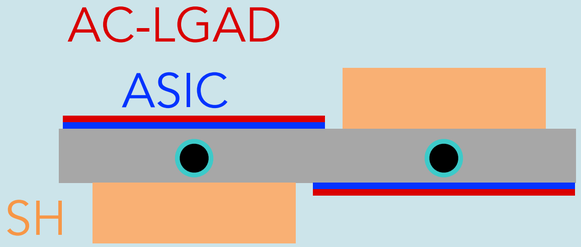
One cooling pipe is shared by 128 ASICs









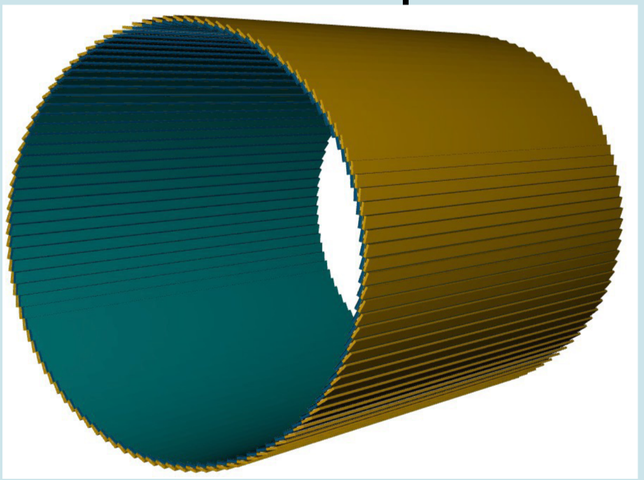


The winding cooling pipe is shared by ASIC and Service Hybrid

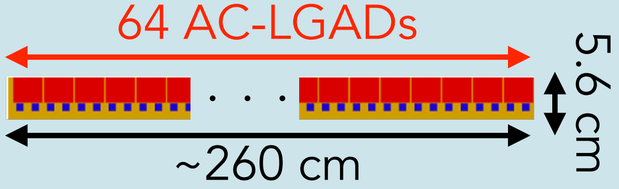
Detector Layout of BTOF

- BTOF is composed of 144 modules to make a cylindric
- 64 AC-LGAD strip sensors are attached to one module
  - ASIC place is under discussion (depending on the ASIC pixel geometry)
- Radius is 60 - 63 cm from the beam pipe covering $-1.42<\eta<1.77$
- Total material budget in acceptance is ~0.01 X/X_0

BTOF shape



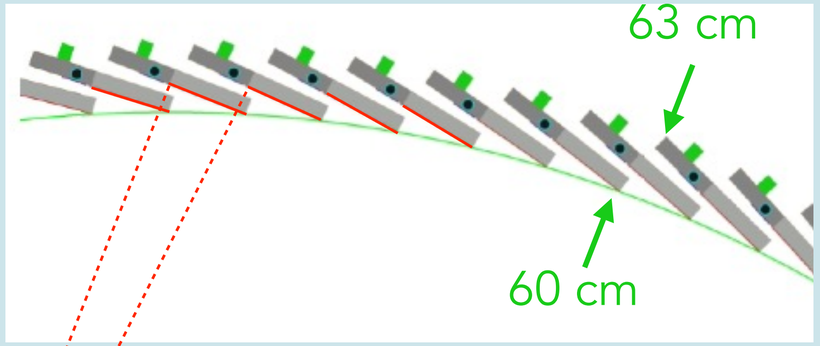
Module top view



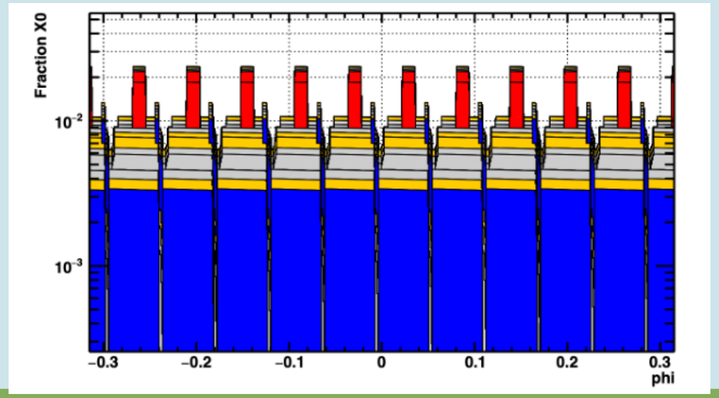
Module cross section

Cylindrical structure by modules

3 mm overlap in Φ



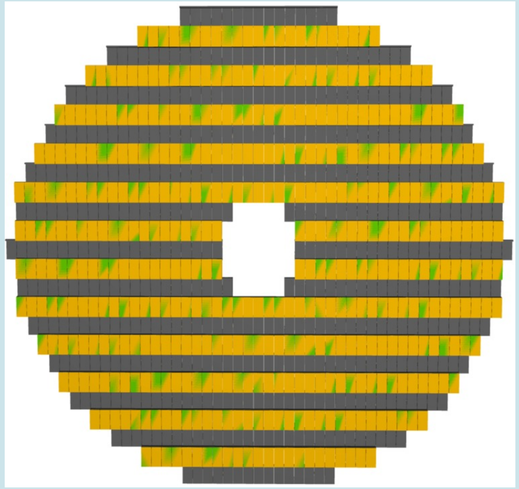
Material budget



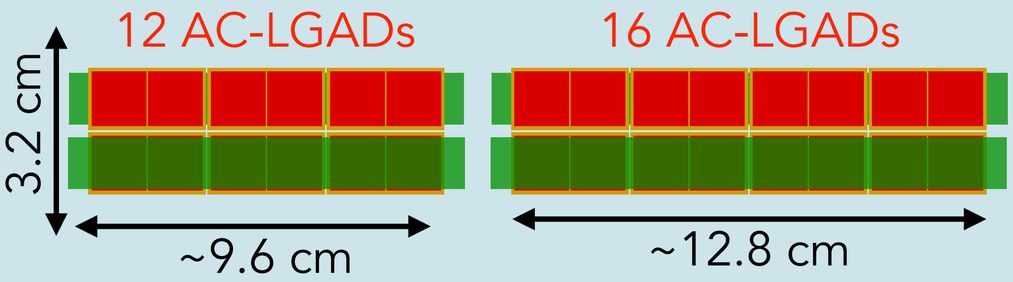
Detector Layout of FTOF

- FTOF is composed of 1816 modules to make a disk
- 12 or 16 AC-LGAD pixel sensors are attached to one module
- Radius is 8 - 60 cm from the beam pipe covering $1.86<\eta<3.85$
- Service hybrid, readout board + power board, is placed in front of sensors
- Total material budget in acceptance is ~0.025 X/X_0
- Service hybrid and cooling system design is important for FTOF

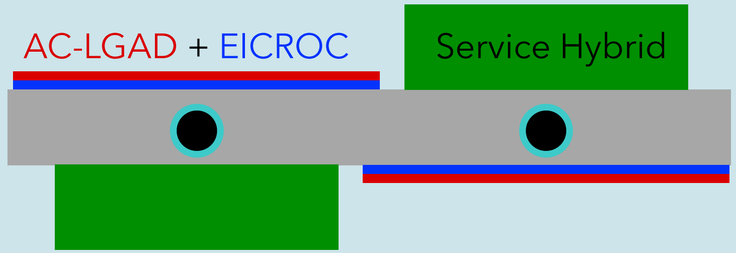
BTOF shape

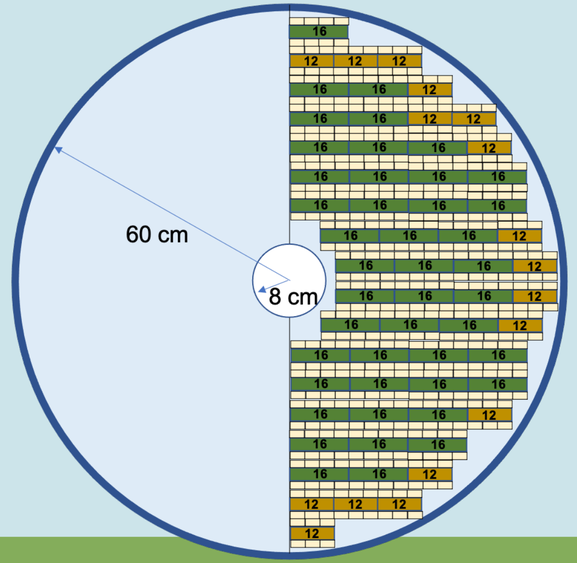


Module top view



Module cross section



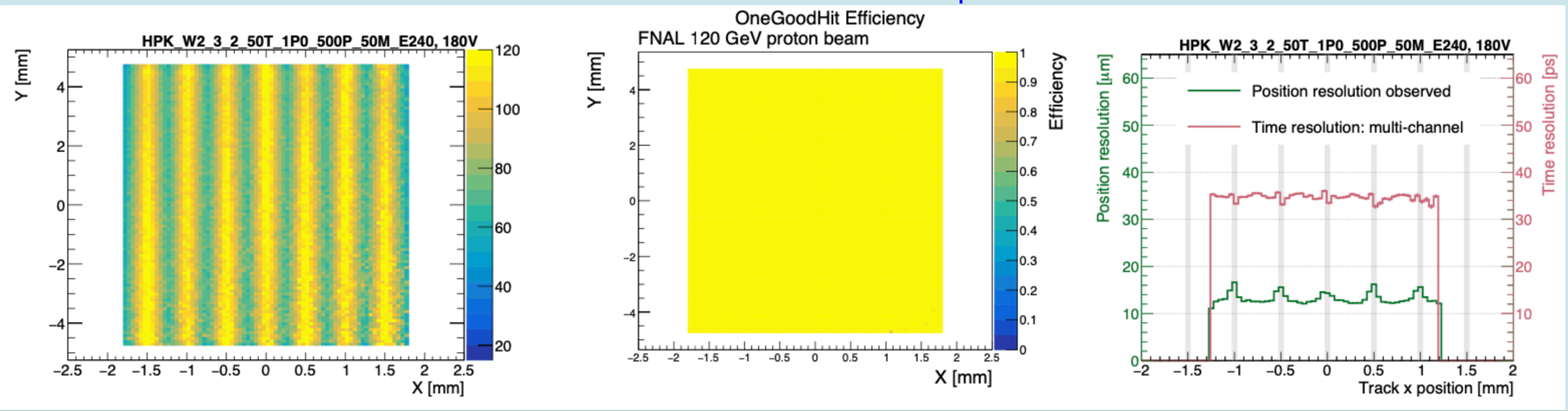


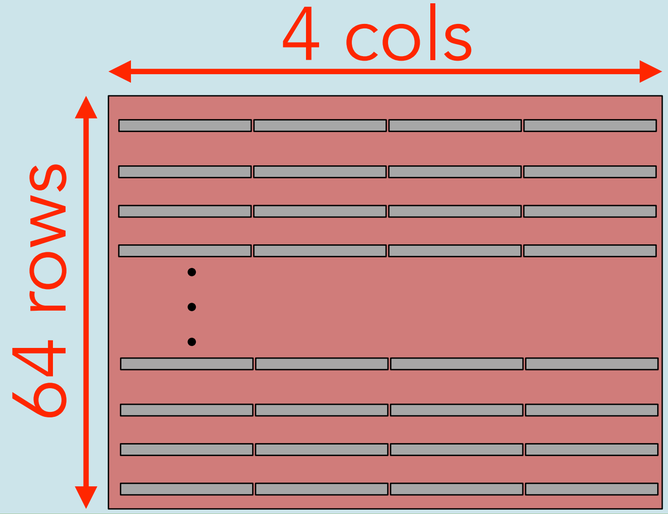
BTOF AC-LGAD sensor

- AC-LGAD technology meets the strict spatial and time resolution requirements
- Strip-type sensor, 3.2 x 4 cm^2 sensor size with 0.05 x 1 cm^2 metals, is used in BTOF
  - The readout metal geometry in a sensor is 64 x 4 and 256 channels each
- 2 ASICs are attached for each with wire bonding

- Total information
  - **9216 sensors**
  - **10 m^2**
  - **2.4 M readout channels**

[eRD112 FY24 Proposal]



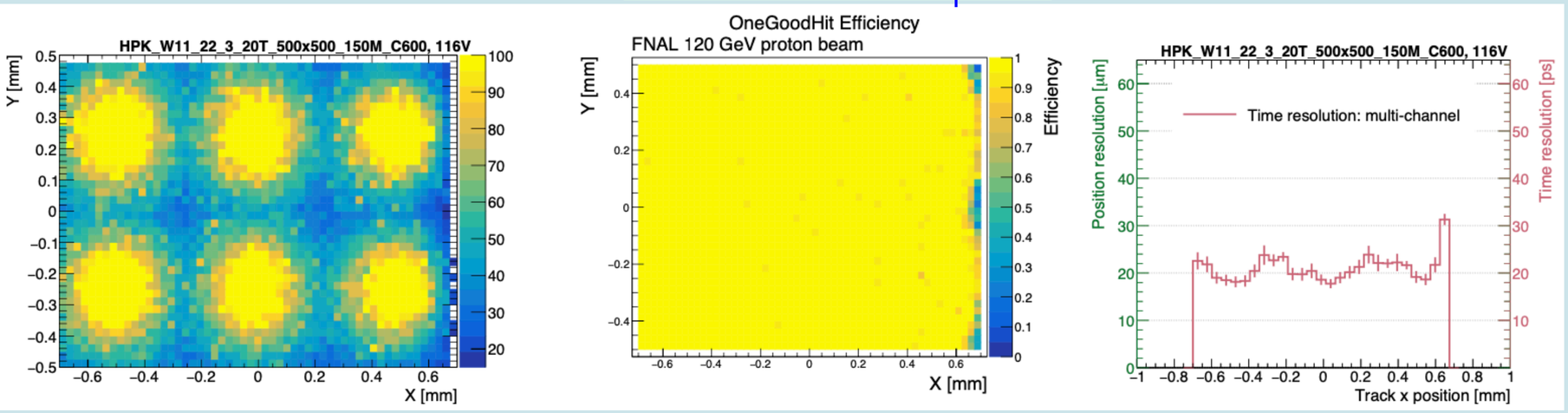


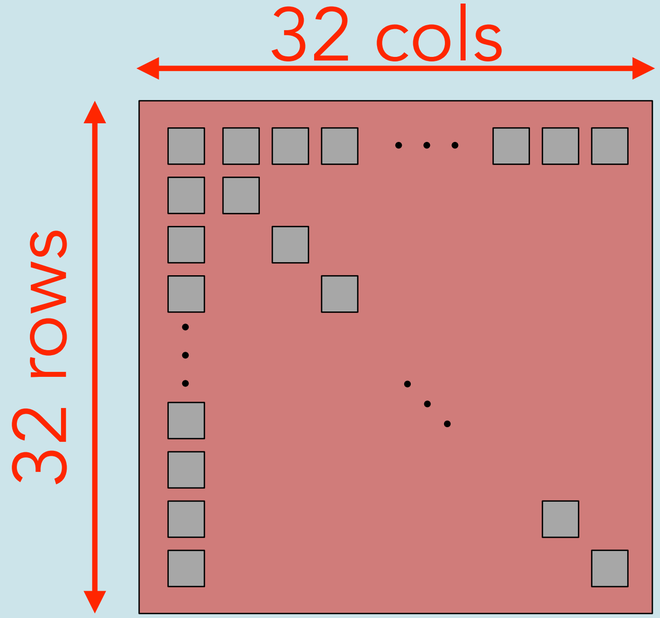
FTOF AC-LGAD sensor

- Pixel-type AC-LGAD sensor, 1.6 x 1.6 cm^2 sensor size with 500 x 500 μm^2 pitch, is used in FTOF
  - The readout metal geometry in a sensor is 32 x 32 and 1024 channels each
- One ASIC (2D 32x32) is attached to the one sensor
- Bump bonding is planned for soldering to ASIC

- Total information
  - **3632 sensors**
  - **1.4 m^2**
  - **3.6 M readout channels**

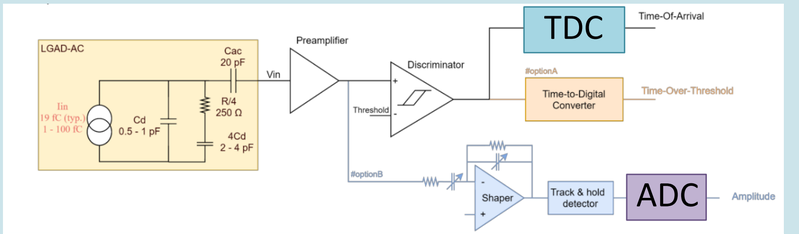
[eRD112 FY24 Proposal]





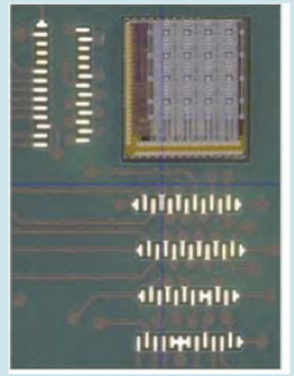
TOF ASIC

- Not only high-time resolution TDC (TOA) but also ADC must be measured
- Due to the large capacitance and readout geometry characteristics caused by the strip type, care must be taken when selecting an ASIC

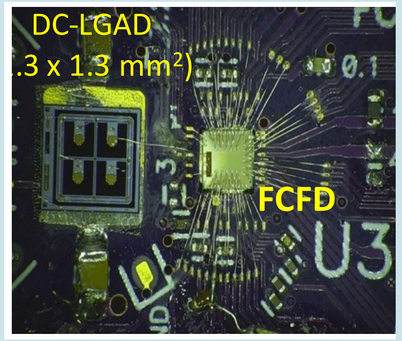


- EICROC (32x32) is one of the common ASICs used in ePIC
  - Design focuses on pixel AC-LGAD readout (tuned for low capacitance)
  - 10-bit TDC and 8-bit ADC is now available (EICROC0)
  - Modification is necessary to read higher capacitance sensor (strip AC-LGAD)

EICROC0



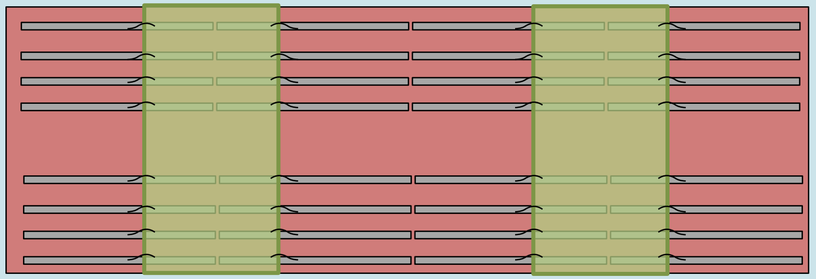
FCFDv0



- FCFD is a new ASIC to use strip AC-LGAD readout
  - FCFD can read higher capacitance AC-LGAD sensor
  - Multiple-channel analog is available for FCFDv1

- The possibility of HGCROC has begun to be discussed
  - It can measure ADC, TOA, and TOT
  - We have to investigate the possibility of the chip as soon as possible and make collaboration with the experts

ASIC



Institutes in TOF tasks (official)

- Brookhaven National Laboratory (USA)
- Fermi National Accelerator Laboratory (USA)
- Rice University (USA)
- Oak Ridge National Laboratory (USA)
- Ohio State University (USA)
- Purdue University (USA)
- University of California Santa Cruz (USA)
- University of Illinois at Chicago (USA)
- Hiroshima University (JP)
- RIKEN (JP)
- Shinshu University (JP)
- Nara Woman University (JP)
- National Chen-Kung University (TW)
- National Taiwan University (TW)
- IJCLab, OMEGA, CEA-Saclay (FR)

Tasks in BTOF

- **AC-LGAD sensor**
  - BNL
  - ORNL
  - Univ. of California, Santa Cruz
  - Univ. of Illinois, Chicago
  - Hiroshima University
  - Shinshu University
- **Frontend ASIC**
  - Fermilab
  - Rice University
  - ORNL
  - Hiroshima University
  - National Taiwan University
  - IJCLab, OMEGA, CEA-Saclay
- **Sensor-ASIC integration**
  - BNL
  - ORNL
  - Univ. of California, Santa Cruz
  - Univ. of Illinois, Chicago
  - National Taiwan University
- **Module structure**
  - Purdue University
  - National Cheng-Kung University
- **Module assembly**
  - BNL
  - ORNL
  - Ohio State University
  - Univ. of California, Santa Cruz
  - Hiroshima University
  - RIKEN
  - Nara Woman University
  - National Taiwan University
- **Flex PCB**
  - ORNL
- **Service Hybrid**
  - Rice University
- **Backend electronics**
  - BNL

Power budget of TOF

- BTOF power consumption is larger than the FTOF due to the size difference
- Sensors+ASICs and SH are placed on the same board, so the cooling power is designed for the sum of the consumption
- SH of BTOF is located in a different place than sensors + ASICs

BTOF

	Power
Sensors	4kW
FCFD	9.4kW
DC-DC	3.3kW
FPGA	1kW
Total	17.7kW

SH = 4.3kW

+

Optical fiber

FTOF

	Power
Sensors	0.3kW
EICROC	3.6kW
DC-DC	2.5kW
FPGA	1kW
Total	7.4kW