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Epic Fpc:
Low Trl Prototype, definition stage.

WP3 Electrical interfaces

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marcello.borri@stfc.ac.uk

Outline

- Introduction;
- Circuit definition;
- Signal ratings;
- Manufacturing technology;
- Layout;
- Material budget;
- Interconnection technology;
- Prototyping;

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Introduction (1/2)

- Last reported at the January 2024 EPIC work-fest.

- WP3 Electrical interfaces is growing:
  - BNL: interest in the simulation of transmission line;
  - LBNL, UK: low level TRL prototyping and multiple supplier evaluation;
    - Oxford University is advertising a summer project to test low-TRL FPC prototypes;

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Introduction (2/2)

- Targeting a low TRL prototype to be included in the TDR:
  - Capture the existing snapshot of the evolving design;
  - Design a low TRL prototype;
  - Validate manufacturing capabilities;
  - Select a potentially suitable interconnection technique;
  - Measure AC signal and DC power integrity;

- Focussing on OB-like FPCs.

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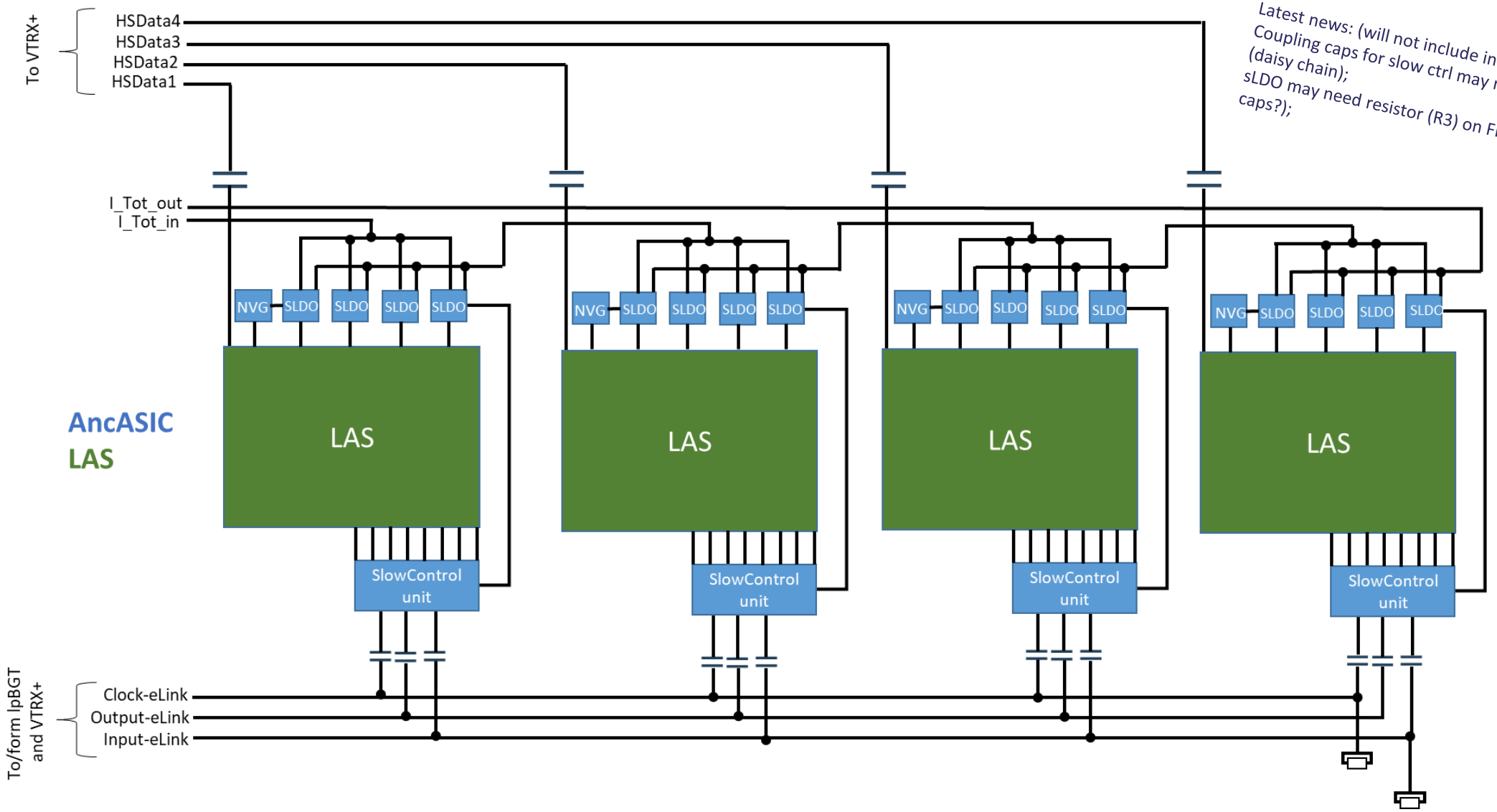
Circuit definition



FPC connects the AncASIC to the DAQ system and pwr supplies.

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Presenting a sequence of 4 sensors.
[longest sequence in Epic Svt]

Signal ratings

Signal name	Type	Comment	Coupling	Standard	lpGBT eLink	Rate
slow ctrl clk (down)	AC	from lpGBT to AncASIC	Capacitive	CERN Low Powering Signal (CLPS)	clock-eLink	80 Mb/s
slow ctrl write (down)	AC	from lpGBT to AncASIC	Capacitive	CERN Low Powering Signal (CLPS)	output-eLink	80 Mb/s
slow ctrl read (up)	AC	from AncAsic to lpGBT	Capacitive	CERN Low Powering Signal (CLPS)	input-eLink	160 Mb/s
data	AC	from AncAsic to VTRX+ (1 diff line/AncASIC)	Capacitive	CERN Low Powering Signal (CLPS)	N/A	5.12 Gb/s (or 10Gb/s)
voltage supply	DC	Max: (2.5V/AncASIC) * (4 AncASIC)	Direct	10% Vdrop for 2.5V/LAS, is it OK?	N/A	N/A
current	DC	2.5 A (total per AnASIC)	Direct		N/A	N/A

To check: Is voltage supply still 2.5V ? (1.8V?)
To check: Is current supply still 2.5A ? (worst case)

Manufacturing technology

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Options – Al FPC suppliers

- Research and Production Enterprise LTU: (under evaluation, UK)
  - https://www.ltu.ua/
- CERN Micro-Pattern Technologies Lab: (currently not considered)
  - https://ep-dep-dt.web.cern.ch/micro-pattern-technologies
- Omni Circuit Boards: (under evaluation, Yuan Mei)
  - https://www.omnicircuitboards.com/
- Q-Flex Inc: (under evaluation, Yuan Mei)
  - https://qflexinc.com/

Comments - Al FPC suppliers

- Risk mitigation of supply chain:
  - To identify at least two different suppliers of Al FPCs;
- Possibly the two (or more) suppliers will use different manufacturing processes:
  - Q: can we get the same design(s) manufactured by both? [standardisation]

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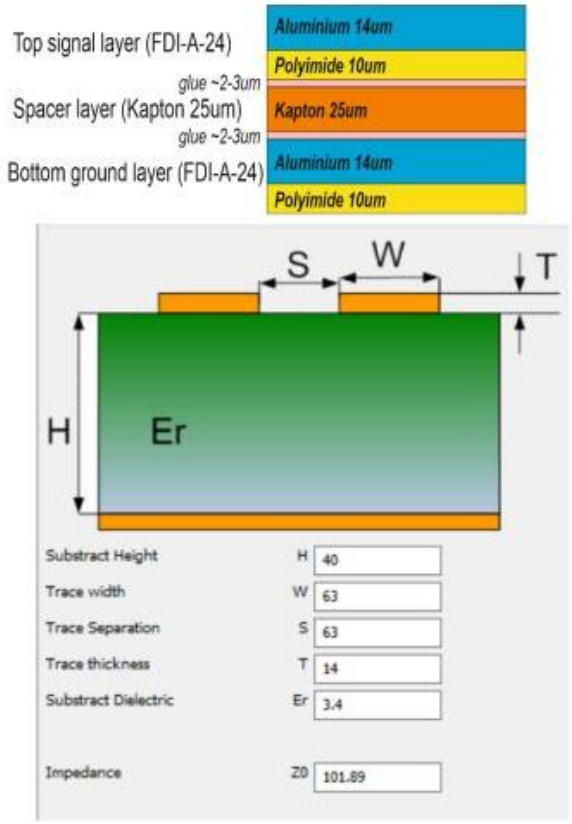
Focus on RPE LTU – UK OB prototype

Cross-section



Proposed FPC stack-up for 100hom impedance tracks

Foot-prints in layout

Signal name	Foot-print	#	Comment
slow ctrl clk (down)	3.15E-04	1.00E+00	FDI-A-24, Diff pair footprint: (63+63+63) = 189um, Space between diff pairs: (63+63) = 126um, totla foot print
slow ctrl write (down)	3.15E-04	1.00E+00	
slow ctrl read (up)	3.15E-04	1.00E+00	
data	3.15E-04	4.00E+00	
voltage supply	3.00E-03	1.00E+00	
Total	5.21E-03		

FDI-A-24, Diff pair footprint:
Differential pair only : (63+63+63) = 189um;
Space between diff pairs: (63+63) = 126um;
Total foot-print: 315um;

Voltage drops for common bus FPC + Bridge FPC										
sLDO	V (target)	V (max)	I (A)	Al resistivity (ohm*m	Al tickness (m	Al length (m)	Width (m)	Al resistance (ohm	Voltage drop (V	% wrt V (target
Opt.1	2.5	TBC	2.5	2.65E-08	1.40E-05	1.50E-01	1.00E-03	2.84E-01	7.10E-01	2.84E+01
Opt.2	2.5	TBC	2.5	2.65E-08	1.40E-05	1.50E-01	2.00E-03	1.42E-01	3.55E-01	1.42E+01
Opt.3	2.5	TBC	2.5	2.65E-08	1.40E-05	1.50E-01	3.00E-03	9.46E-02	2.37E-01	9.46E+00
Opt.4	2.5	TBC	2.5	2.65E-08	1.40E-05	1.50E-01	4.00E-03	7.10E-02	1.77E-01	7.10E+00
Opt.5	2.5	TBC	2.5	2.65E-08	1.40E-05	1.50E-01	5.00E-03	5.68E-02	1.42E-01	5.68E+00

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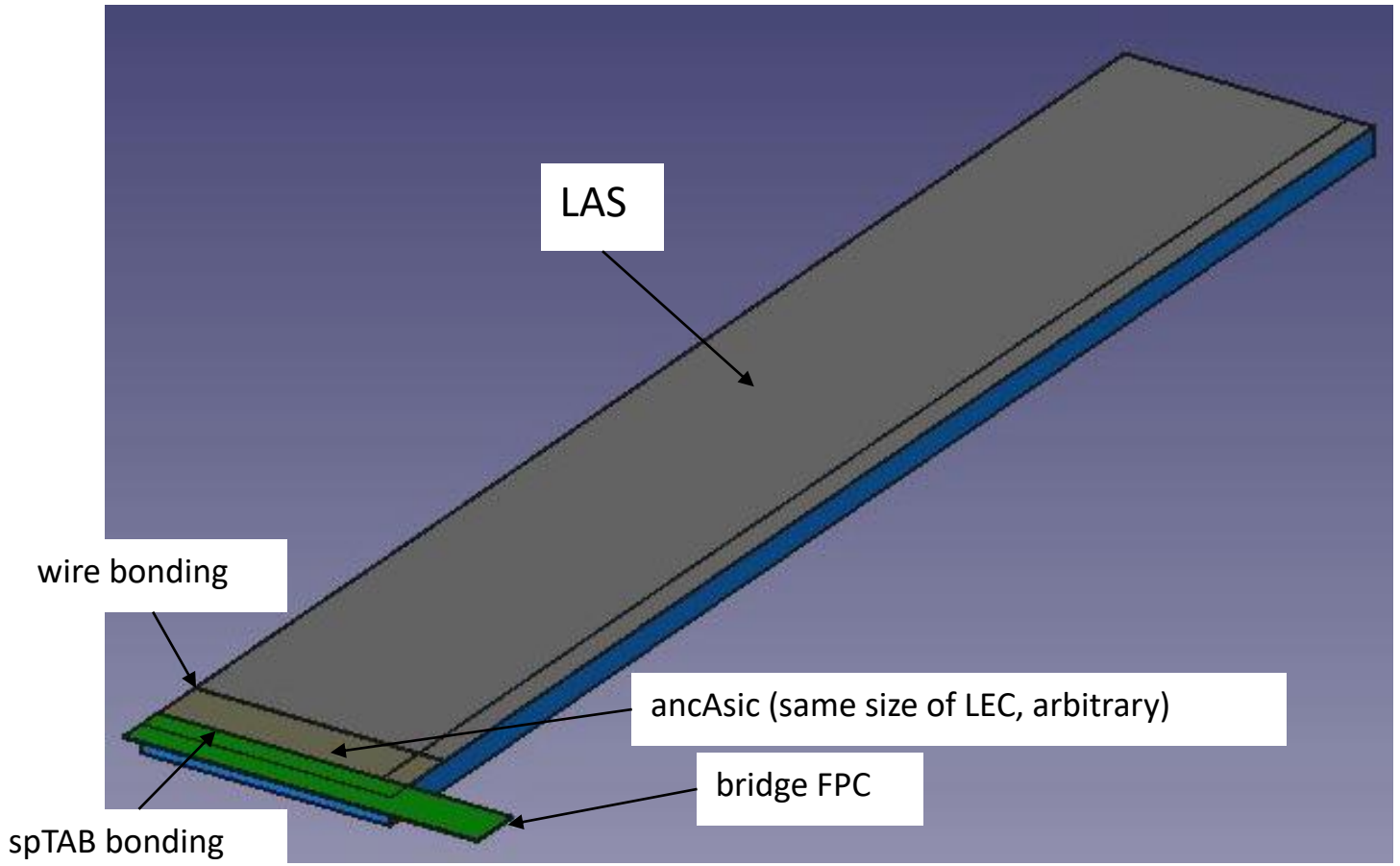
Layout

Module based approach to layout



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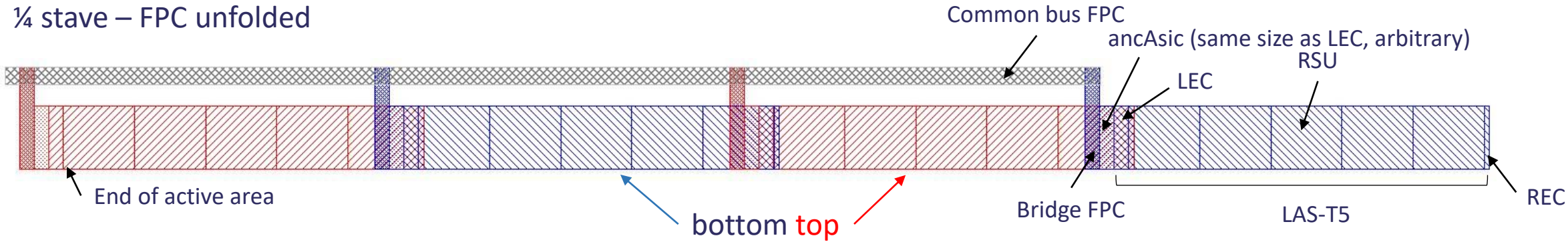
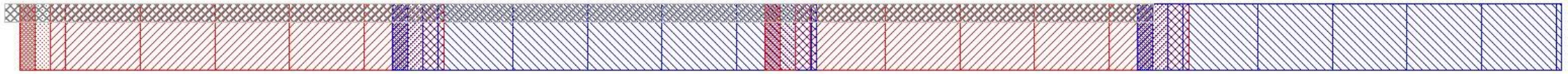
Modules/LAS on stave & FPCs

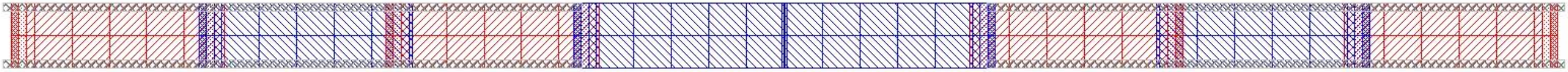
¼ stave – FPC unfolded



¼ stave – FPC folded



Full OB L4 stave w FPCs folded



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Bridge FPC: connects ancASICs to Common Bus FPC; Size: W: ~5mm; L: ~30mm;
Common bus FPC: connects FPC bridges to end of stave; Size: W: ~5mm; L: ~340mm;

Material budget

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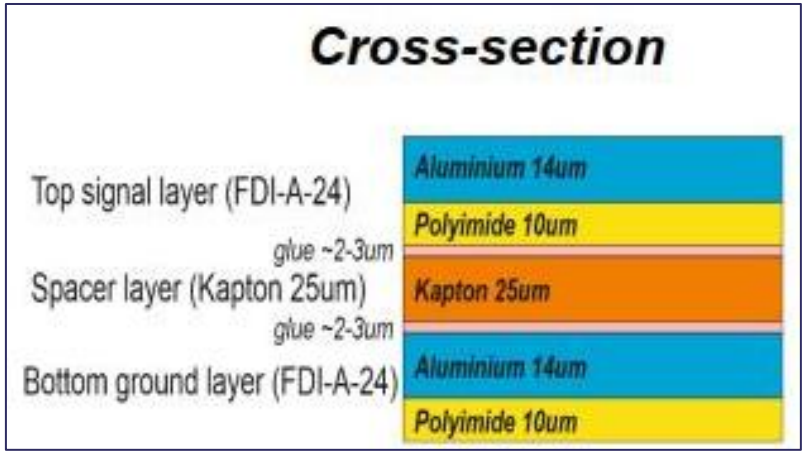
Cross-section estimate

	Components	Thickness	Material	X0 (cm)	X0 (%)	Comment
HIC	FPC metal layers	28	Al	8.897	0.031	14um/layer x 2 layers = 28um (FDI-A-24)
	FPC insulating layers 1	20	polyimide	28.57	0.007	10um/layer x 2 layers = 20um (FDI-A-24)
	FPC insulating layers 2	25	polyimide	28.57	0.009	
	FPC binding glue	5	TBC	39.07	0.001	real glue unknown, assuming Araldite 2011
	Pixel Chip	50	Si	9.37	0.053	
Total (FPC + Pixel chip)					0.102	
Total FPC only					0.049	Note FPC material budget closer to Pixel chip (0.053%X))

RPE LTU Ukraine



Proposed FPC stack-up for 100hom impedance tracks

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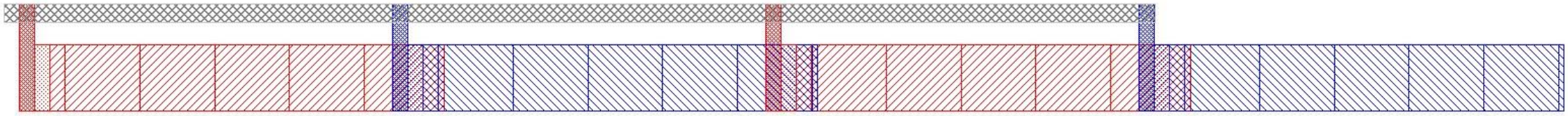
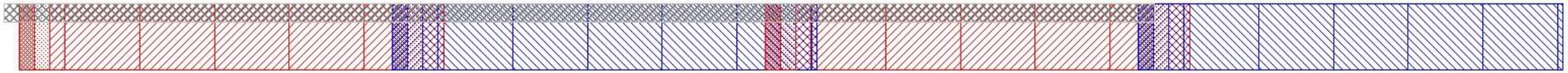
Estimate of material budget on stave (FPC and LAS only)

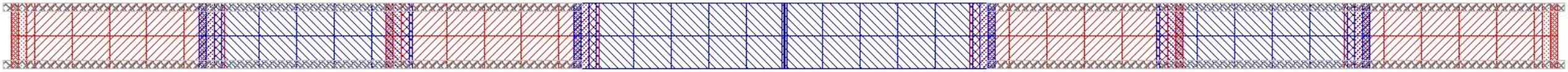
¼ stave – FPC unfolded



¼ stave – FPC folded



Full OB L4 stave w FPCs folded



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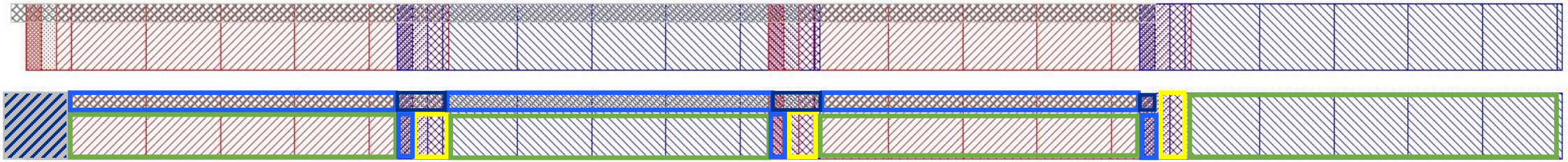

- → Si only: 0.053% X0
- → Si + FPC: (0.053 + 0.049)% X0 = 0.102% X0
- → Si + Si : (0.053 + 0.053)% X0 = 0.106% X0
- → Si + Si + FPC or Si + FPC +FPC: ~ (0.053 + 0.053 + 0.049)% X0 = 0.155% X0

Average material budget calculation in 0.25 OB L4 stave							
epciFpcDV2							
	X0 (%)	X (mm)	Y (mm)	Units	Area (mm^2)	Fraction	Avrg X0
Si only	0.053	95	14	3	3990		
		107	19	1	2033	0.738384	0.039402
Si + FPC	0.102	95	5	3	1425		
		4.5	14	2	126	0.190143	0.019369
Si + Si	0.107	9	19	1	171		
		9	14	2	252	0.051857	0.005534
Si + Si + FPC or Si + FPC + FPC	0.155	13.5	5	2	135		
		5	5	1	25	0.019615	0.003045
Total					8157	1	0.067349

Estimate considers only Si and FPC:

- No discrete caps and/or resistors;
- No shims or similar;
- No interconnection encapsulation;

Peak material budget:
~0.155% X0

Average material budget over 4 sensors:
~0.067% X0

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Corrugated prototype test pieces

Each piece → 2 layers 34 gsm veil + 5 layers resin

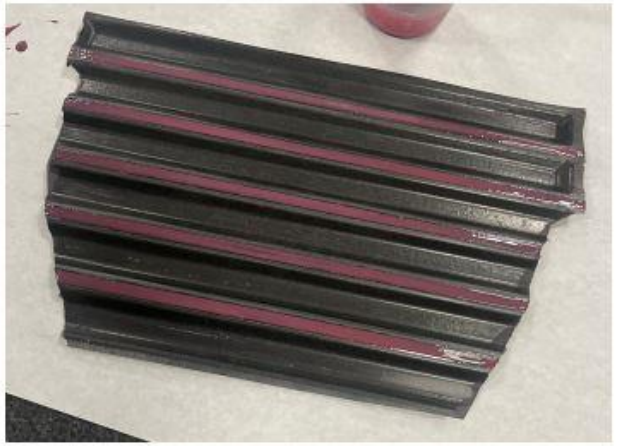
Face sheets glued with 9309 adhesive in 5 mm strips

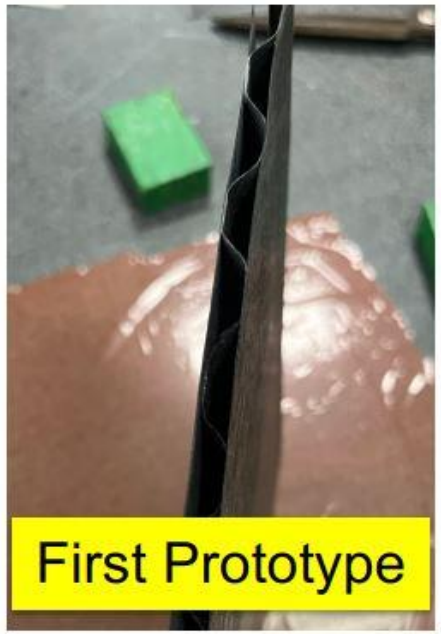
Final size of prototype test piece = 22.4 cm x 20.2 cm

Final weight of prototype test piece = 22.5 g

Density = 497 gsm → ~ 0.12% X/X0

Silicon ~0.05% X/X0, adhesive 0.01-0.02% X/X0





11

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Target material budget for L3 and disks is 0.25% X0.

Interconnection technology

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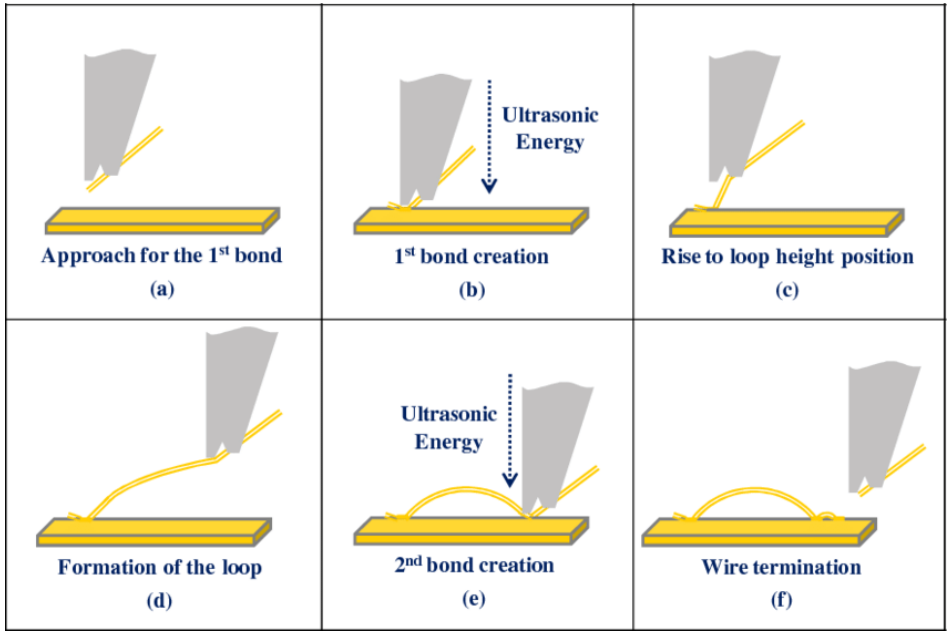
Options – wire-bonding

Potentially suitable to interconnect: Las to ancAsic

- Wire-bonding (Al wedge - wedge)
  - Pros:
    - Popular/standard technique across the community;
  - Cons:
    - Fragile: thin wire with raised wire profile;
    - Small cross section to conduct current (e.g. 25um dia wire);



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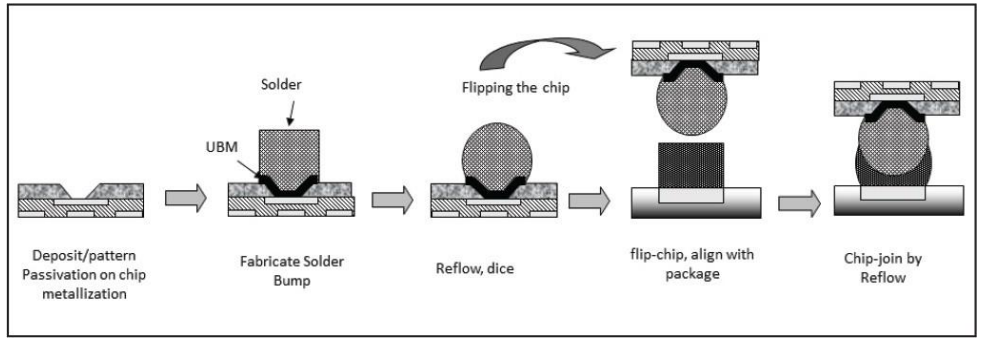
Options – bump-bonding

Potentially suitable to interconnect: ancAsic to FPC

- Bump bonding
  - Pros:
    - Larger cross section to conduct current;
  - Cons:
    - Need mainly external supplier, very few sites potentially equipped to do in house.
    - Thermal cycle Vs thermal mismatch: Si to FPC [~factor of 10]; Yield issue?
    - Less efficient cooling of AncASIC [sits on FPC]



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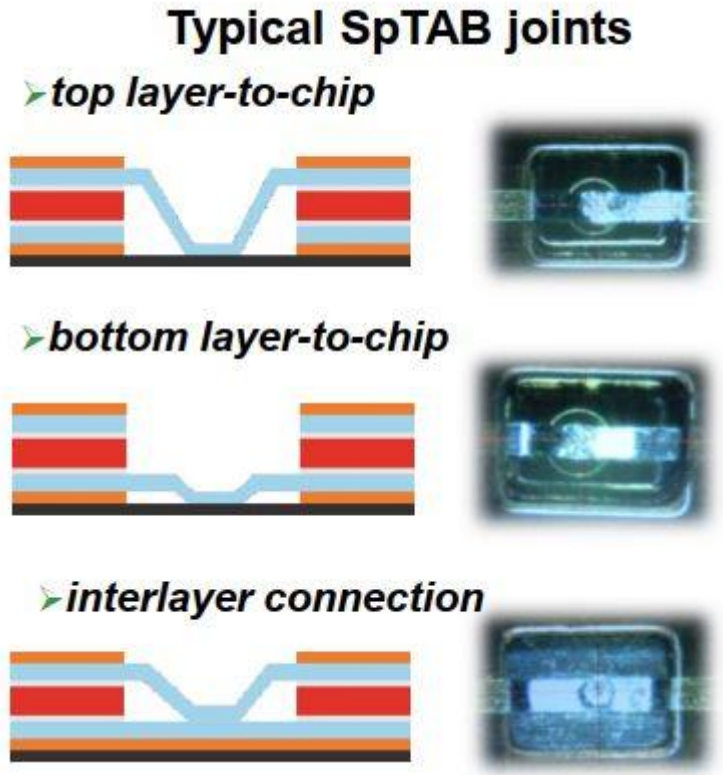
Options – spTAB

Potentially suitable to interconnect: ancAsic to FPC

- Single Point Tape Automated Bonding (spTAB):
  - Pros:
    - Large cross section to conduct current (e.g. 200um (width) x 14um (thickness));
    - Less fragile than wire bonding i.e. larger cross section and lower profile;
    - Uses wire-bonding machines, it requires specific wedge on wire-bonding machine; Commonly available across sites;
  - Cons:
    - Minimum pad size limited to ~70um;
    - Higher ultrasonic pwr than wire bonds, careful trade off width Vs thickness; Potential yield issue?
    - Is spTAB mostly supplier specific?
      - Research and Production Enterprise LTU, can do it;
      - Others? [Under investigation]



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1st low TRL prototype

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Test plan

- Foundation work to inform final design.

- Low TRL prototype:
  - Validate the supplier capabilities for Al FPCs;
  - Validate AC and DC signal integrity;

  - Quality of manufacturing against material budget for different suppliers;
  - AC signal propagation for meaningful rates, amplitudes and couplings;
  - DC signal distribution for meaningful currents and voltages;

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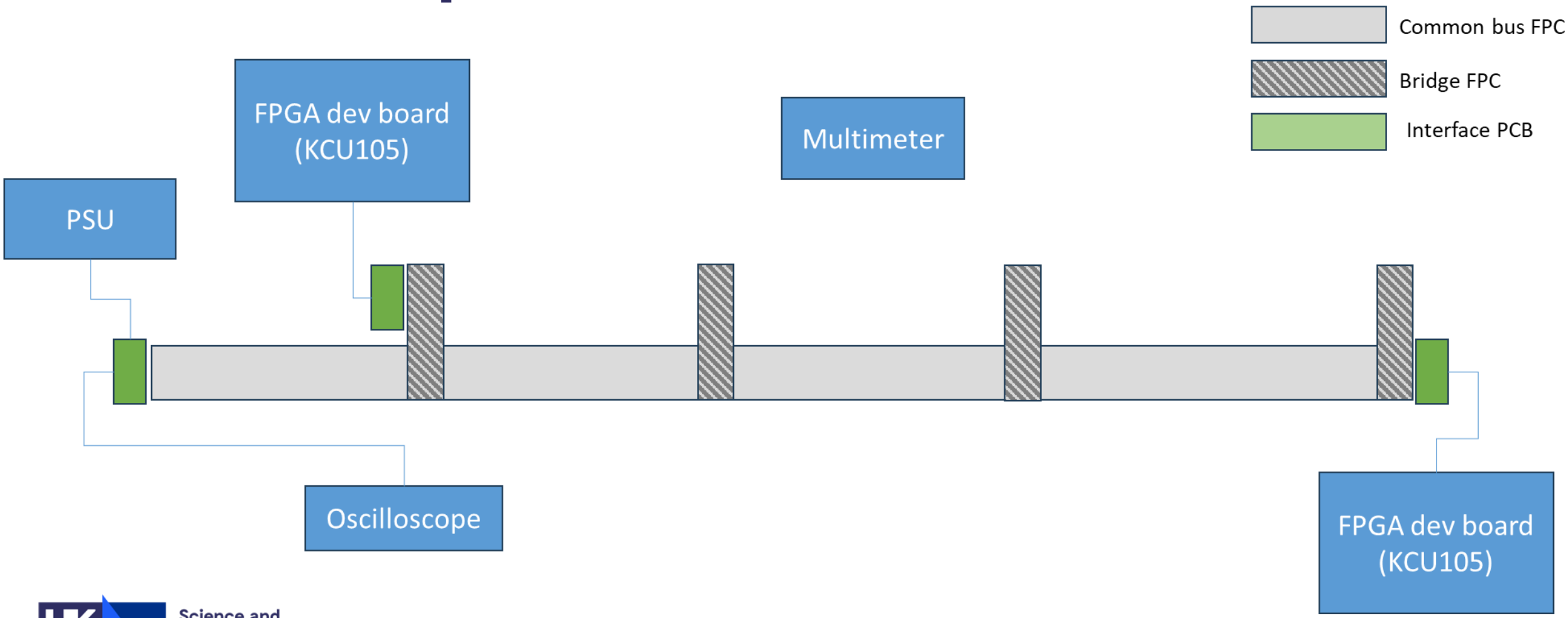
Test set-up



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Conclusion

- Presented outcome of the definition stage of a Low TRL prototype for the TDR;
- Design stage started;
- Next: procurement and testing (w Oxford)

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Interconnection capabilities

LBNL

Bonder:
Hesse Mechatronics
Bondjet BJ815 (General)
Bondjet BJ820 (Atlas)
Bondjet BJ855 (Atlas)

Bonding wedge:
SPT- FP45-W-2020-1.00-CM
W=003 VW=004 VR=0075 45RA2

Tab bonding wedge
SPT- 7000A-W-10060-1.00-M
TDF=046 X=040

Wire:
Heraeus Malaysia
Al
DIA: 25um
EL:1-4%
BL:15-17g

RAL

5 x automated Hess bonders, configured for Al wedge, one is also able to do Au-ball bonding. We also have a small manual bonder, capable of doing Al-wedge, Au-ball, ribbons, heavy wire and tab (depending on weight of media), but no targetting aids on that one, so just have to line it up as best as you can under a microscope.

We also have a separate TPT machine which was bought and is configured purely for SpTAB on ATLAS staves.

All of the above have various amounts of spare capacity, but I expect 2-3 automated bonders will be fully utilised on ATLAS ITk upgrade work. The TPT will need to be reserved for that too, but should have at least some spare capacity if something else needs TAB bonding.

The other machines (2x automated and 1x manual have reasonable spare capacity for ad-hoc or small production jobs. None of the bonders are readily available for 'non-standard' work, e.g. if wire and tool need changing, this will have to be more carefully scheduled around other work and will carry some overheads to retool to the non-standard and then back afterwards. Ideally, we keep most machines in a standardised state and only modify a single process development machine (an older Hesse bonder).

Notes

- DC supply filtering for sLDO: decoupling caps;
- Pwr consumption of FPC;
- Ground folded down;
- Type of connector at end of stave?
- Broadside coupling of transmission lines;
- All components radiation hard;
- Termination resistor at receiver end;
- Vias by LTU?