**AstroPix Wafer Testing - BIC ePIC meeting - March 8, 2024 (Friday) -**

https://indico.bnl.gov/event/22373/

Attendee: Sylvester, Jessica, Sanghoon, Bobae, Flera, Henry, Hwi Dong, Jared, Jeongsu, Maria, Manoj, Nicolas, Richard, Vitaliy

Current work progress at Korea - Sanghoon Lim

- ALICE ITS2
    - Scale is smaller than BIC
    - 60 m2
    - Testing at level of chip and not at wafer
    - 8% sent to CERN
    - CERN has wafer testing maachine - 8% tested at wafer level
    - Company do post processing thinning and dicing
    - Dice and tested at chip level
    - Post processing does not affect - test procedure
    - Two different machine
        - Pusan and Yonsei
        - ALICIA
    - ALICE Machine
        - Shown Bonding plan and probes
        - Two different modes
            - Chip test mode
        - Probe cad moves to position
        - Elctrical contact test (UI)
        - Complete the tests
    - Testing Time
        - 3 minutes for probe measurements
    - Tests (1M pixels - ALPID)
        - Threshold scan - tuning threshold is important
        - List of chip test procedure on slide 6 for ALPID (50 um chip)
        - prowering , IV, DAC, power on reset, SEU, FIFO, Data port, Digital Scan, etc.
    - Probe card for ALPIDE
        - DAQ board, proximity card, Carrier Card with probes
        - Local company
            - Moved proximity card to probe card itself
            - Received the design file singel chip carrier board
            - Use same probes as shown in AstroPix v3 schematic
- AstroPix Probe Card
    - Working on how to utilize knowledge/infrastructure from ALPIDE
    - Start designing in April
        - First testing with single chip - May-ish
        - Need to find different company to put needles (probe card)
    - Need to update the testing
    - For v3, start with single chip testing

        - Like to have both single chip and wafer
    - Comflict between ALICE and ePIC (use of machine) - Jessica
        - 2 or 3 years later ALICE mass production starts - Sanghoon
        - Don't think there is actual conflict in production- Sanghoon

AstroPix wafer testing - Nicolas

List of test for wafer level testing

- Slide 2 shows list (based on Sanghoon's presentation in lst meeting)
- IV
- Power Measurement
- SPI commands - routing, configuration, readout
    - Need configuring the chip
    - Idle bytes toggling, correct header, payload
- Daisychain
    - Inject data from right to left
- Threshold Scan, Tuning
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- What is best way to handle guard rings - Manoj
    - It is Floating, not important for wafer level testing
- Is it important to have readout - Manoj
    - More inclusive list for now and then take a look in detail – Jessica
    - No way to know that what is not needed
    - So have a inclusive list - check many things as we can
- Does configuration have any readback - Vitaliy
    - Only can readback the configuration by Shift register base and not by SPI - Nicolas
    - On module, would the shift register be available or not -Vitaliy
        - No it is not able
        - Possible to implement SPI readback but not implemented
    - **Follow Up on implementation of SPI readback**

Documentation

- QC document in place by workshop in May (Sanghoon to prepare)
    - Start with what Sanghoon and Nicolas showed
    - Measurement should be compatible with system
    - Start to identify range of values we are looking for (range where we can say chip is good or bad)
- If there any other discussion or suggestions about any other tests during QC test
    - Some type of energy calibration - Jessica
        - Right now at module level or stave level - Jessica
    - Any thoughts by anyone for initial QC testing ?
        - No comments
        - Lets thick about it and add it to the list temporarily
- Can provide some templates of these documents - Jessica