ePIC Silicon Vertex Tracker R&D

eRD104: Services Reduction
eRD111: Modules, Mechanics, Cooling and Integration
eRD113: Sensor Development and Characterization

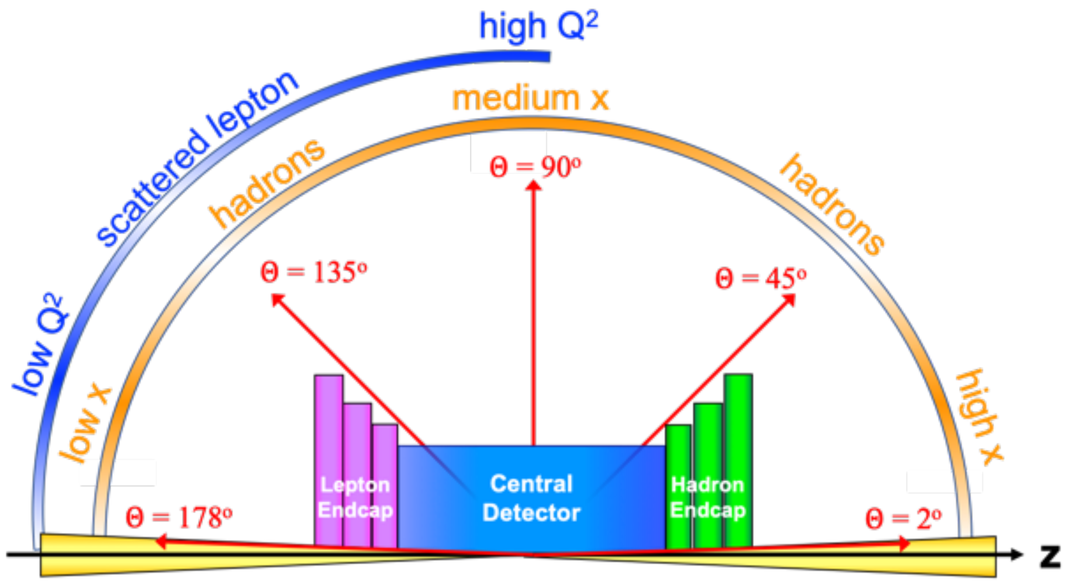
Ernst Sichtermann (LBNL)
for the ePIC SVT Detector Subsystem Collaboration

ePIC / EIC Project R&D Day
https://indico.bnl.gov/event/22388/

Outline

- Introduction
- Sensor and Characterization
- Service Reduction
- Modules, Mechanics, Cooling and Integration
- Outlook

ePIC Tracking Resolution Requirements



	Momentum Resolution	Spatial Resolution
Backward (-3.5 to -2.5)	~0.10%×p⊕2.0%	~ 30/p_T μm ⊕ 40 μm
Backward (-2.5 to -1.0)	~ 0.05%×p⊕1.0%	~ 30/p_T μm ⊕ 20 μm
Barrel (-1.0 to 1.0)	~0.05%×p⊕0.5%	~ 20/p_T μm ⊕ 5 μm
Forward (1.0 to 2.5)	~0.05%×p⊕1.0%	~ 30/p_T μm ⊕ 20 μm
Forward (2.5 to 3.5)	~0.10%×p⊕2.0%	~ 30/p_T μm ⊕ 40 μm

ePIC SVT Detector Subsystem Collaboration

- The overarching goal is the development and construction of a well-integrated full tracking and vertexing detector subsystem for the ePIC project detector based on 65nm MAPS sensors
- ePIC SVT DSC has its origins in the EIC Silicon Consortium,
- Kickoff meeting provides an overview — https://indico.bnl.gov/event/19823/
- SVT workfest at the January 2024 collaboration is another good pointer — https://indico.bnl.gov/event/20473/sessions/6736/#20240109

Participating Institutions

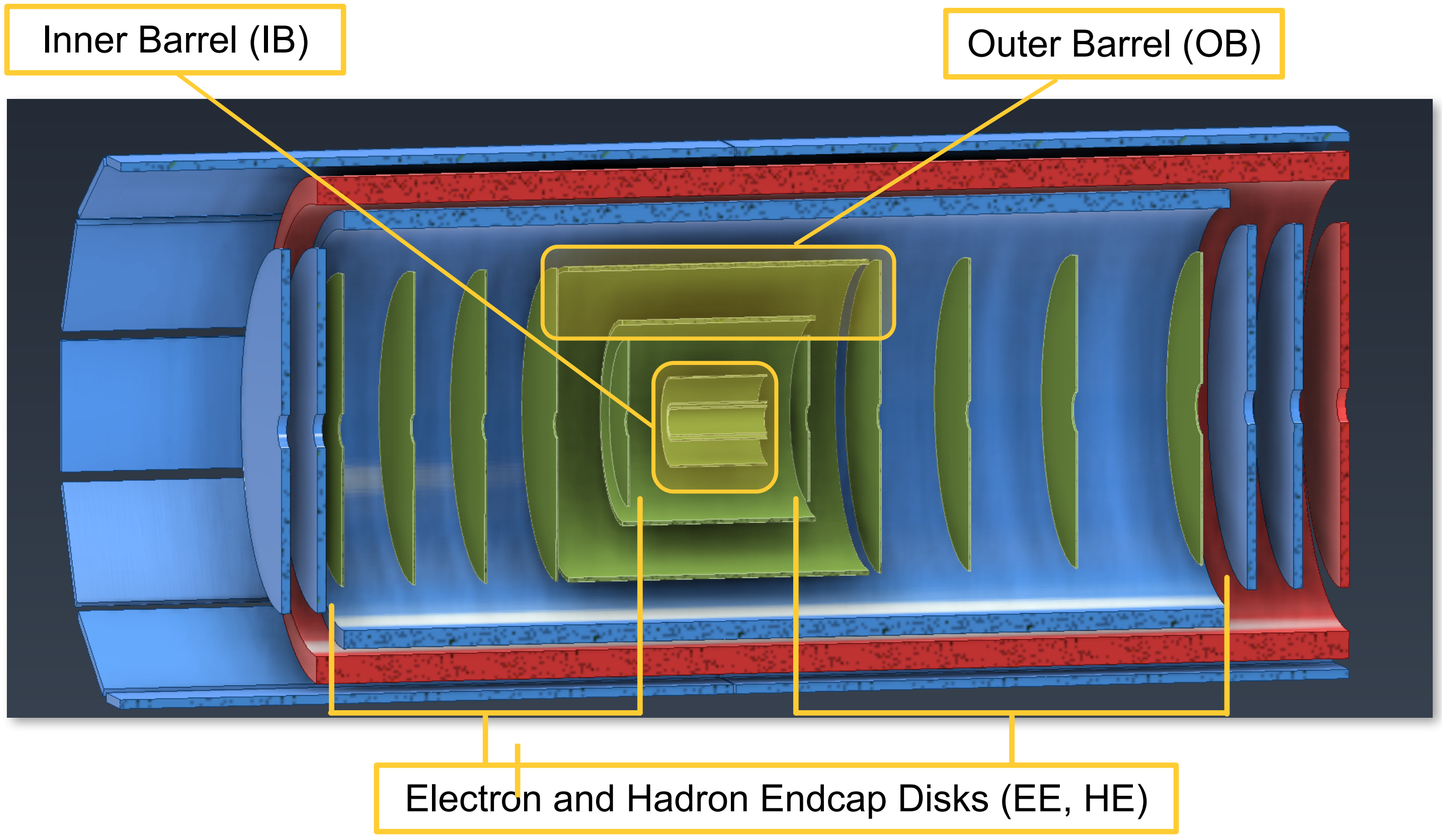
Extensive Si-detector experience in the ALICE, ATLAS, CMS, sPHENIX, STAR collider experiments

SVT Concept

- **Inner Barrel (IB)**
  - Three layers, L0, L1, L2,
  - Radii of 36, 41, 120 mm
  - Length of 27 cm
  - X/X_0 ~ 0.05% per layer
  - Curved, thinned, wafer-scale sensor,
  - Approx. 20μm pixel pitch

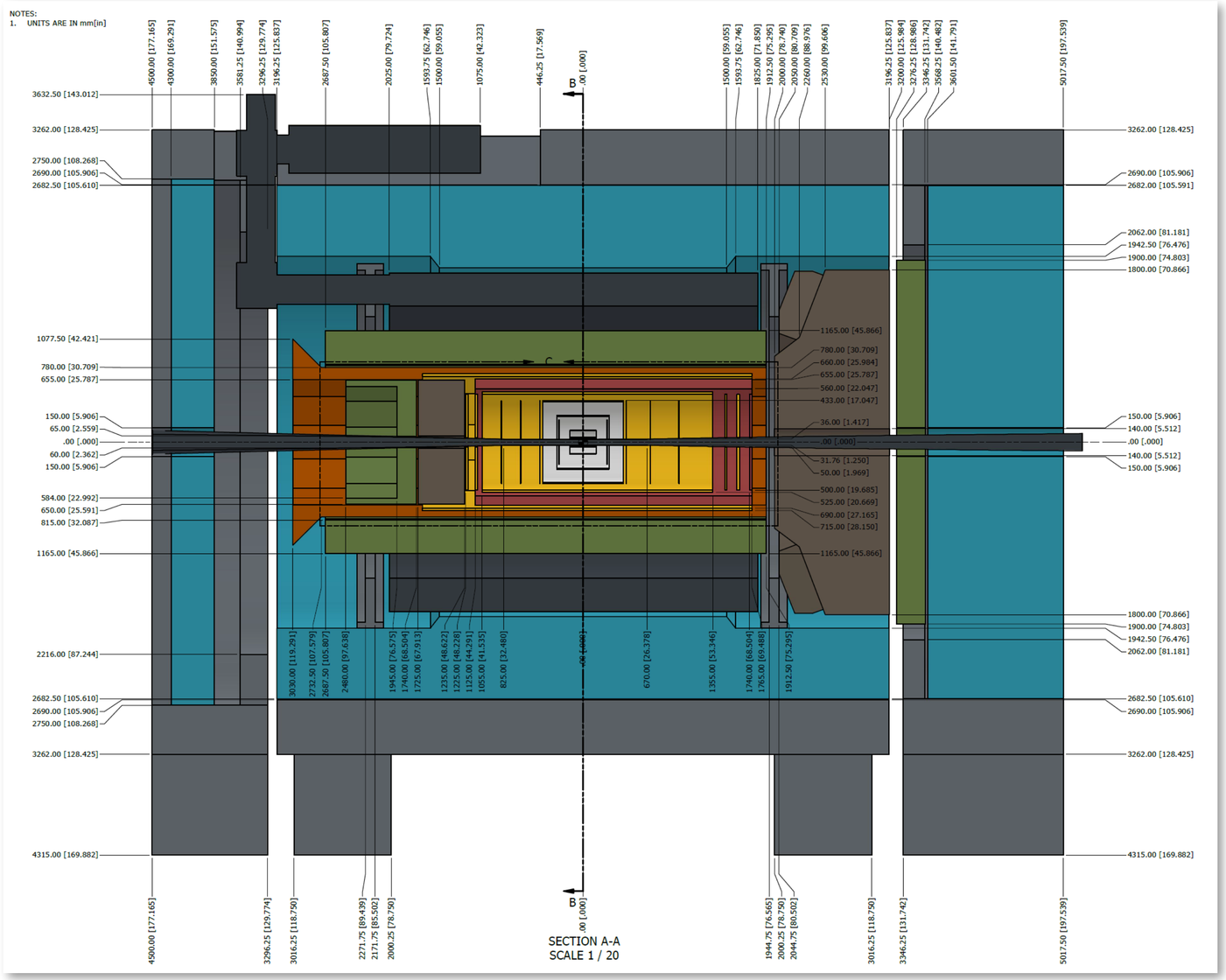
- **Outer Barrel (OB)**
  - Two layers, L3, L4
  - Radii of 27 and 42 cm
  - X/X_0 ~0.25% and ~0.55%
  - More conventional structure w. staves
  - Sensor derived from IB sensor

- **Electron/Hadron Endcaps (EE, HE)**
  - Two arrays with five disks
  - X/X_0 ~0.25% per disk
  - More conventional structure
  - Sensor derived from IB sensor; common with OB



- **Lengths for L2—L4 increase so as to project back to z = 0; disk radii adjust accordingly**

SVT outer dimensions and integration in ePIC



Spatial extent along the beam axis:

$-106.25 < z_{SVT} < 136.25$ cm

Radially:

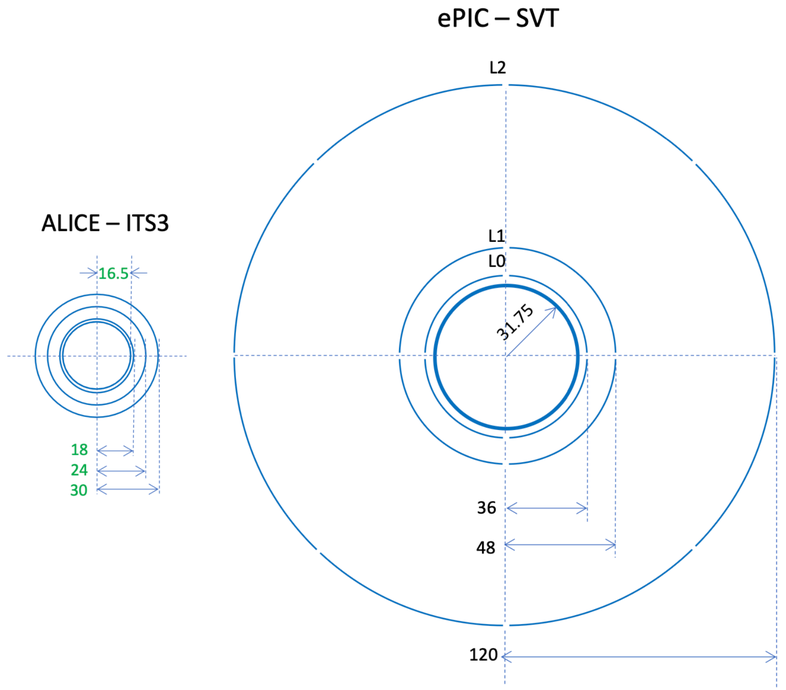
$r_{out} < 43.00$ cm

$r_{in}(z)$ determined by beam-pipe + 5mm

Beam-pipe bake-out with SVT installed; clamshell of detector halves,

ePIC SVT R&D

At a high level, the ePIC SVT thus requires us to develop:



1. ITS3-like Inner-Barrel layers

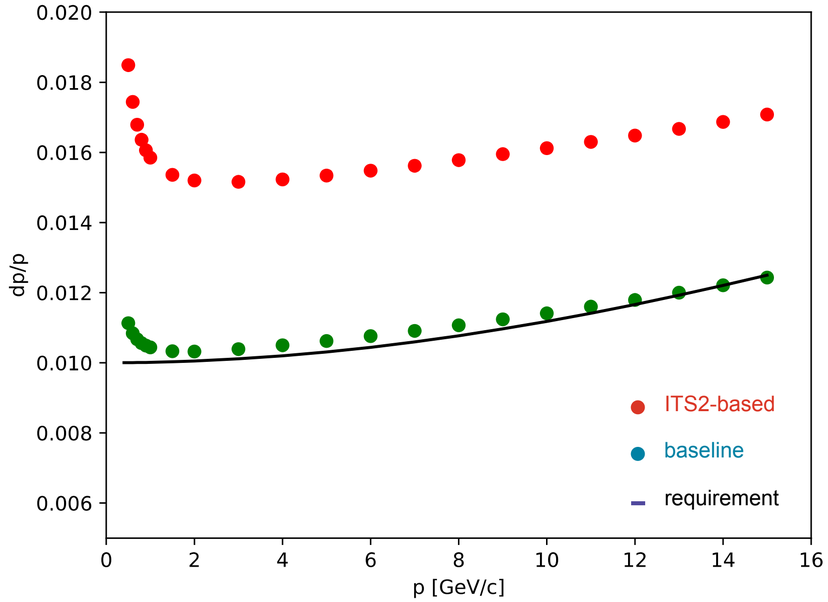
- Re-use the ITS3 sensor as is
- Adapt the ITS3 detector concept to the EIC:
  - Mechanics of bent layers — sensor and support — for the larger EIC radii
  - Services and cooling design and routing for the EIC acceptance requirements
  - Considerations related to in-situ beam-pipe bake-out at the EIC

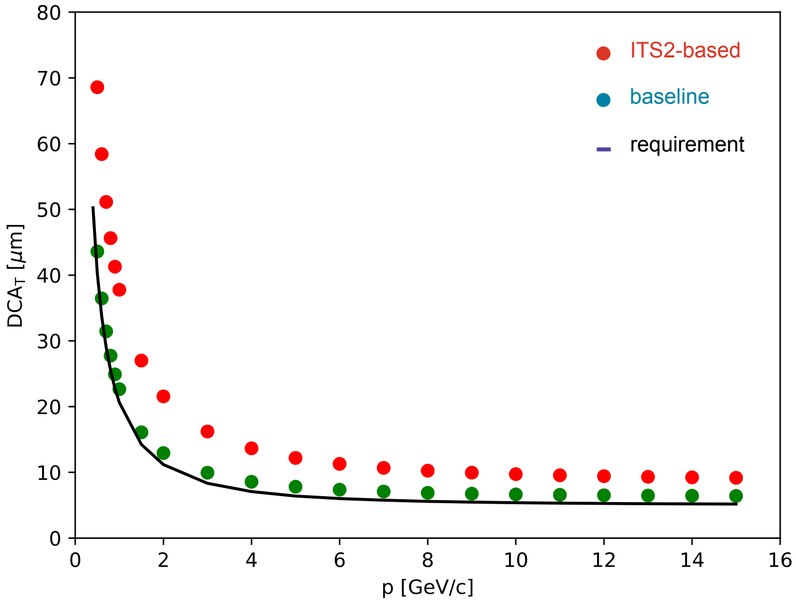
2. EIC variant for the staves in the Outer Barrel and the Endcap Disks

- EIC Large Area Sensor (LAS), i.e. ITS3 sensor size optimized for large-area coverage, yield, and cost
  - EIC LAS will be stitched, but not to wafer scale; functionality and interfaces stay largely unchanged
  - Size(s) of the EIC LAS defined by requirements for full coverage and yields, cost; currently 5 and/or 6 RSUs
  - Approximately 4,000 EIC-LAS sensors will be used in the OB and Disks,
- More conventional carbon composite mechanical support structures with integrated cooling

Recently/Frequenty Asked Question — Can SVT be done with ALPIDE?

- NAS Science Assessment was followed by the Community Yellow Report to develop the associated detector requirements,
- We take the tracking and vertexing requirements as guidance and illustrate the performance of an ITS2-based approach in comparison with our baseline,
- The following results are from fully consistent and up-to-date fast simulations that include multiple scattering, digitization, and Kalman-filter based tracking,
- The momentum resolution (top) for backward angles, ~165^{o} corresponding to η = -2, is shown. Tracks at this angle traverse all backward disks. Note that the detector is quite constrained in this region and possibilities for rearrangement are nearly non-existent. The geometrical configuration is identical, but X/X_0 is assumed to be 0.50% per disk and the pixel pitch is 28 μm in the ITS2-based approach. The curve shows the requirement, the green points show the projected baseline performance, and the red points show the projected ITS2-based performance,
- The single-track DCA (bottom) is shown at mid-rapidity. The innermost barrel layers, L0 and L1, play a key role in this quantity. An ITS2-based solution entails additional material associated with its more traditional mechanical structure and cooling. X/X_0 is assumed to be 0.35% per layer for these layers and the pixel-pitch is 28 μm in the ITS2-based approach. The curve shows the requirement, the green points show the projected baseline performance, and the red points show the projected ITS2-based performance,
- Since ePIC offers essentially no possibilities for reconfiguration of the lever-arm or radii in these regions, an ITS2-based approach will not achieve the requirements.





SVT R&D

Project R&D for the ePIC SVT is organized in three areas:

- **eRD104** — services reduction
  - Investigates methods to significantly reduce the services load;
  - Powering system
  - Readout system

- **eRD111** — modules, mechanics, cooling, and integration
  - Development of a full tracking detector solution composed of next-generation 65 nm MAPS;
  - Forming modules from stitched sensors
  - Barrel and Disks
  - Cooling
  - Mechanics and integration

- **eRD113** — sensor development and characterization (started in FY23)
  - Development of the EIC MAPS;
  - Sensor design
  - Sensor Characterization

In addition, the SVT relies on Project Engineering and Design support and significant in-kind contributions.

The SVT does *not* rely on the Generic EIC-related R&D Program, c.f. https://www.jlab.org/research/eic_rd_prgm. However, several members of the ePIC SVT DSC are part of submitted proposals to that program.

Sensors and Characterization

Sensor Choice

Technology of choice for the SVT is Monolithic Active Pixel Sensor,

This choice was made following a technology survey, c.f.

> Laura Gonella on behalf of eRD16 and eRD18, *“EIC Silicon Vertex and Tracking: Technology Survey”* at the 1st EIC Yellow Report Workshop

Drivers include high granularity, low power consumption, and low material, as well as synergies with large-scale developments in the broader community – in particular the ALICE-ITS3 development,

Pragmatic choice to seek to join the ITS3 development and adapt, where needed (and only there!), the sensor, called “MOSAIX”, for use in the SVT,

Large SVT area of ~8 m^2 is one of the drivers in the need to adapt ITS3 to become EIC-LAS; same for the choice to use an ancillary IC to provide serial powering, bias voltage, and multiplex slow controls,

Formal partnership with ITS3 now in an advanced stage.

ITS3 Wafer Scale Sensor — Development Path

- **MLR1** - Submitted Q4 2020
  - **Technology exploration** and prototype circuit blocks for future sensors
  - Large number of test structures; including Analogue and Digital Pixel Test Structures (APTS, DPTS)

- **ER1** - Submitted Q4 2022
  - Exploratory designs (MOSS, MOST sensors) for **proof of stitching principles**, learning methodology and yield
  - Also, small prototypes and test chips

- **ER2** – Design ongoing, submission in 2nd half of 2024
  - **MOSAIX** sensor aims to satisfy ITS3 requirements
  - Not an evolution of MOSS/MOST; substantial redesign of existing circuits, with new features

- **ER3** – Production version
  - Minimal modifications to MOSAIX

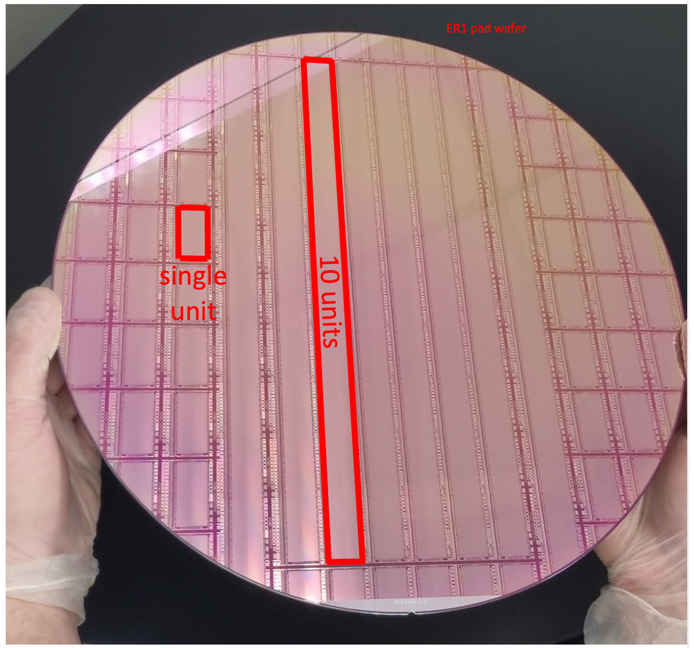
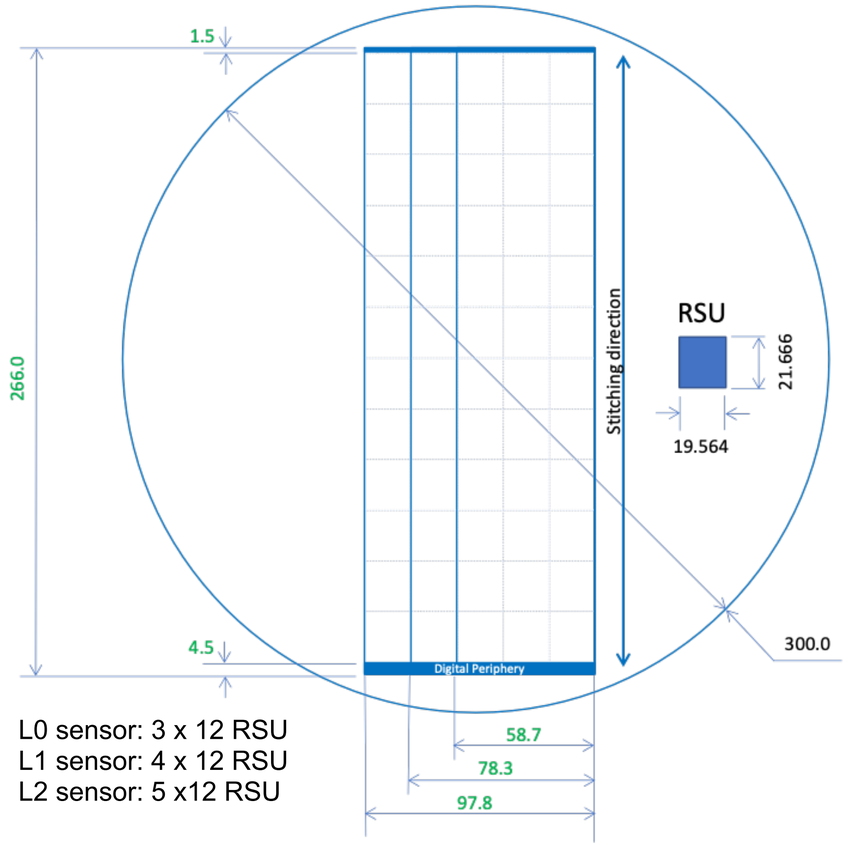


Figure credit: Gianluca Aglieri Rinella, Walter Snoeys — https://indico.cern.ch/event/1280150/

MOSAIX

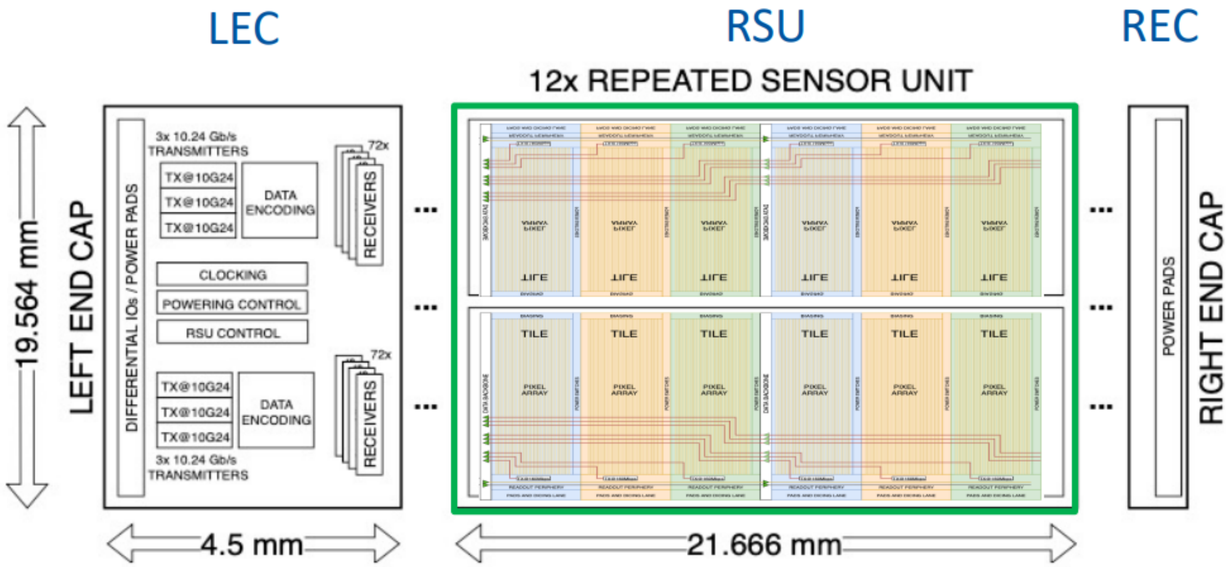
- Complex circuit designed, led by ITS3 team at CERN
  - Approximately 30 FTE of designers working on the submission, including ePIC SVT designers



L0 sensor: 3 x 12 RSU
L1 sensor: 4 x 12 RSU
L2 sensor: 5 x12 RSU

ER2 sensor widths

19.564 x 3 = 58.692
19.564 x 4 = 78.256
19.564 x 5 = 97.820



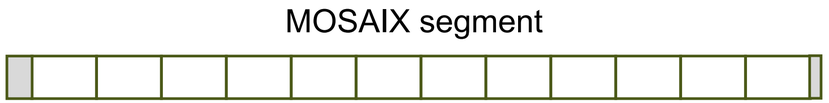
Pixel size: ~ 20 x 22 μm^2
Frame duration: 2 to 5 μs
Data link: 10.24 Gbps

EIC Large-Area-Sensor (EIC-LAS)

- The ePIC SVT OB, EE and HE will cover an area of approximately 8 m^2
- A sensor design is needed for **low-cost, high acceptance, large area coverage**
- The EIC LAS sensor will be based off the ER2 and ER3 designs with modifications for use in the SVT
- Modifications of MOSAIX are kept to a minimum
  - Work within the available time and resources
  - Reduce risk of submission failure

MOSAIX to EIC-LAS

Inner Barrel



- 12 RSUs
- 8 data links
- 7 slow control links
- Direct powering

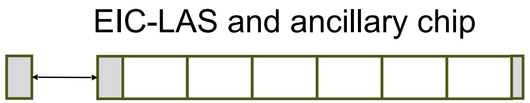
Improve yield and coverage

Lower material budget

Lower material budget, fit integration requirements

Lower material budget, fit integration requirements

Outer Barrel, E/H Endcaps



- **5 or 6 RSUs**
- **Single data link**

EIC-LAS

- Multiplex slow control
- Serial powering

Ancillary ASIC

Partnership with ITS3 — CERN-EIC agreement

- Meeting at CERN in April 2023: EIC, ePIC SVT, ALICE ITS3 → Agreed on partnership

- Draft of agreement received in December 2023
  - Further discussions with ITS3 colleagues on ER2 and ER3 sensors procurement
  - Now with BNL legal

- The agreement provides a collaborative framework around four main points
  - **Procurement of components** for the EIC ePIC detector (includes ER2)
  - **Participation in the design** of the Pixel Sensor Chip for the ALICE ITS3
  - **Transfer of the design database** of the ITS3 sensor to BNL
  - **Contribution to other CERN activities** related to the ALICE ITS3

ePIC SVT Designers' Group

- Two sensor designers affiliated with ePIC institutions (BNL, MIT) are embedded in the ITS3 team at CERN
  - As per CERN/EIC agreement
  - Transfer of knowledge to the ePIC designers for EIC-LAS

- Complemented with team of experienced designers in the UK (RAL) and the US (BNL, LBNL)

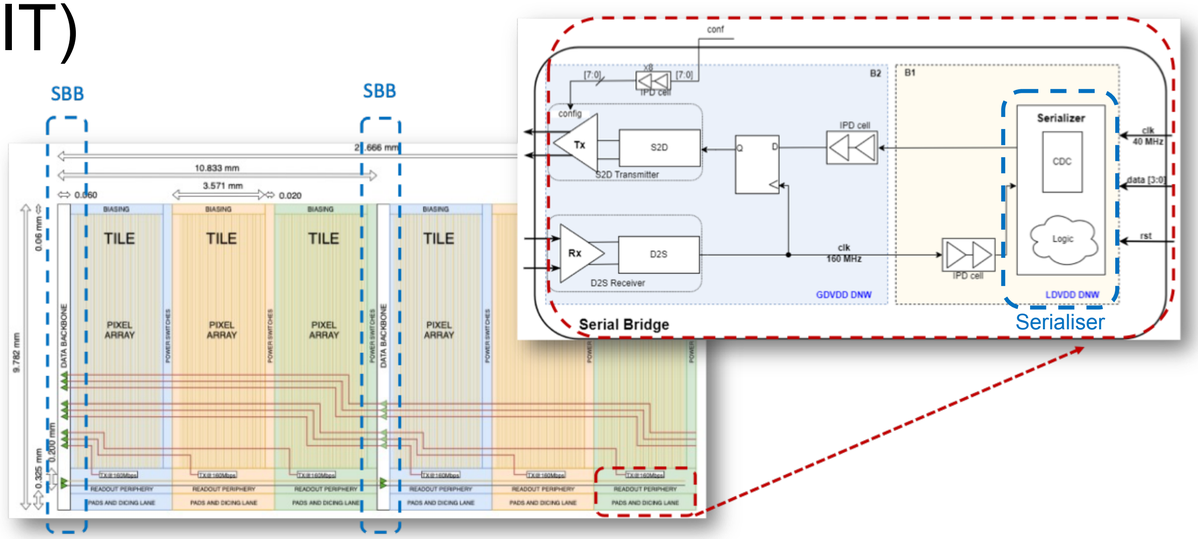
- Bi-weekly WP1 Sensor Design meetings (co-conveners: I. Sedgwick, RAL; J. De Melo, BNL)

- Tools for collaborative work in place and being set up
  - Cliosoft being setup by BNL for collaborative working on sensor designs
  - Action tracker, specification document, schedule gannt project, shared document repository

MOSAIX Design – ePIC contributions

- Development of **logic libraries** (RAL, LBNL)
  - Enhanced Design for Manufacture (DfM) rules, reduced leakage current for improved power consumption, specialised cells for use in the pixel array
  - Overall management of the effort, library generation (netlists, abstracts etc) and verification of the generated cells by ePIC SVT designers, with layout work split across several institutes on the MOSAIX team

- Work on MOSAIX tile circuitry (BNL, MIT)
  - Stitched backbone
  - Tile serialiser



EIC-LAS

- Specification capture in progress
- Access to MOSAIX database needed to start work
  - Pending progress with agreement signature

65nm EIC-LAS Specification				
Specification	Unit	Value	Comment	Status
Number of RSUs	N/A	5-6 (TBD)		
Output Data Channels	N/A	1-2	1 if no redundancy, 2 if redundancy desired	
Data Output Speed	Gbit/s	10		
Power	W			
Supply Voltage	A			
Area	μm^2			

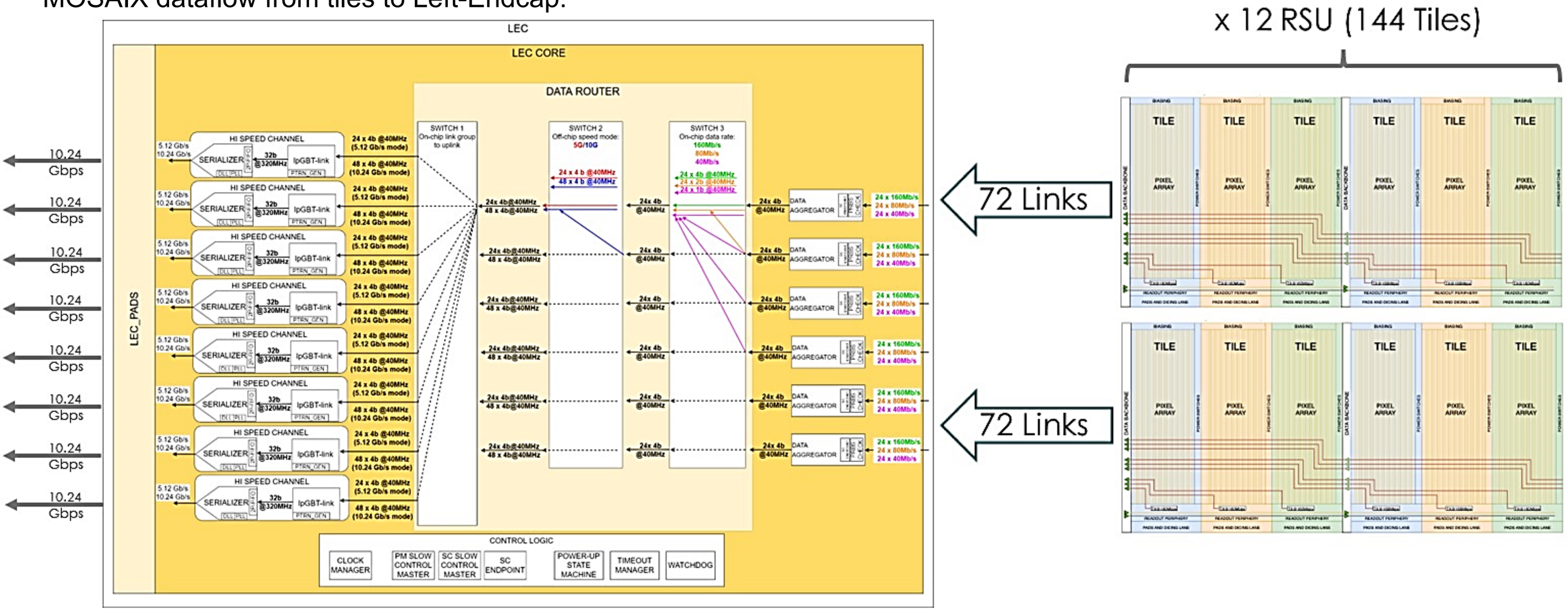
- Estimated power consumption range: 1.2 – 1.6 W per EIC-LAS
  - Derived from evolving MOSAIX power figures
  - This estimate takes into account the reduction in the number of RSUs
  - LEC power consumption not yet scaled to reflect the reduction in the number of data links
    - More information needed on power consumption of various LEC blocks
    - Significant reduction in power consumption expected

EIC-LAS — Work Ahead

Reduction from 12 RSUs per segment to 5 and/or 6

Reduction of data links to one per EIC-LAS

MOSAIX dataflow from tiles to Left-Endcap:



Both modifications require access to the design database.

Sensor Testing and Characterization

- Effort within ePIC SVT WP2 Sensor Testing (co-conveners: G. M. Innocenti, MIT; L. Tomasek, CTU Prague)

  - **Covers ITS3 sensors, EIC-LAS and AncASIC, including test setups development**
  - **MLR1 essentially done; ongoing efforts on ER1, preparations ongoing for ER2**

- Characterisation of prototypes
  - Tests — characterization, DAQ development, thermal, irradiation — in labs and test beams
  - Development of wafer probing capability for production
  - Irradiations at SVT facilities

- Production testing/QA
  - Probing of all ER3, EIC-LAS production, AncASIC production wafers

Sensor Testing and Characterization — Facilities

- Clean rooms and labs equipped with radioactive sources, climate chambers, wire bonders, wafer probers, etc at multiple institutions

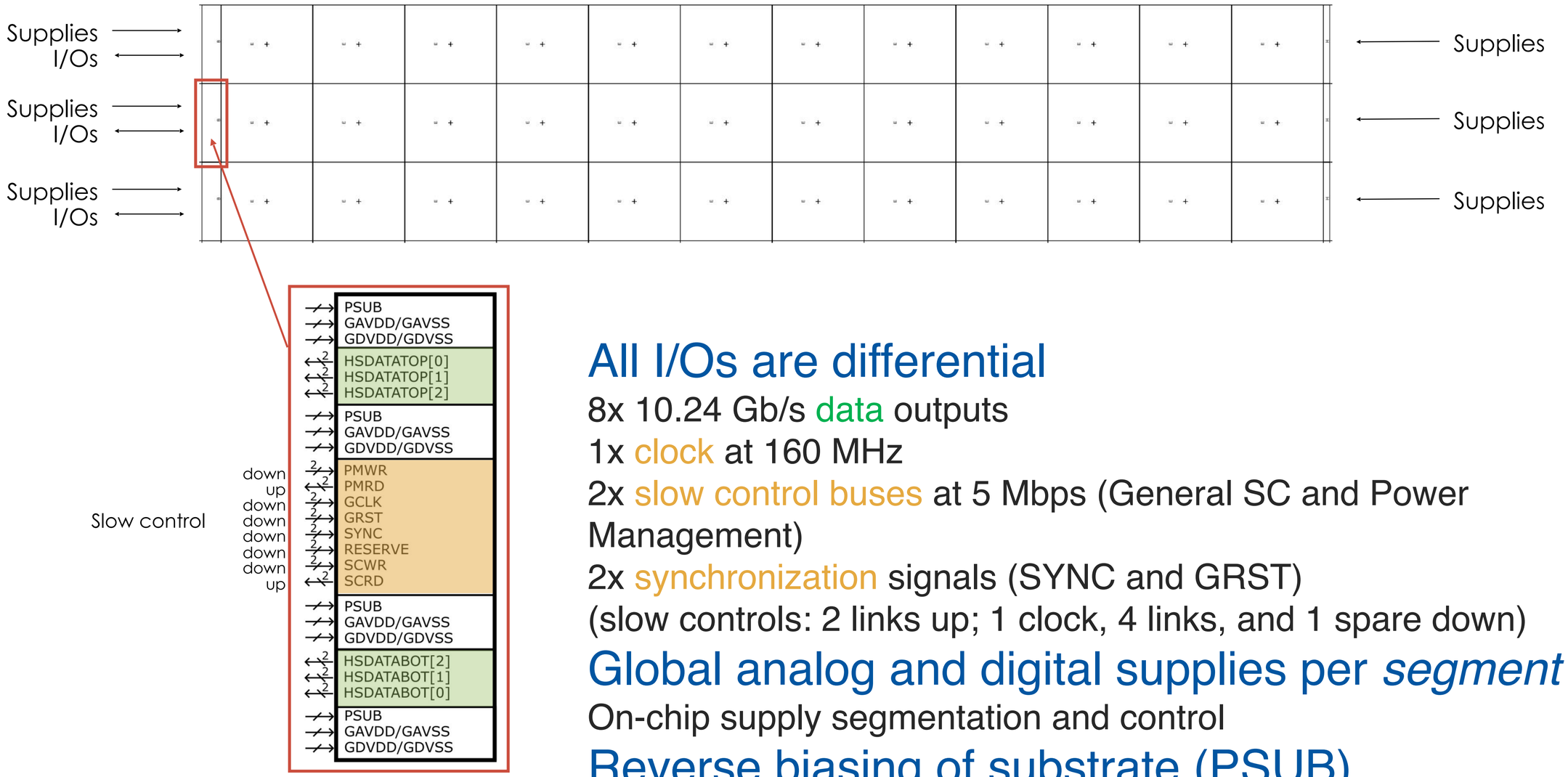
- Irradiation facilities in the collaboration available for displacement damage, TID and SEE testing
  - Birmingham: 27 MeV protons, upcoming neutron irradiation facility
  - CTU Prague: X-ray source, slow and fast neutrons
  - UJP Prague: Cobalt-60 gamma ray
  - Nuclear Physics Institute CAS Rez: reactor neutrons, ~30 MeV proton and heavy ion beam, electrons up to 25 MeV
  - LBNL: BASE @ 88” cyclotron (protons, heavy ions, neutrons)
  - Daresbury lab: X-ray source
  - LANL: 800 GeV protons

Service Reduction

Service Reduction

- Services are strongly coupled with sensor,
- Traditionally powering forms a leading contribution to the service load; readout and slow-control are key as well,
- Four power domains, bias voltage, and need to multiplex slow-control incorporated in a single Ancillary IC,
- Work organized across WP1, WP2, and WP5 Readout and Powering (co-conveners: J. Glover, Birmingham; J. Schambach, ORNL)

MOSAIX Interfaces in the Left End Cap (LEC)



All I/Os are differential

8x 10.24 Gb/s data outputs

1x clock at 160 MHz

2x slow control buses at 5 Mbps (General SC and Power Management)

2x synchronization signals (SYNC and GRST)

(slow controls: 2 links up; 1 clock, 4 links, and 1 spare down)

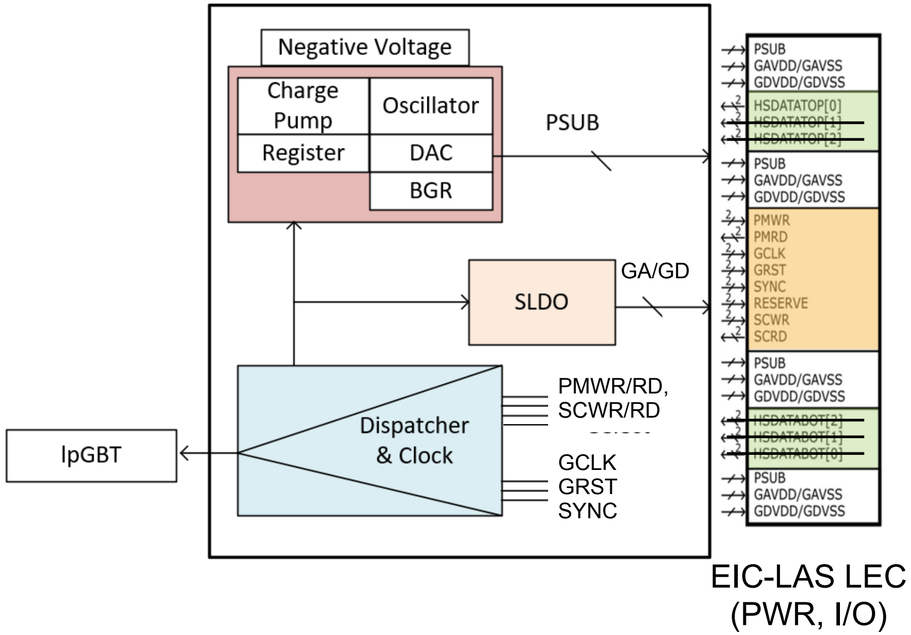
Global analog and digital supplies per *segment*

On-chip supply segmentation and control

Reverse biasing of substrate (PSUB)

Ancillary ASIC — Overview

Ancillary ASIC
High level block diagram



EIC-LAS LEC
(PWR, I/O)

Negative Bias Generator Specification				
Specification	Unit	Value	Comment	Status
Voltage Range	V	0 to -6	Relative to local ground	
Current Capacity	A	10^{-3}		
Voltage Ripple	mV	< 0.1		
Power	W	$< 10^{-2}$		
Supply Voltage	V	1.8		
Area	μm^2	4×10^5		

Shunt LDO Specification				
Specification	Unit	Value	Comment	Status
Voltage Output	V	1.1 - 2.0		
No. of Channels		5	Includes 1 to drive rest of ancillary chip	
Current Capacity per channel	A	0 - 1.5		
Voltage Ripple	mV			
Power	W			
Supply Voltage	A			
Area	μm^2			
Min-Max Input Current Slew Rate	A/s			
Min-Max Equivalent Load Resistance	ohm			
Over-Voltage Limit	V	2.5		
Max Current @ Over-Voltage Limit	A	2		

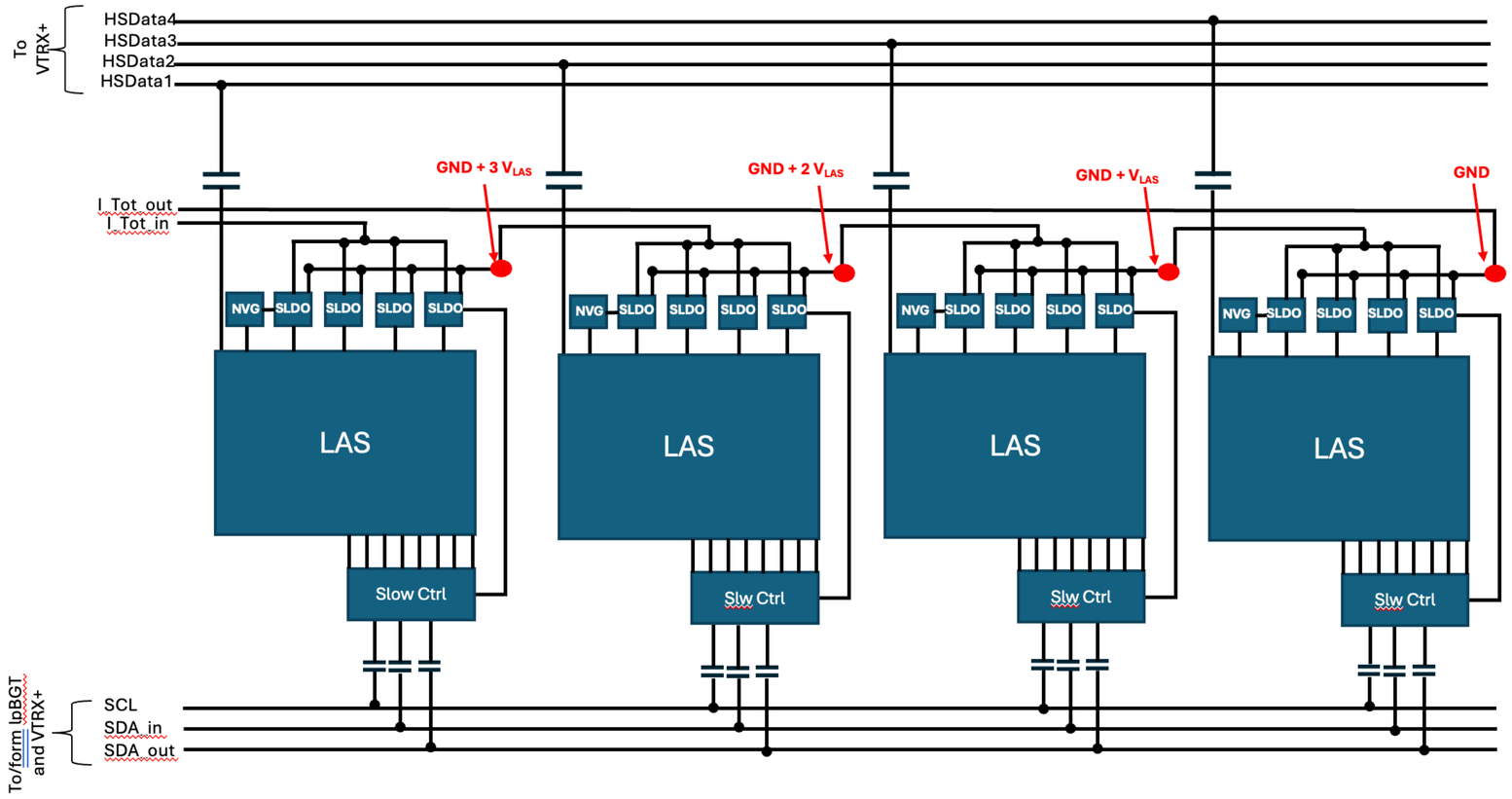
Slow Control Multiplexer Specification				
Specification	Unit	Value	Comment	Status
Input Signals	N/A	TBD		
Output Signals	N/A	PM Bus • PMWR • PMRD SC Bus • SCWR • SCRD GCLK GRST SYNC RESERVE	• CERN Low Power Signalling Compliant • Manchester Encoding • Exact details need to be confirmed with MOSAIX	
Voltage Ripple	mV			
Power	W			
Supply Voltage	A			
Area	μm^2			

- Estimated power consumption: up to 50% of EIC-LAS power
  - Dominated by SLDO regulators
    - Based on MOSAIX/EIC-LAS current needs as estimated at this time
  - Further optimisations considered for a more efficient current to voltage conversion

Outer Barrel and Disk Powering

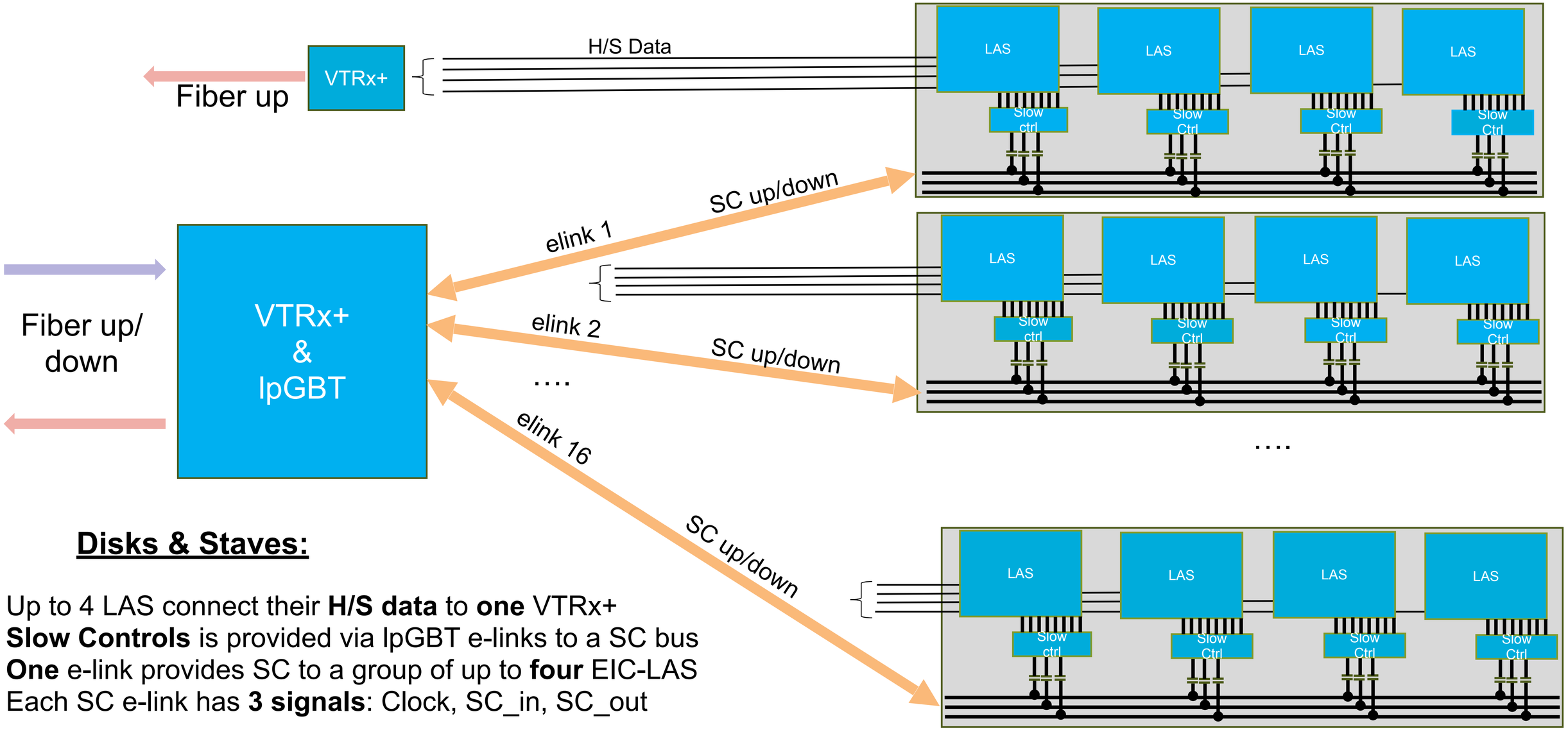
Tiling of sensors on staves and disks naturally leads to groupings of (up to) four EIC-LAS; this is key to service reduction with serial powering.

At a functional level:



A group of (up to) **four** EIC-LAS, each with **four** power domains and a bias voltage, is serially powered via **one** current loop in this scheme.

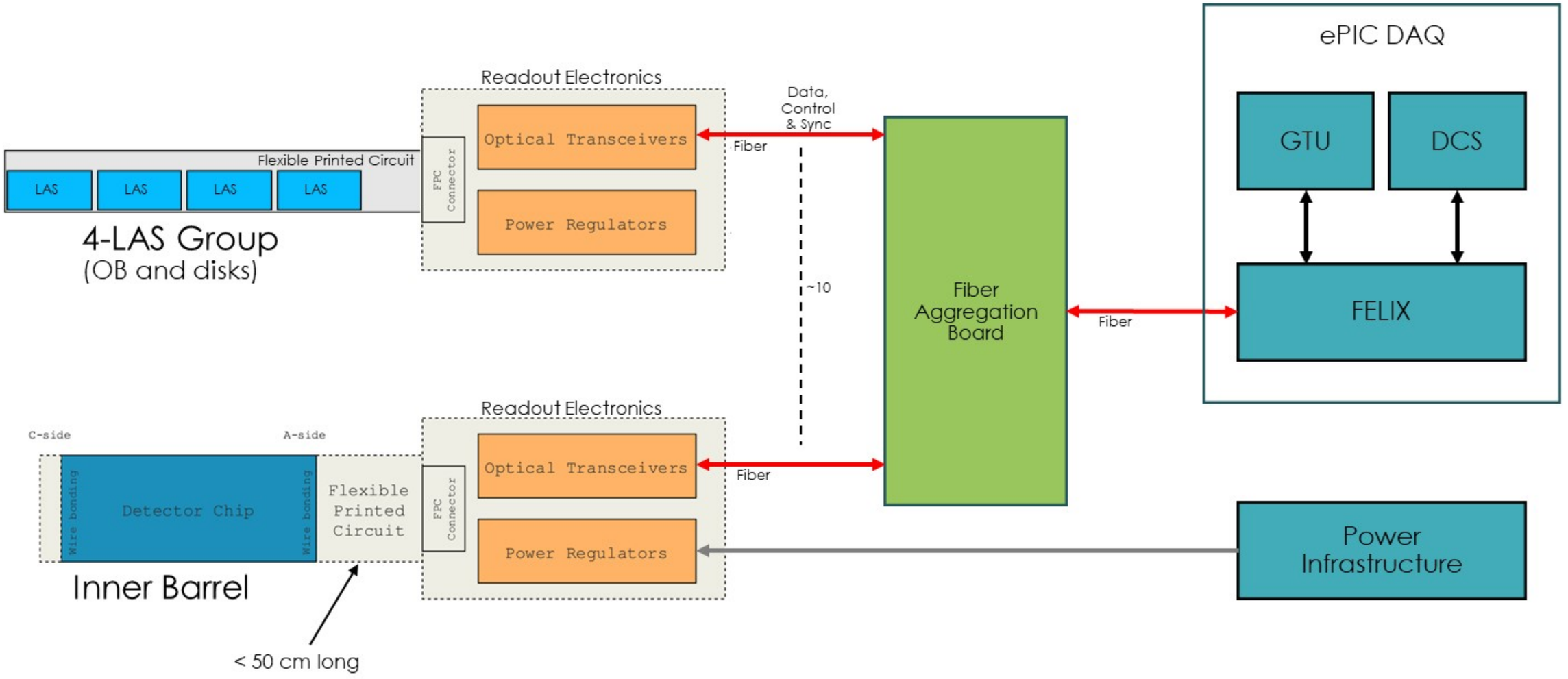
Outer Barrel and Disk Readout Electronics



Disks & Staves:

Up to 4 LAS connect their **H/S data** to **one** VTRx+
Slow Controls is provided via lpGBT e-links to a SC bus
One e-link provides SC to a group of up to **four** EIC-LAS
Each SC e-link has **3 signals**: Clock, SC_in, SC_out

SVT Electronics for Data & Control



(Note: Powering of readout electronics is estimated to be a sub-dominant contribution to overall SVT power dissipation.)

SVT Prototype Developments — Readout

- A full setup with lpGBT, VTRx+, and FPGA development boards (stand-ins for FELIX) exists at ORNL for evaluation of the various RDO components.
- Alternatives to CERN's lpGBT universe of components using commercial alternatives are being investigated.
- First results with these setups have been achieved:
  - Evaluation of the Samtec Optical FireFly as an alternative to VTRx+
  - Evaluation of the Microchip PolarFire FPGA as a radiation-tolerant FPGA replacement of the lpGBT
- Evaluation of Aggregator Board architectures with commercial FPGA development boards has been started at MIT.
- A test setup for the characterization of CERN Engineering Run chiplets to be used in the MOSAIX and LAS designs is under development.
- Investigations on Redundancy issues on the LAS design interfaces has started.
- Work is ongoing on defining the details of the LAS physical and protocol interfaces.

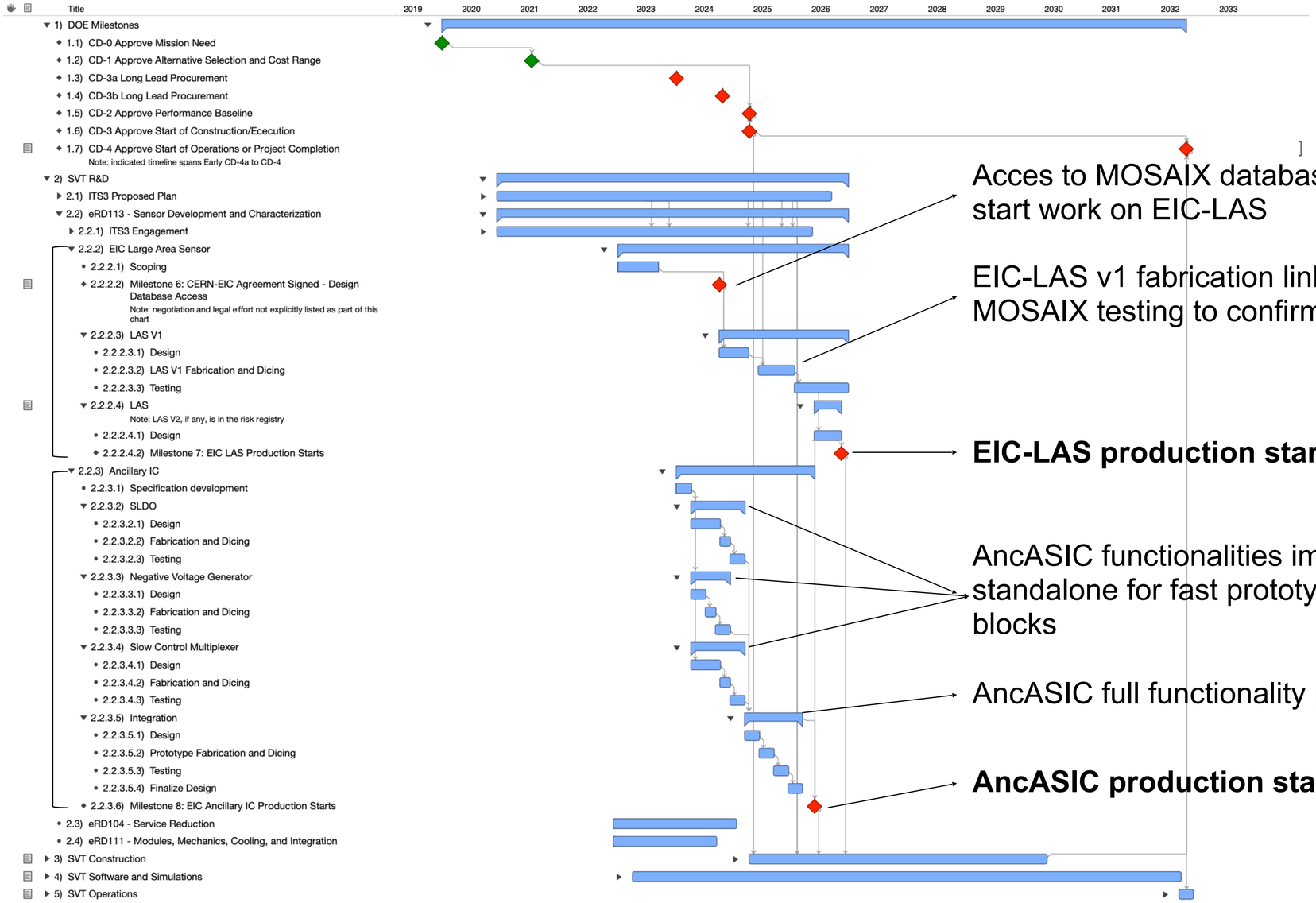
Schedule

IB wafer scale sensor

EIC-LAS

Ancillary ASIC

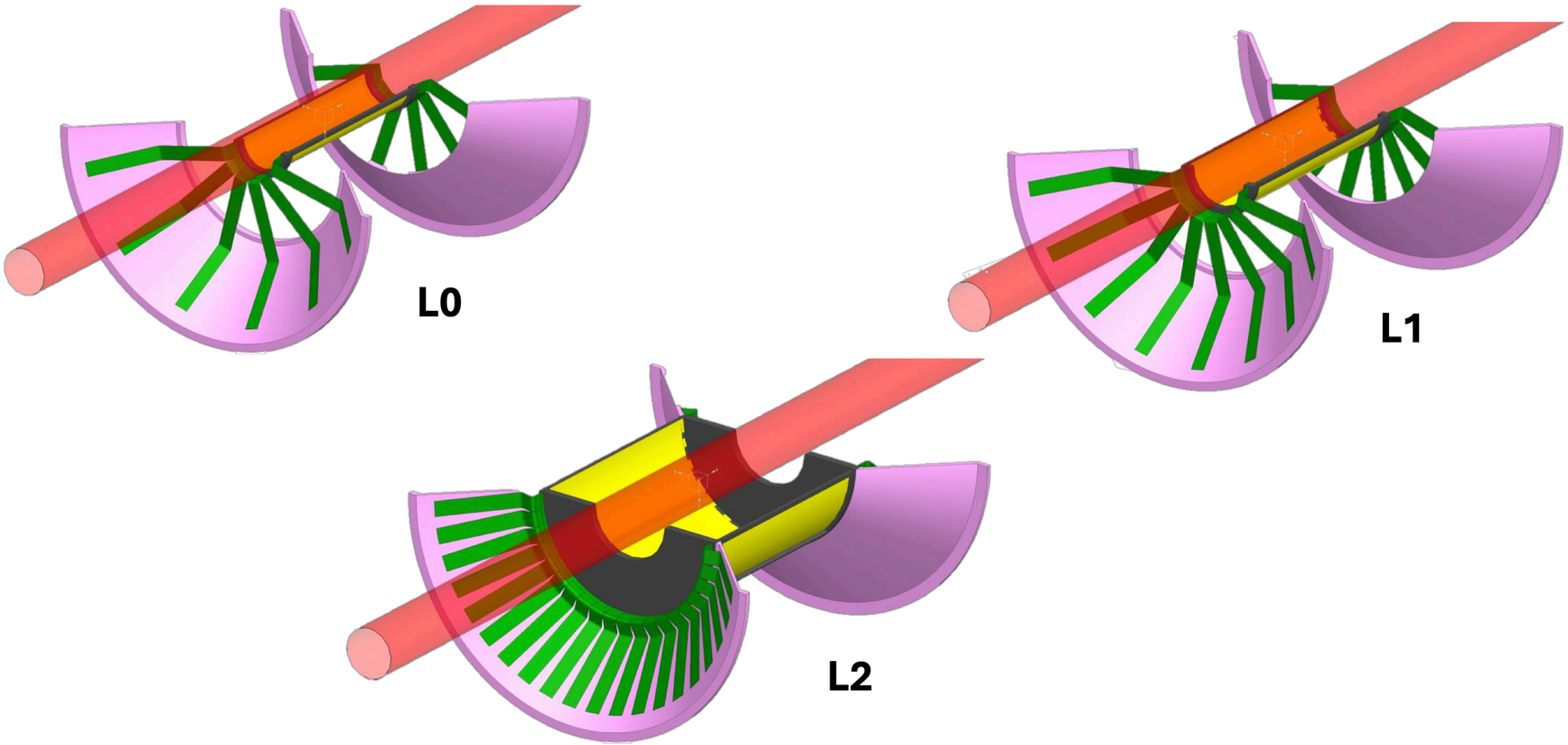
N.B.: calendar quarters



Modules, Mechanics, Cooling and Integration

- Remaining Project R&D is mostly focused on Cooling,
  - ITS3 effort has demonstrated air-cooling is feasible for their array of vertexing layers,
- Mechanics, Integration largely transitioned to PED,
- Ongoing effort for prototypes of IB layer, OB stave, disk quadrant this Summer aimed at demonstrating:
  - Assembly, tooling, and procedures,
  - Mechanical performance,
  - Thermal performance,
  - Feedback into design (and, in my personal opinion, key to finalizing technical requirements).

Mechanics — Inner Barrel



Initial stages of suitably adapting the ITS3 concept(s) to the ePIC SVT
Ongoing bending tests at INFN

Mechanics — Outer Barrel

The Outer Barrel will consist of staves,

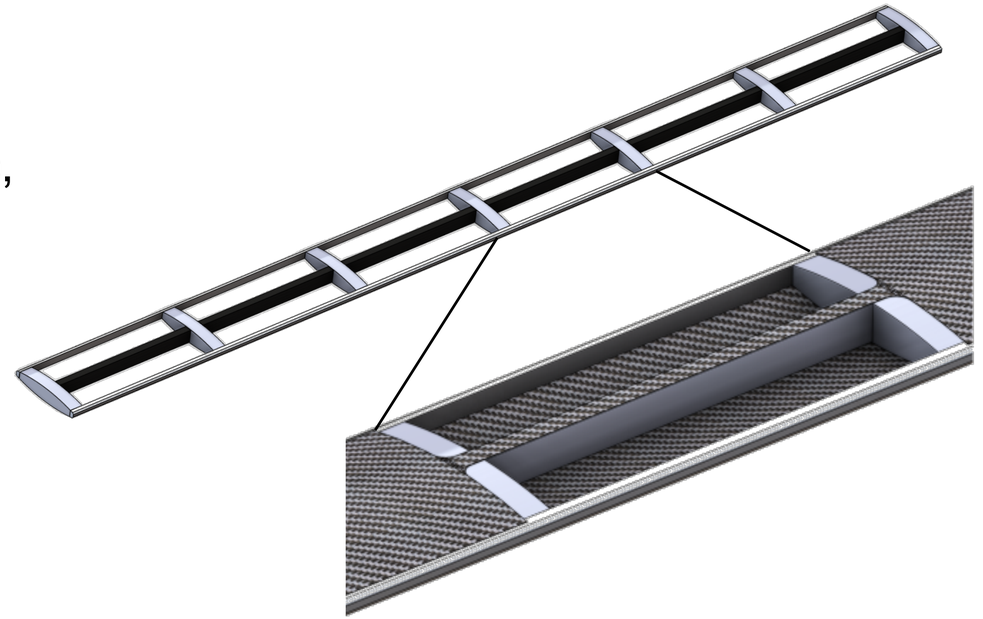
Stave will have twins of sensors on alternating sides (c.f. slide 16),

Core will consist of foam blocks, supporting all sensor edges,

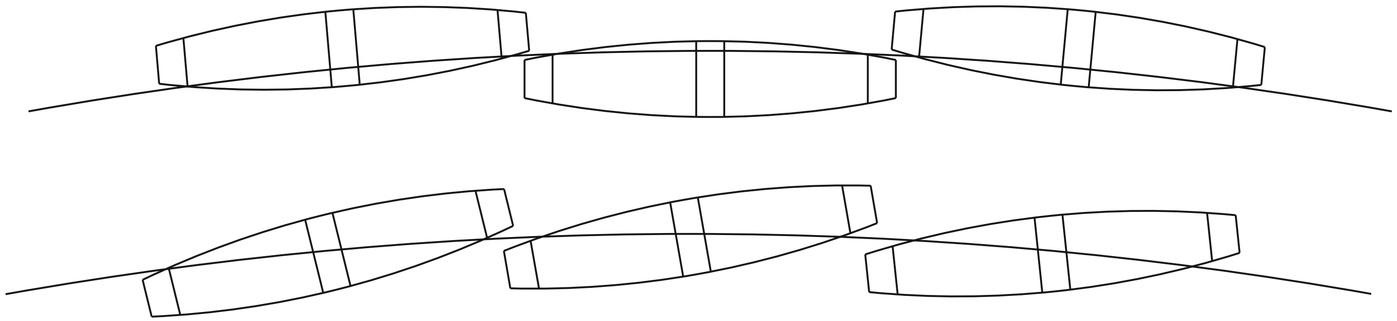
Surface between twins of sensors will be covered with a CF skin,

Thickness and possible curvature, as well as material and lay-up remain to be optimized,

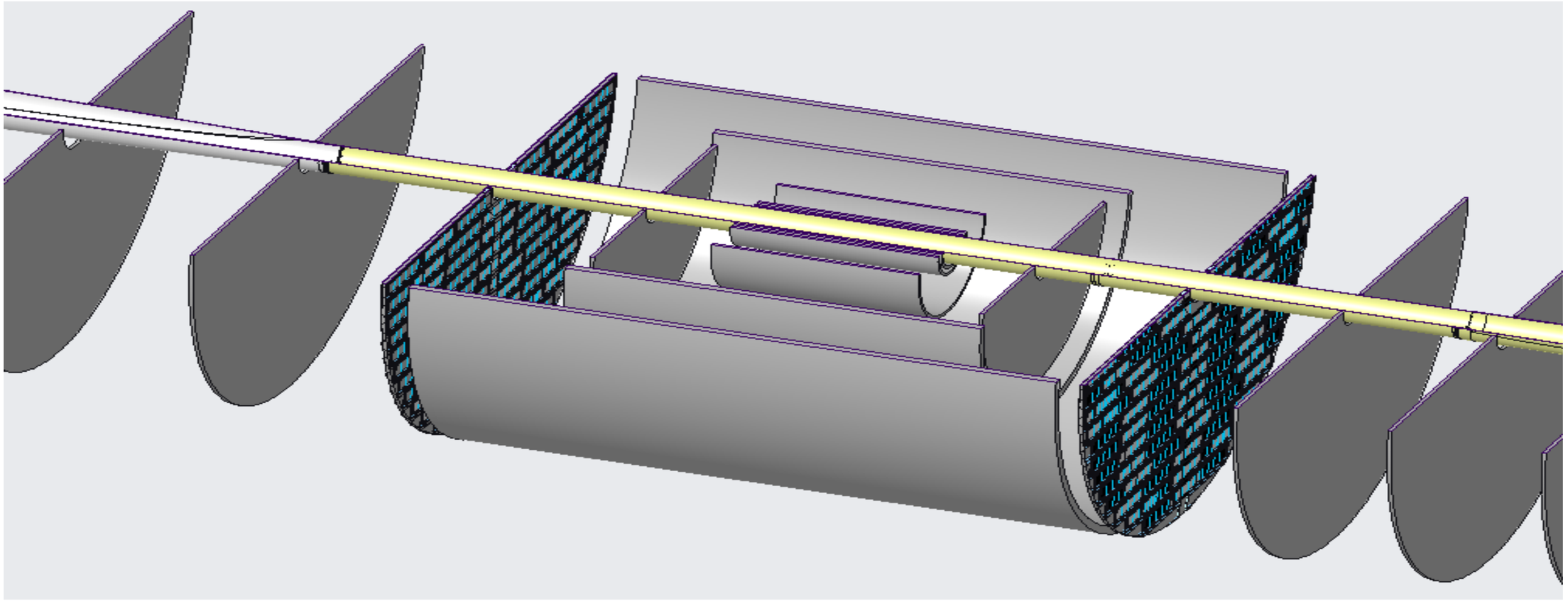
After co-cure or bonding the structure will be self-supporting.



Castellated as well as tilted arrangement of staves being considered for the OB.



Mechanics — Disks



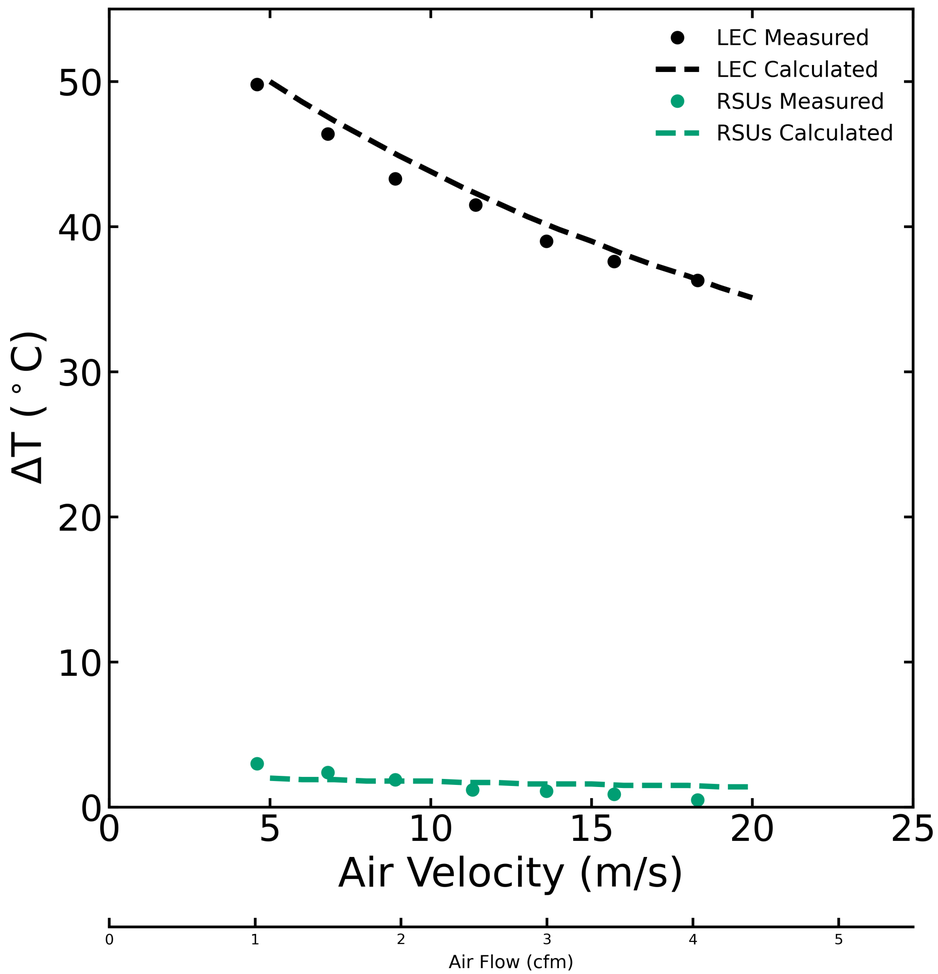
Note the crossing angle and acceptance cones of the beampipe. Top-down symmetry favors a horizontal segmentation of the disks.

SVT Cooling by the Numbers

- 4000 EIC-LAS sensors in the SVT
  - Power consumption based on best estimates: up to 1.6 W per EIC-LAS
  - Paired with an Ancillary IC for slow control, serial powering, bias: up to 50% of EIC-LAS
  - Readout with VTRx+ is estimated to form subleading contribution
- ***Baseline*** cooling design is ***air*** internal to the mechanical structure(s); liquid cooling in strategic places as necessary
- End goal is operation of SVT at/near ***room temperature***
- Measure thermal performance with $\Delta T = T_{sensor} - T_{inlet\ air}$
- "Reasonable" ΔT is one that achieves room temperature operation with sensible air inlet temperature
  - $\Delta T < 10°C$ is used often as a "standard", but is not a requirement

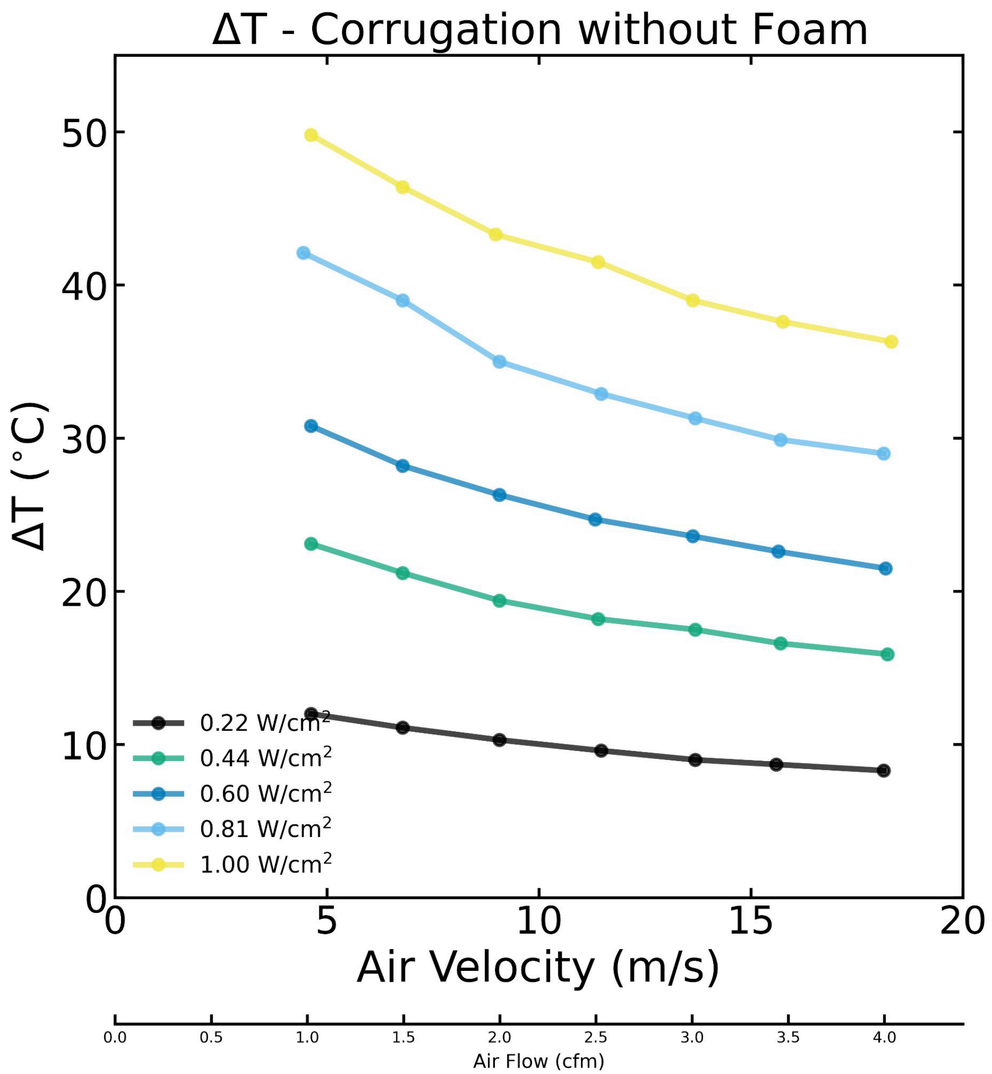
SVT Cooling — Disks

- ***Baseline*** disk design using corrugated carbon fiber
  - Provides a channel for forced air convection
- Air cooling sufficient for **RSUs**
- **LEC** trending in the right direction



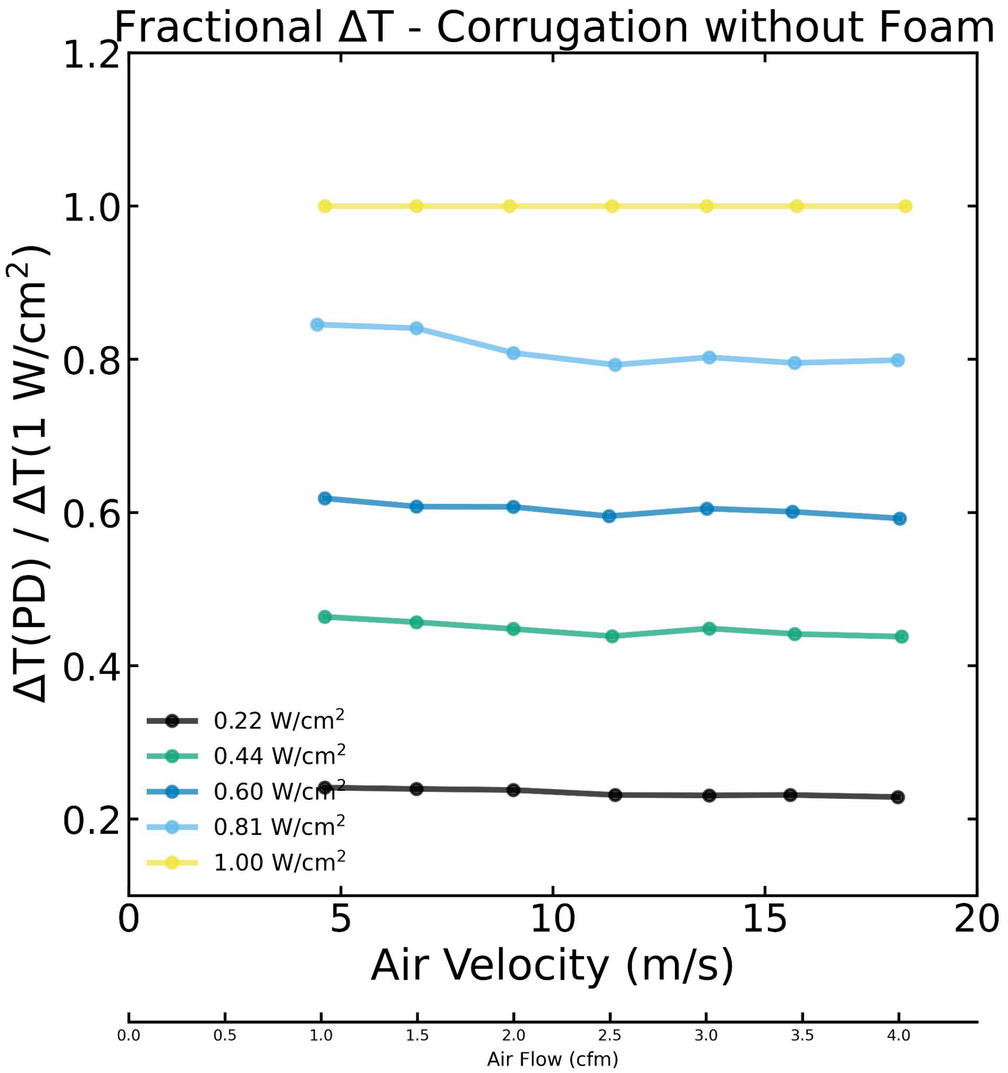
SVT Cooling — Disks

- Studied a range of LEC power densities
- **ΔT reasonable for power < 0.6 W/cm²**



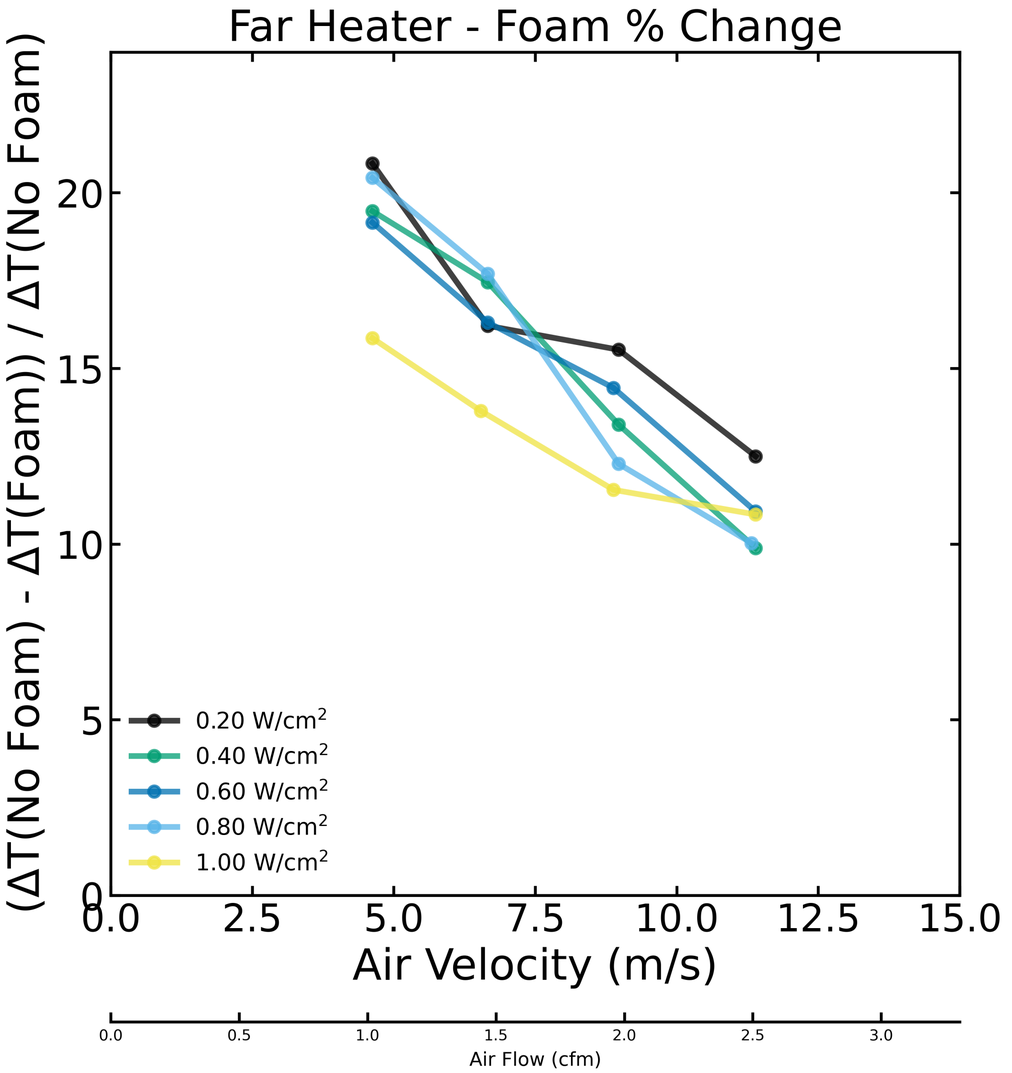
SVT Cooling — Disks

- Studied a range of LEC power densities
- ΔT reasonable for power < 0.6 W/cm²
- **ΔT scales with power density**



SVT Cooling — Disks

- Studied a range of LEC power densities
- ΔT reasonable for power < 0.6 W/cm^2
- ΔT scales with power density
- **Carbon foam** under LEC provides **10-20% reduction in ΔT**
  - Caveat: this is insulating foam. Will be measured with thermally conductive foam



SVT Cooling by the Numbers

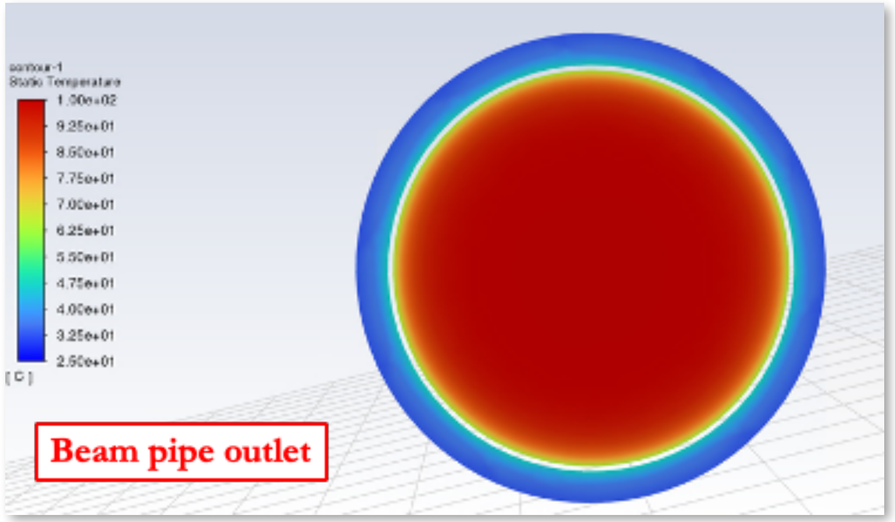
- ***Current*** baseline estimates
- IB: 50 cfm
- OB: max 400 cfm
- Discs: max 500 cfm

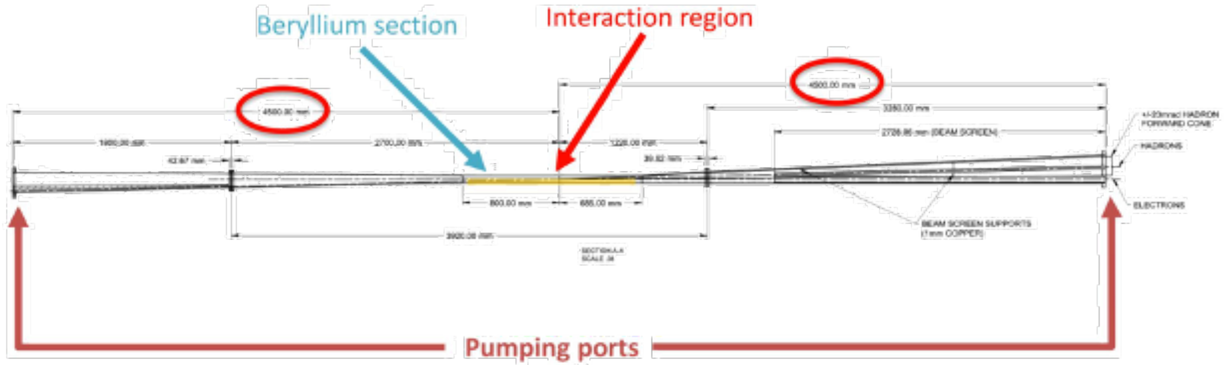
- Total system as we understand it is ~1000 cfm
  - Requires compressed air

- Optimization continues and we expect this number to go down

Beam-pipe bake-out

- Beam-pipe bake-out with SVT installed
- Aiming for no additions to cooling
  - No extra material (e.g. insulators) or changes (i.e. liquid instead of air)
- ANSYS studies at JLab and LBNL
  - Flow N2 in beam-pipe to get inner wall >100°C
  - Room temperature air between beam-pipe and silicon
  - Studies done with both full length of beam pipe and shortened section near SVT IB
- Bench setup at JLab verifies results
  - Covers 1 m of 3 m Be beam pipe section
- Path forward to cool detector





Beam-pipe bake-out

- Refine temperature envelopes for materials
  - ALPIDE (ITS2) can work reliably at 40°C
  - Estimates from climate chamber studies at LBNL up to 50°C show 65 nm DPTS performs reliably
- Initial thermoelastic study done by ALICE ITS3
  - 16 cycles between 10 – 48°C on ITS3 layer 2 (includes glue, foam, silicon) → no failures
- Similar thermoelastic study upcoming for ePIC SVT IB
  - Cycle test, longevity test, bake-it-til-you-break-it test
- Start of investigations of simplification — specifically, is air-flow between L0 and L1 sufficient and how does it reduce (unwanted) cooling of the beam-pipe during bake-out?

Outlook

- Lots of progress on many aspects of the ePIC SVT detector,
- Lots of work remains to ensure readiness for (pre-)TDR,
- CERN-EIC agreement is in an advanced stage; key to technology-access for EIC-LAS,
- EIC-LAS will be paired with an ancillary IC that is to provide serial powering, negative bias voltage, and multiplexed slow-control,
- Sensor + IC schedule compatible with project timelines; development would need to continue beyond the nominal CD-2/3 timeline of April 2025, sensor and IC production start(s) anticipated throughout 2026,
- SVT readout chain largely defined — FPC development ongoing and compatible with material requirements,
- Thermo-mechanical prototypes — IB, OB stave, disk quadrant — with thinned dummy silicon planned this year in preparation for TDR; ITS3 ER2 availability projected starting mid-c2025
- Air-cooling of the SVT appears feasible; essential for IB and highly desirable to minimize material in OB and disks,
- Continued resource needs for R&D and PED in upcoming years,
- Not explicitly discussed: global mechanics.