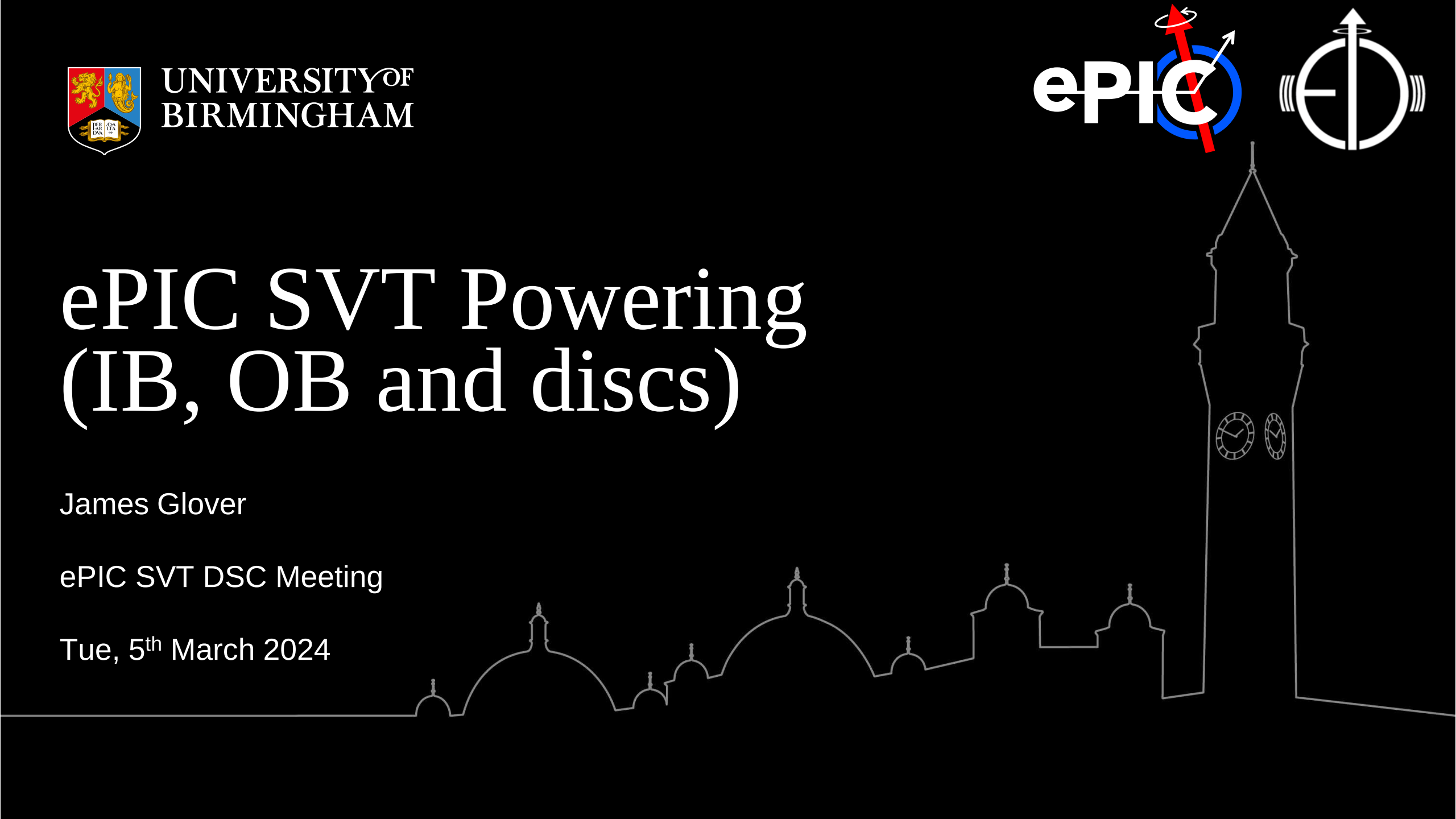


ePIC SVT Powering (IB, OB and discs)

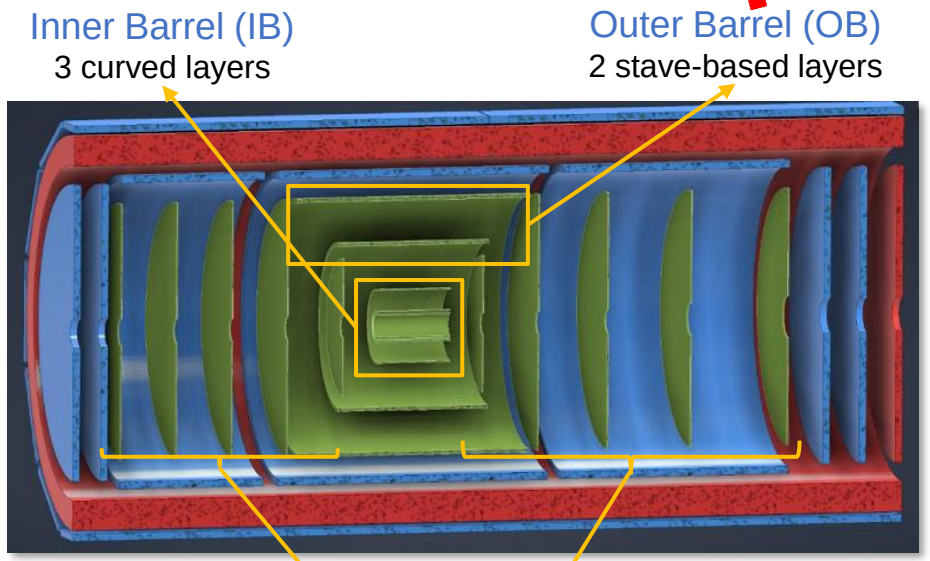
James Glover

ePIC SVT DSC Meeting

Tue, 5th March 2024

ePIC Silicon Vertex Tracker (SVT)

- SVT powering scheme split between IB and the rest of the SVT (OB,EE & HE).
- IB will be supplied with a voltage based, parallel powering scheme.
  - Like the ITS3 proposal, using the same wafer-scale sensors.
- OB, EE & HE will be supplied with a current based, serial powering scheme.
  - Using the EIC-LAS with an ancillary chip.



IB	–	Inner Barrel
OB	–	Outer Barrel
EE	–	Electron Endcap
HE	–	Hadron Endcap

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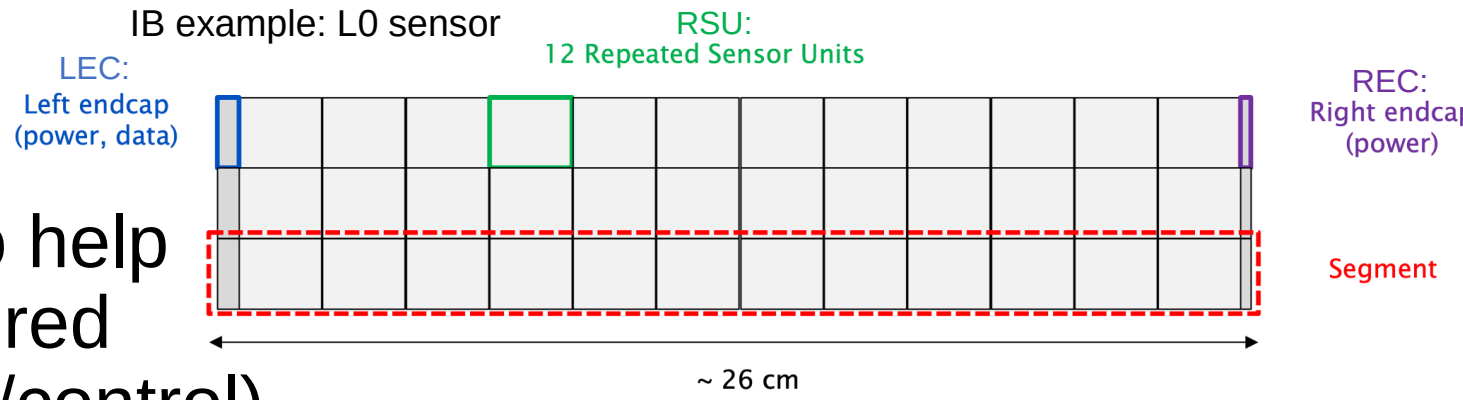
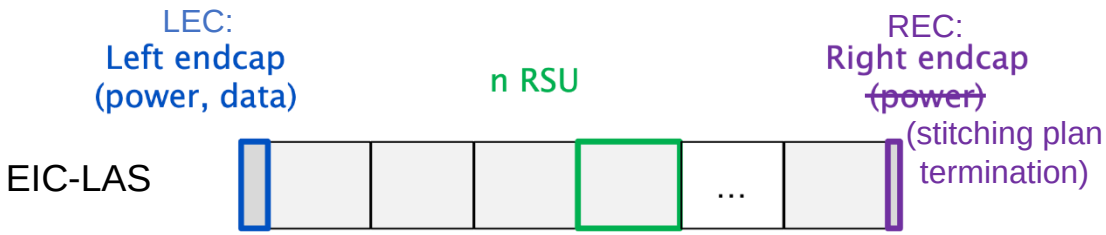
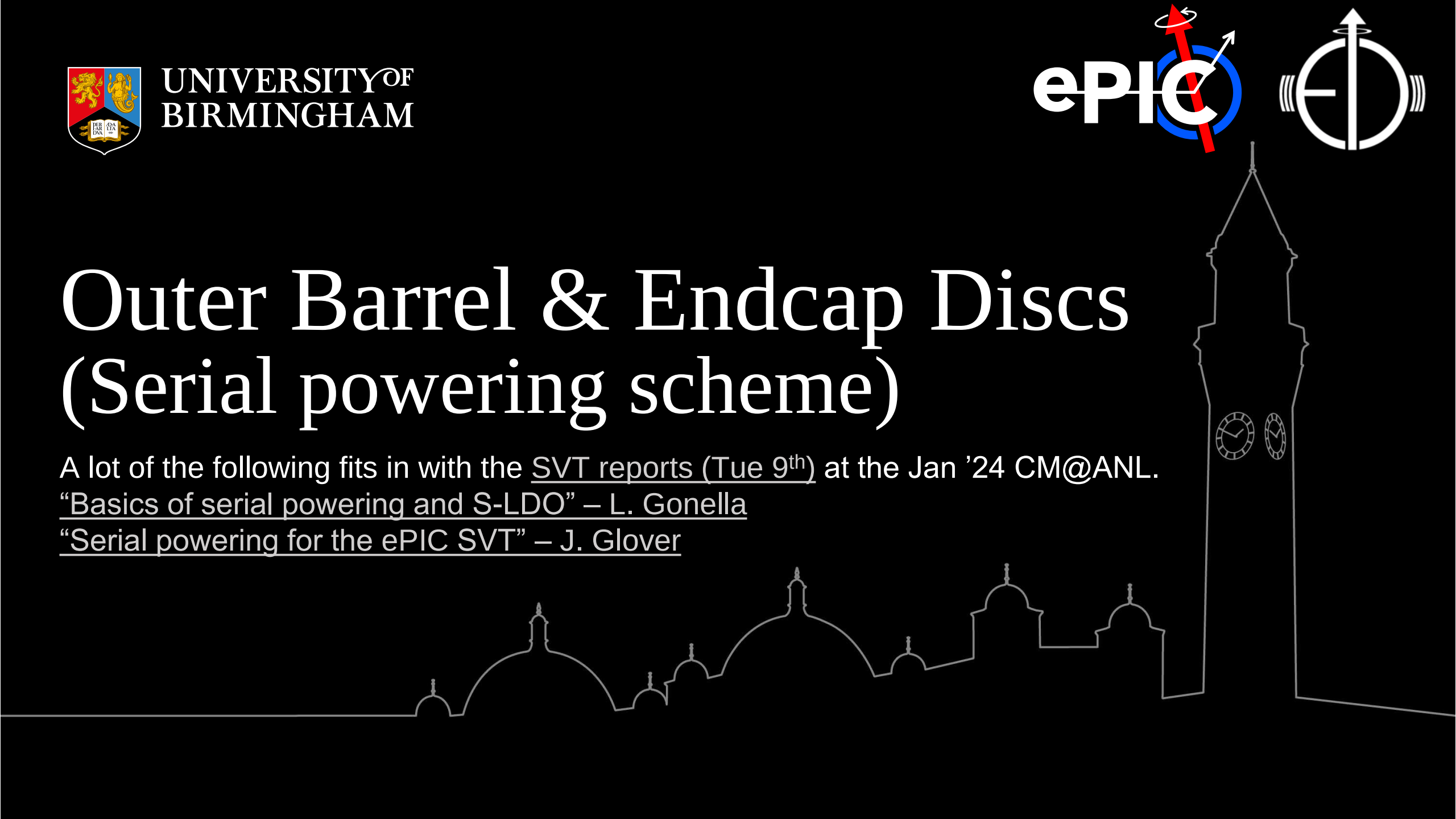
MAPS for ePIC

- Wafer-scale sensor used in IB.
- EIC-LAS (Large Area Sensor) is the EIC optimised sensor variant to help minimise the material required due to service (data/power/control) connections and improve yield for large area coverage.
  - For OB, EE, and HE of SVT.
  - Currently, options for EID-LAS with both 5 and 6 RSUs are being considered.



From:
https://wiki.bnl.gov/EPIC/index.php?title=Si_Vertex_Tracker





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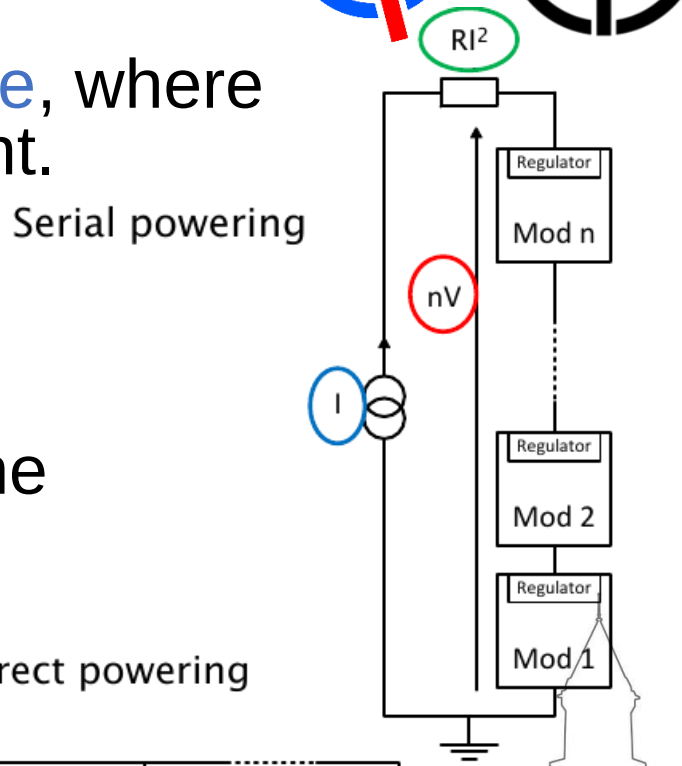
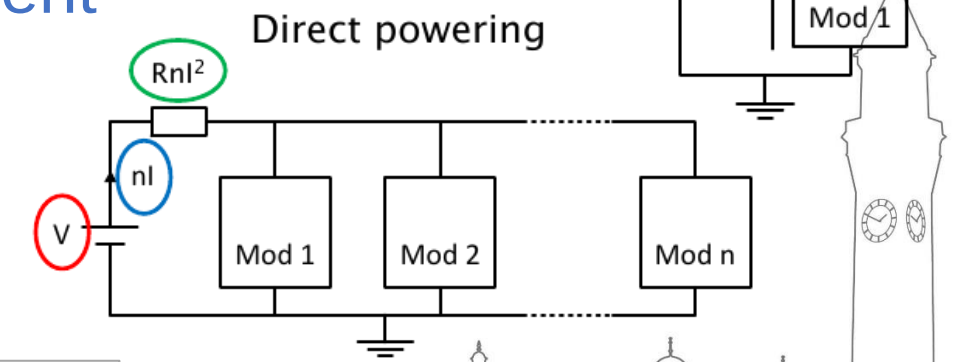
Outer Barrel & Endcap Discs (Serial powering scheme)

A lot of the following fits in with the SVT reports (Tue 9th) at the Jan ’24 CM@ANL.
“Basics of serial powering and S-LDO” – L. Gonella
“Serial powering for the ePIC SVT” – J. Glover

Serial powering basics

- Serial powering is a current based powering scheme, where modules are powered in series by a constant current.
- The current to voltage conversion is done by regulators close to/on module.
- In a serial powering chain made of n modules, the transmitted current is only the current needed by one module, I.
- For n modules powered in series, the current is reduced of a factor n with respect to a direct powering scheme → Higher power efficiency and reduced cable volume.
  - Cable cross-section and the power losses on the cables scale by the same factor.

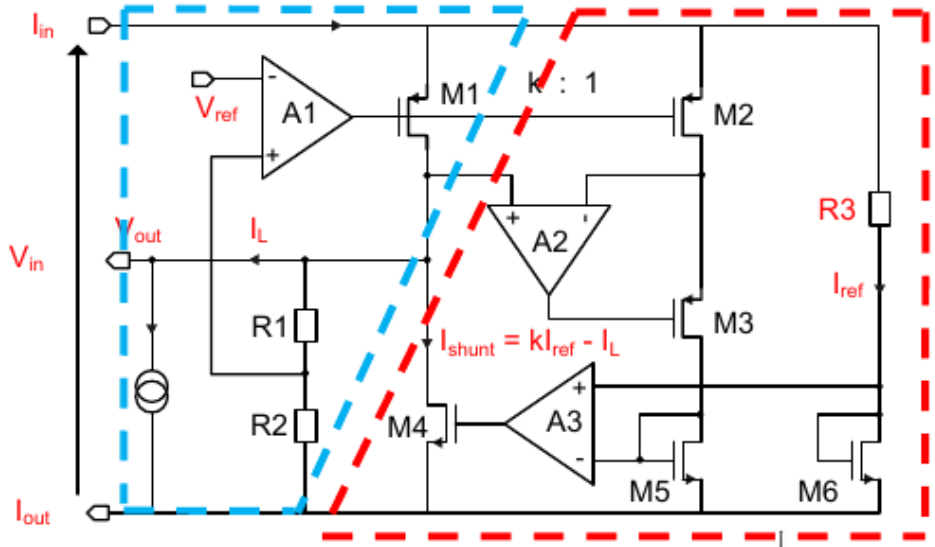




From: Jan '24 CM@ANL – L. Gonella, "Basics of serial powering and S-LDO", https://indico.bnl.gov/event/20473/contributions/84989/

Shunt-LDO regulator

- For this powering scheme, on-chip regulators are needed that can:
  - Operate in parallel
  - Generate different output voltages out of the current supply
  - Shunt additional current in case of device failure.
- The Shunt-LDO regulator was designed to match these requirements.
  - First prototype version in the ATLAS pixel FEI4 chip (180 nm process).
  - Full SP version in the RD53 chip (65 nm process).
- It combines two regulation loops.
  - Shunt regulation circuitry → regulates the current to the chip.
  - LDO (Low Drop Out) regulation loop → generates the voltage for the chip.



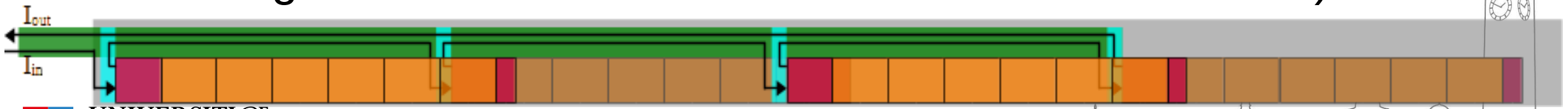
From: Jan '24 CM@ANL – L. Gonella, "Basics of serial powering and S-LDO", https://indico.bnl.gov/event/20473/contributions/84989/

FPC considerations

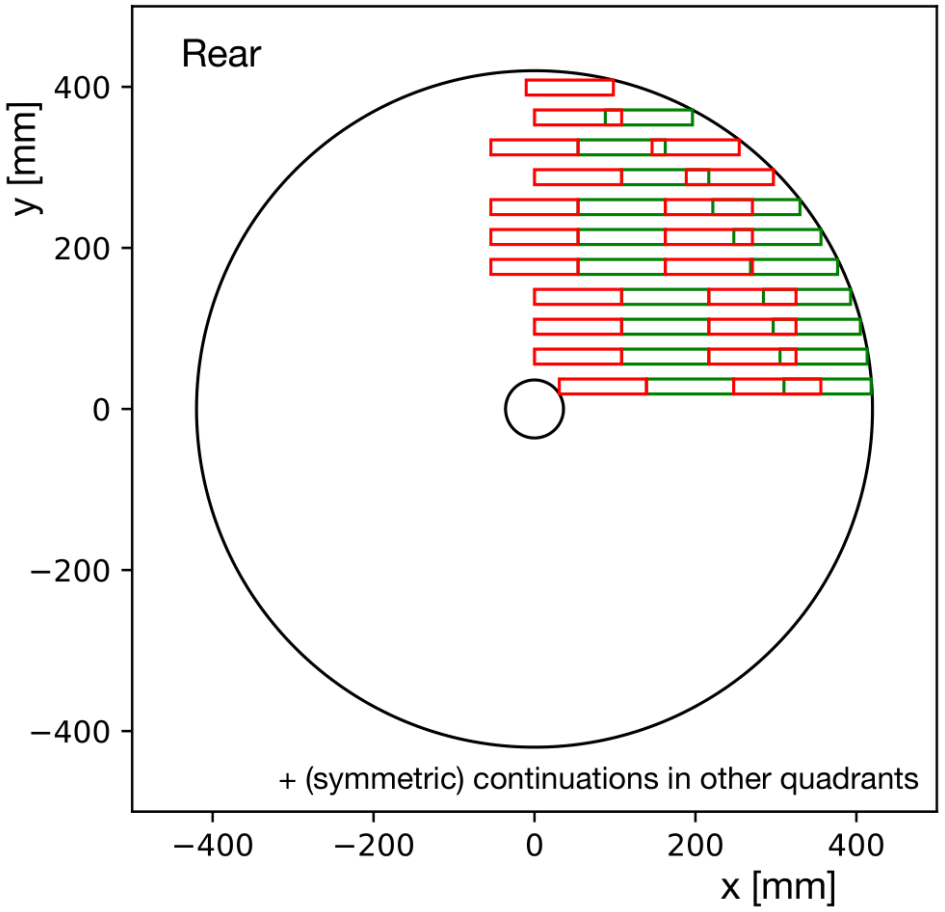
The flexible printer circuit (FPC) will be the interconnect between clusters of EIC-LAS. This needs:

- To enable the readout of data from many EIC-LAS to 1 VTRx+.
- Host the current to voltage regulation (for each EIC-LAS) and interconnections within a SP chain.
- Clusters of 4 EIC-LAS per SP chain work well with VTRx+ readout.
  (each EIC-LAS to have 1 multiplexed data link, for all RSUs, with 4 links available on a single VTRx+)

FPC designs are preferring clusters 1 EIC-LAS wide (even if interfacing sensors on different sides of the same structure).



Endcap Discs



Need to consider options when shorter structures are required.

- Larger y coordinates in the plot (←).
- Clusters of < 4 EIC-LAS would be inefficient (less of a benefit from SP).
- Linking neighbouring structures together would increase complexity of the FPC.
  - Multiple FPC designs.
  - Some designs may only be needed in small numbers.

ITS3's power domains

Table 3.11: Power domains of one sensor segment. The substrate bias is common to all the segments composing a sensor. The nominal operating voltages are referred to the potential of the GAVSS input net. The input currents are obtained assuming the maximum estimated power consumption of the LEC and RSU circuits at 25 °C.

Supply purpose	Nets	Voltage [V]	Current [mA]	Pads on LEC	Pads on REC
Services	SDVDD-SDVSS	1.2 to 1.32	227	Yes	Yes
Global analogue	GAVDD-GAVSS	1.2 to 1.32	540	Yes	Yes
Global digital	GDVDD-GDVSS	1.2 to 1.32	1369	Yes	Yes
Serialisers	TXVDD-TXVSS	1.8	200	Yes	No
Substrate bias	PSUB	−1.2 to 0			

From ITS3 TDR (Section 3.4.5):
https://indico.cern.ch/event/1372078/attachments/2790270/4865816/20240129ITS3_TDR_V3LHCC.pdf

- 3 domains all around +1.2 V.
  - Services
  - Global analogue
  - Global digital
- 1 Serialisers domain at +1.8 V.
- 1 Substrate bias domain at -1.2 V.

Ancillary ASIC

- Power domains to be achieved using S-LDOs and negative voltage generator (NVG),these will be part of an ancillary ASIC (along with multiplexing of slow controls).
- Chip designers are working on power consumption estimates.
  - This will be dominated by the S-LDOs
- Some aspects will be introduced here.
- A talk by the chip designers will be at a future (SVT) meeting when power figures are finalised.

The 1.8 V problem

To keep the 1.8 V Serialisers domain of the wafer-scale sensor:

- All Shunt-LDOs (S-LDOs) need to be in parallel, and if we run them at 1.8V, the 1.2V supplies will waste considerable power.

Chip design (MOSAIX) currently has on-chip LDOs for the serialisers (while each serialiser runs at 1.2 V).

- We could remove this LDO and rely on the S-LDO to generate the 1.2V for the serialisers.
- We then have 4 domains of 1.2 – 1.32 V.

From recent chip designers meeting (closed session).

The 1.32 V problem

The Services domain needs to be at a higher voltage than the other domains (Global analogue and Global digital):

- This is because Services drives the tile power switches, and they want to guarantee the PMOS devices in these switches can always be fully turned off.
- Therefore, even though the table quotes GA, GD and Services at 1.2 – 1.32 V, GA and GD are nominally 1.2V, and Services is nominally 1.32V.
- This has less impact on power than the 1.8V issue, but will still lead to increased power.

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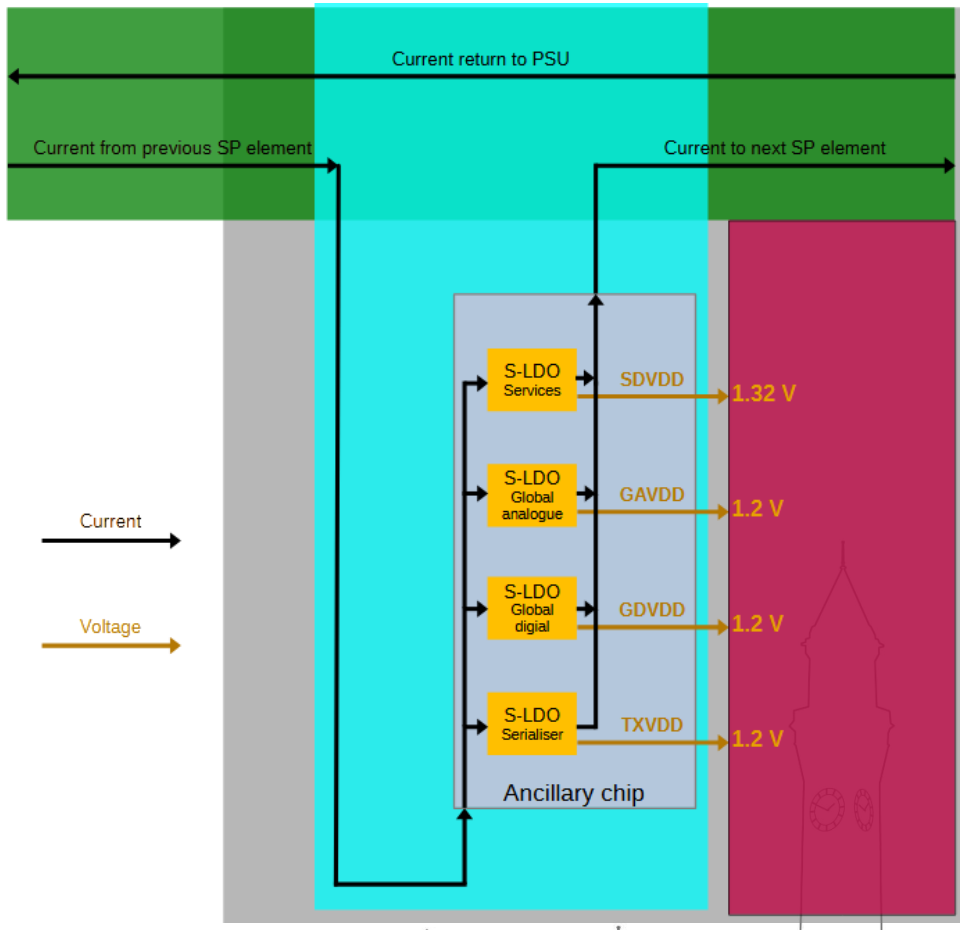
From recent chip designers meeting (closed session).

1 S-LDO per (+ve) domain

- 4 S-LDOs would be needed (in parallel).
  - Services (1.32 V).
  - Global analogue (1.2 V).
  - Global digital (1.2 V).
  - Serialisers (1.2 V).
- What about redundancy?
  - Per EIC-LAS and per SP chain.



Redundancy options

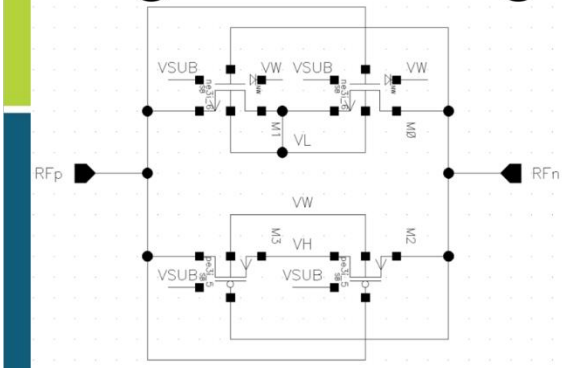
1. 1 S-LDO failure, kills 1 EIC-LAS, but keeps SP chain.
   - 4 S-LDOs per EIC-LAS.
   - If any 1 fails, the EIC-LAS is lost.
   - Up to 2 (on the same EIC-LAS) can fail before the SP chain is lost*.
2. Redundancy for each S-LDO (2 per domain).
   - 8 S-LDOs per EIC-LAS (more material).
   - Master/slave relationship (slave only supplies domain if master has failed).
   - Requires additional circuitry (and material), on top of the additional S-LDO.
   - Any (single) S-LDO failure does not affect the detector performance.
   - 2 S-LDOs (for the same domain) would have to fail before losing an EIC-LAS.
   - Up to 2 domains (on the same EIC-LAS) can fail before the SP chain is lost.

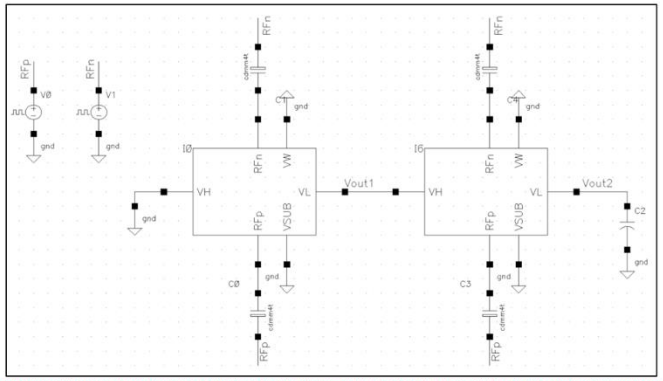
*Assuming 2 S-LDOs remain, each shunting $> \frac{1}{2} I_{EIC\text{-}LAS}$.

Substrate bias domain

From: 9th Jan ’24, ePIC CM@ANL – G. Deptuch, “EIC-LAS ancillary / support IC”, https://indico.bnl.gov/event/20473/contributions/84985/attachments/51831/88643/ePIC_SVT_MAPS_design_org.pptx

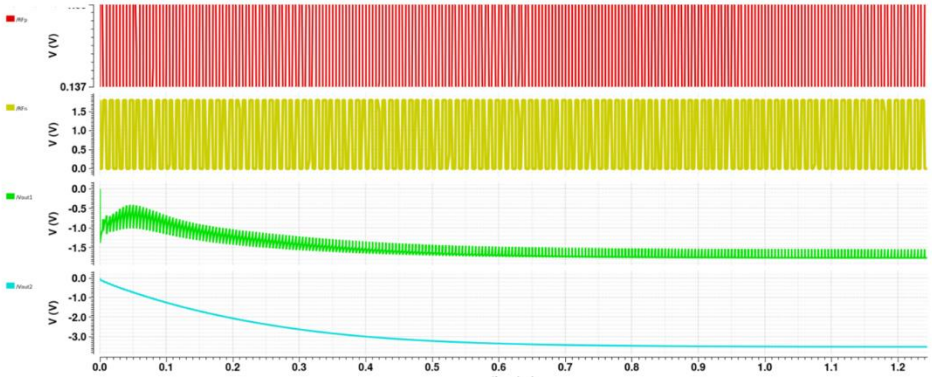
Negative Voltage Generator





Preliminary:

Vout2 = -3.6 V



- The S-LDO configurations only cover the positive voltage power domains.
- A -1.2 V domain is needed for the substrate of the chip.
- Can not be supplied in a parallel powering scheme.
  - Each EIC-LAS in the SP chain will have a difference ground reference.
  - The -1.2 V must be referenced to the specific EIC-LAS’s ground.

4

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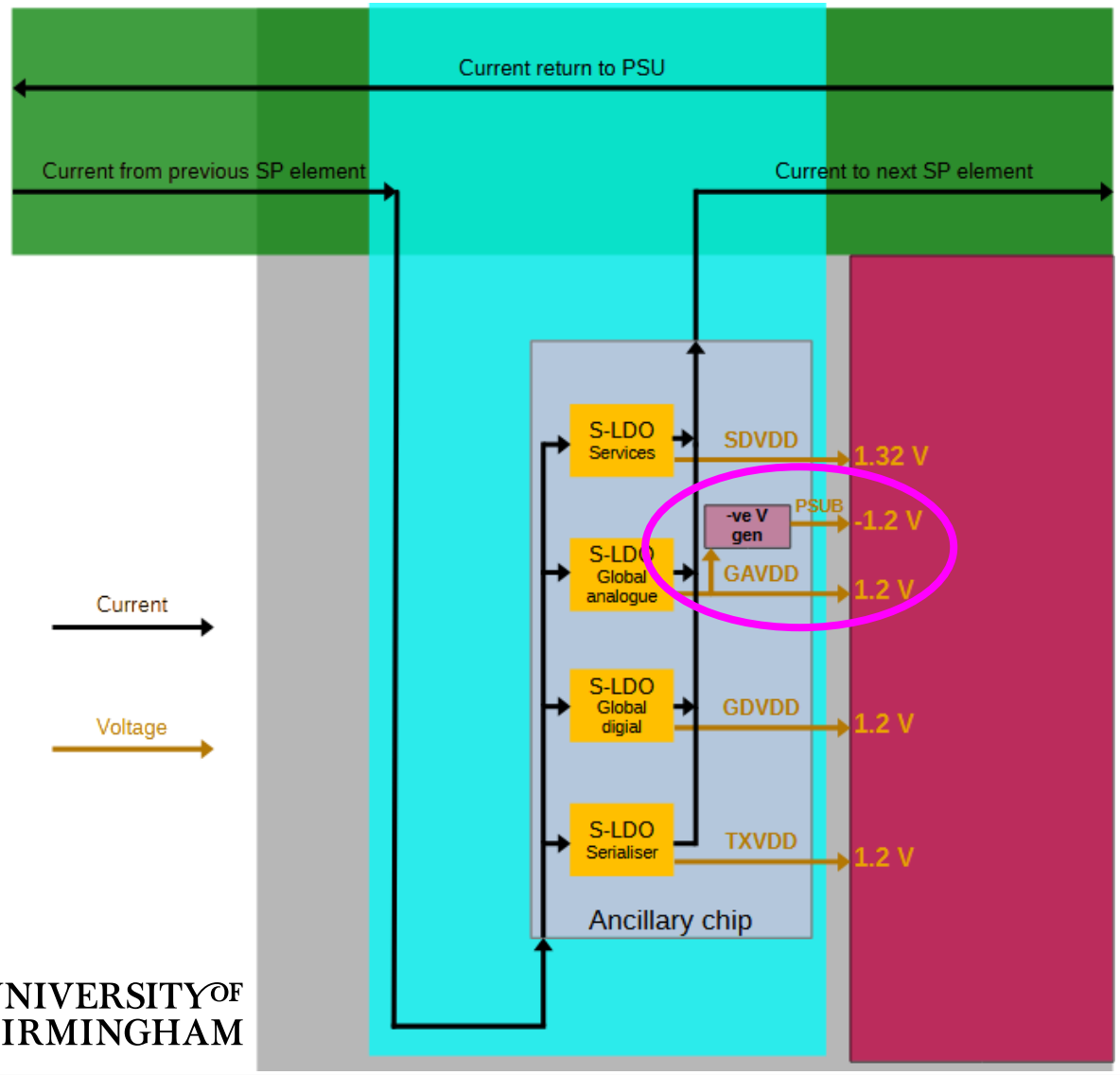
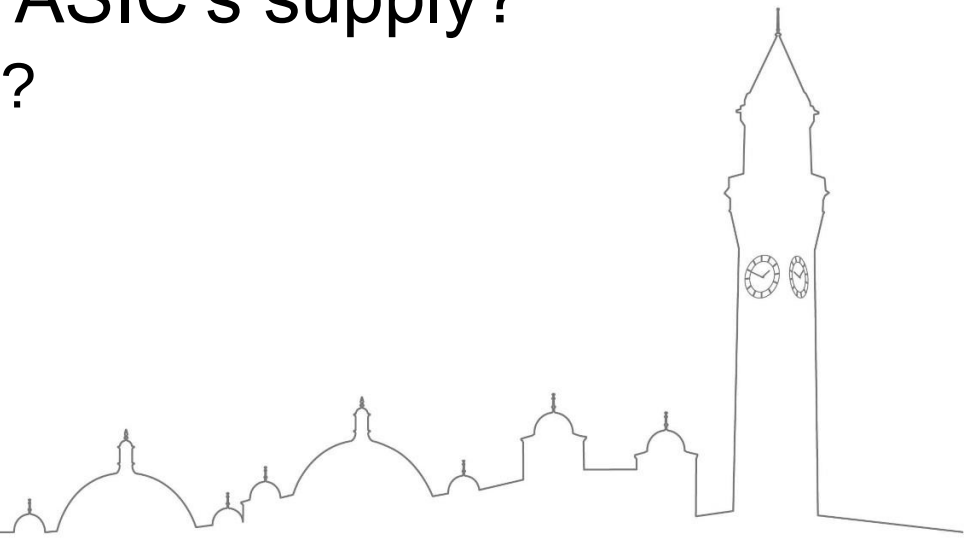
S-LDO config per EIC-LAS



- Basic configuration overview (no redundancy shown).
- Negative voltage generator shown on Global analogue for ease.
  - Could be run from another domain's S-LDO.
  - Or a dedicated S-LDO.

Powering the ancillary ASIC

- The S-LDOs will be powered by the current supply.
- Rest of the ASIC needs power from somewhere else.
  - Most likely needing 1.8 V.
- Direct powering to ancillary ASIC?
  - Two lines = 1 PSU channel per ancillary ASIC.
- Do we also want voltage regulation for the ASIC's supply?
  - A separate 1.8V S-LDO running in LDO-mode?



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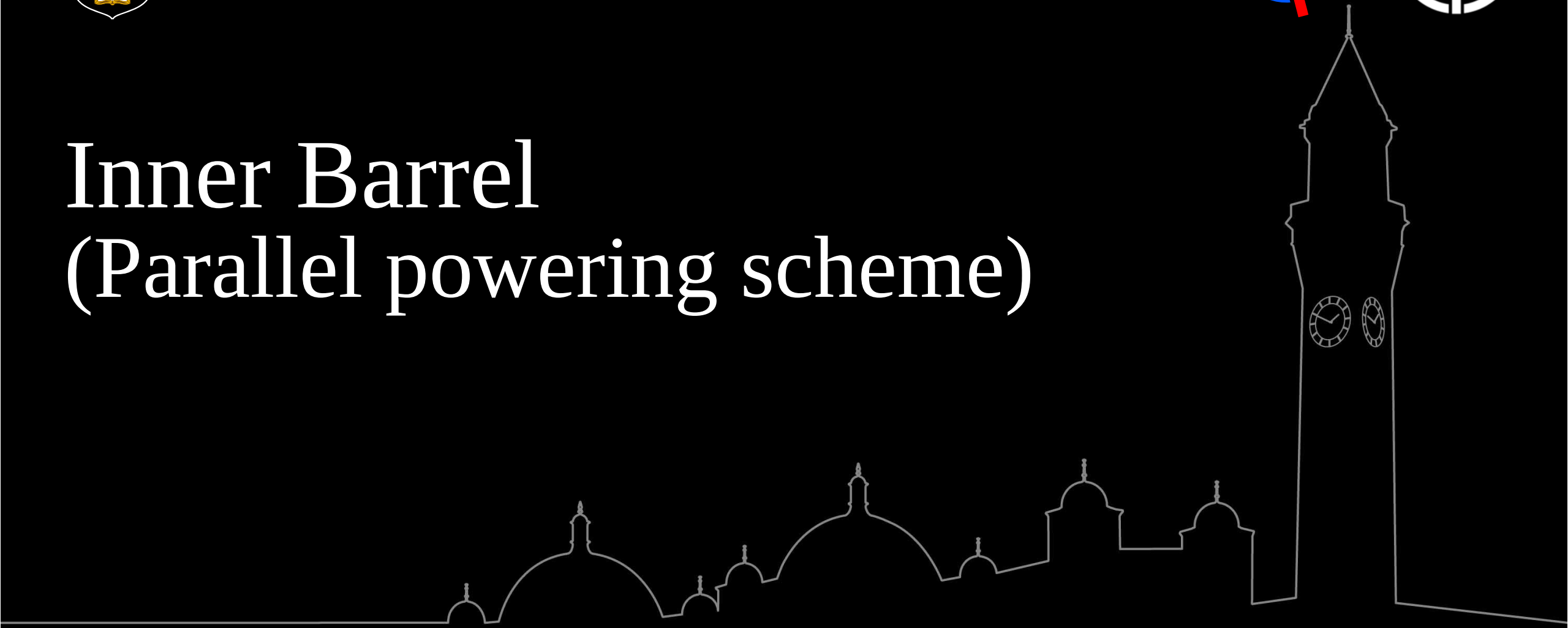
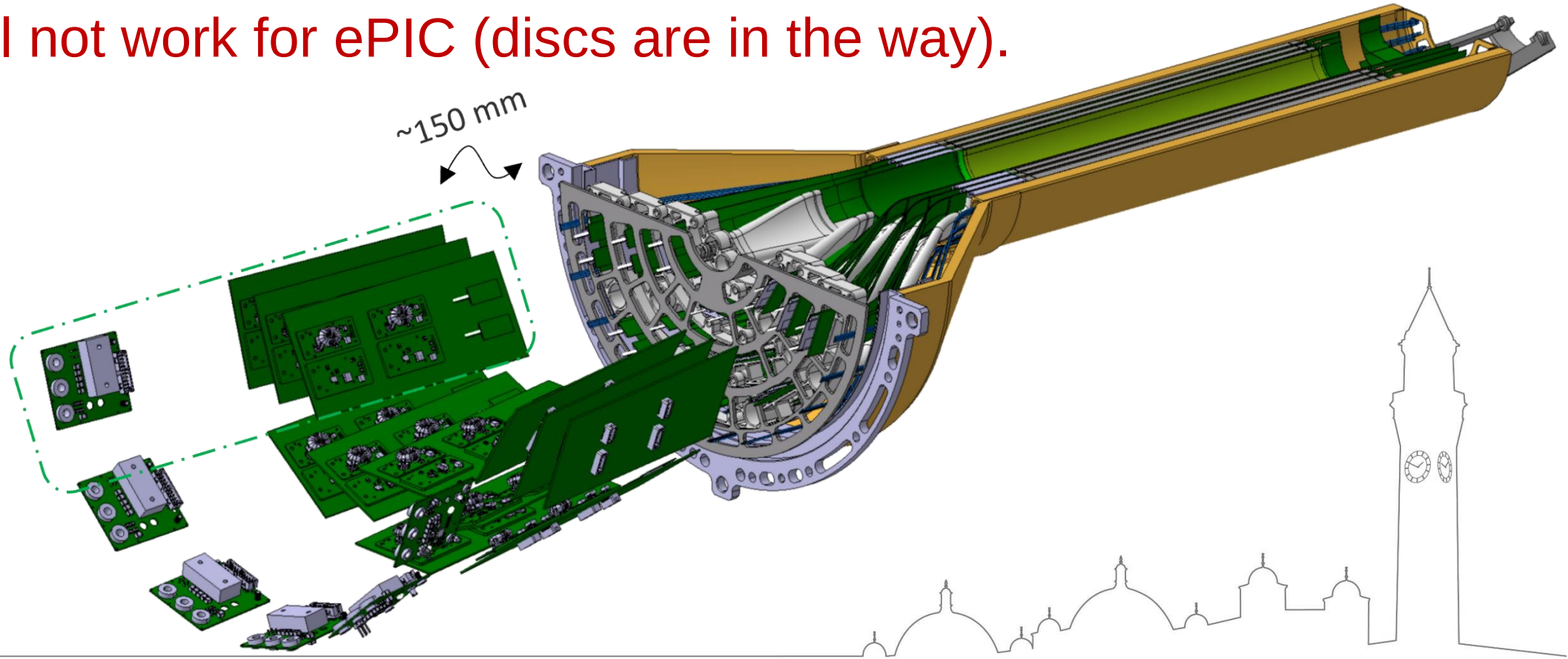
Inner Barrel
(Parallel powering scheme)



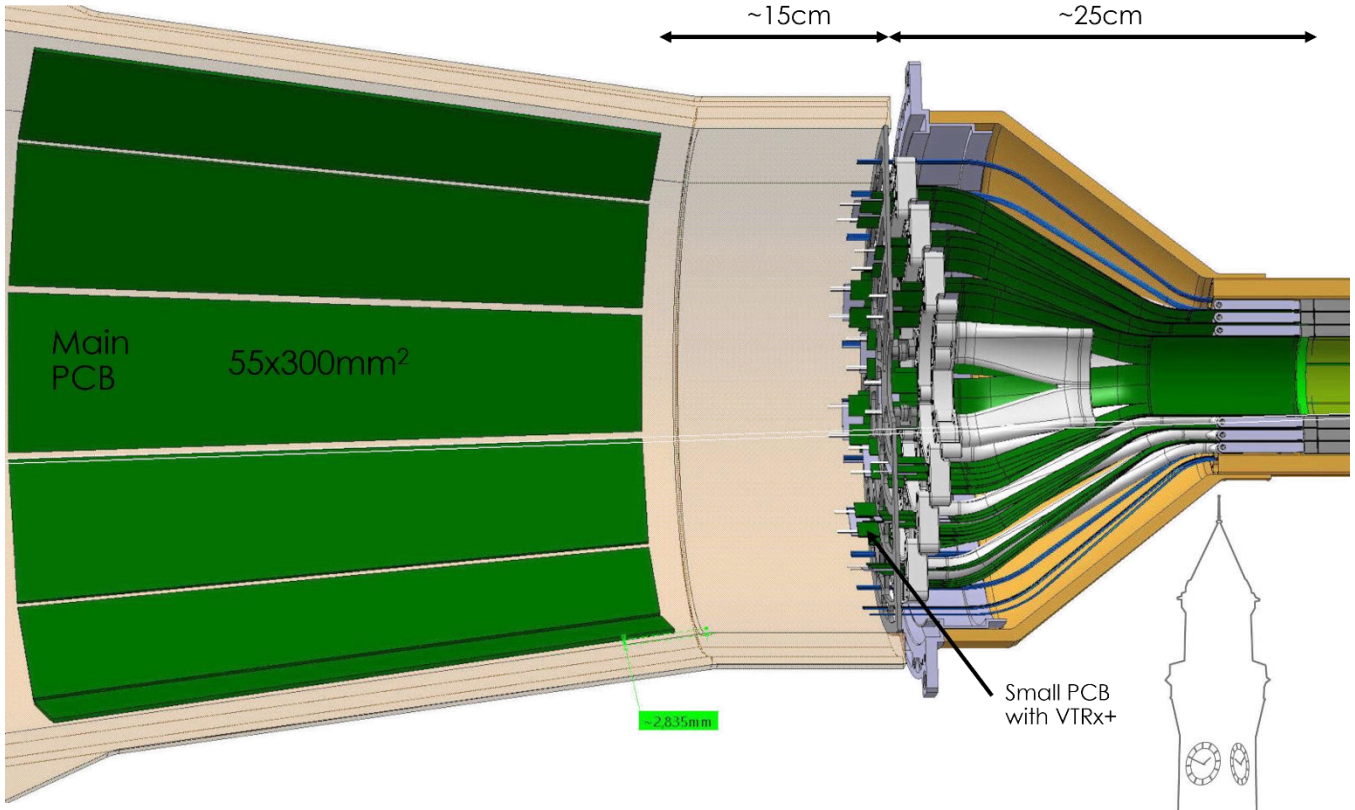
ALICE ITS3's plan

- ITS3's plan is to have a support cone and all their services running (roughly) parallel to the beam pipe.
- This will not work for ePIC (discs are in the way).



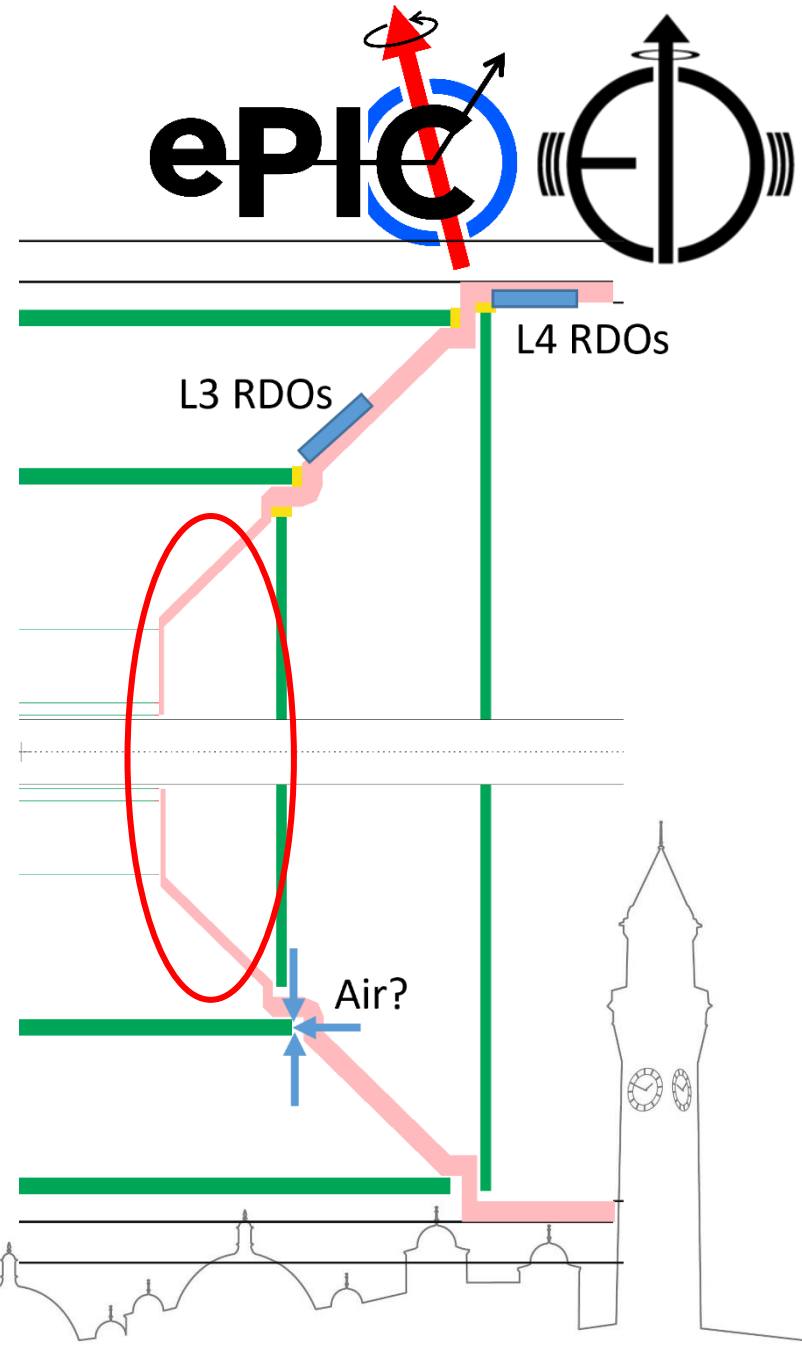
ITS3 PCBs

- ITS3 have a (relatively) long FPCs between the sensor and the readout VTRx+ (~25 cm).
  - This is to be as short as possible for ePIC.
- There is then a (relatively) short distance (~15 cm) until the main PCB (which is very large, 5.5 × 30 cm^2).



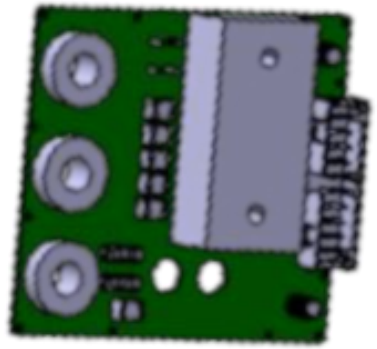
ePIC envelop

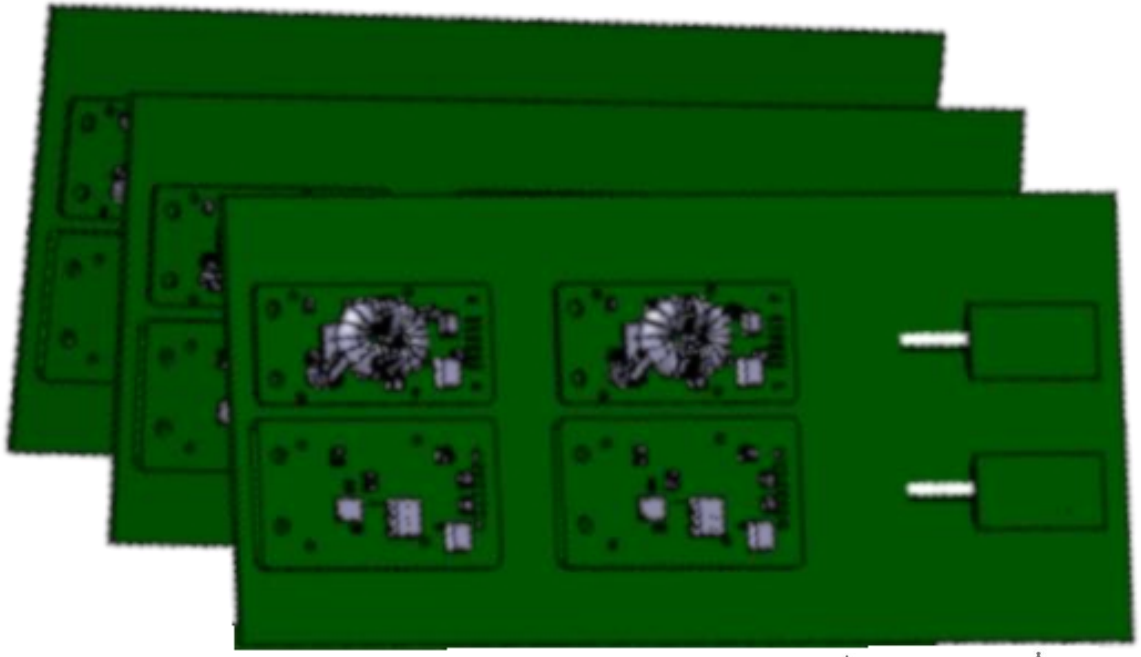
- ePIC's services envelop is too tight to fit an equivalent to this main PCB as close to the sensors.
- Does this main PCB really need to be as big as ITS3 have estimated (5.5 × 30 cm^2)?



Main PCB contents

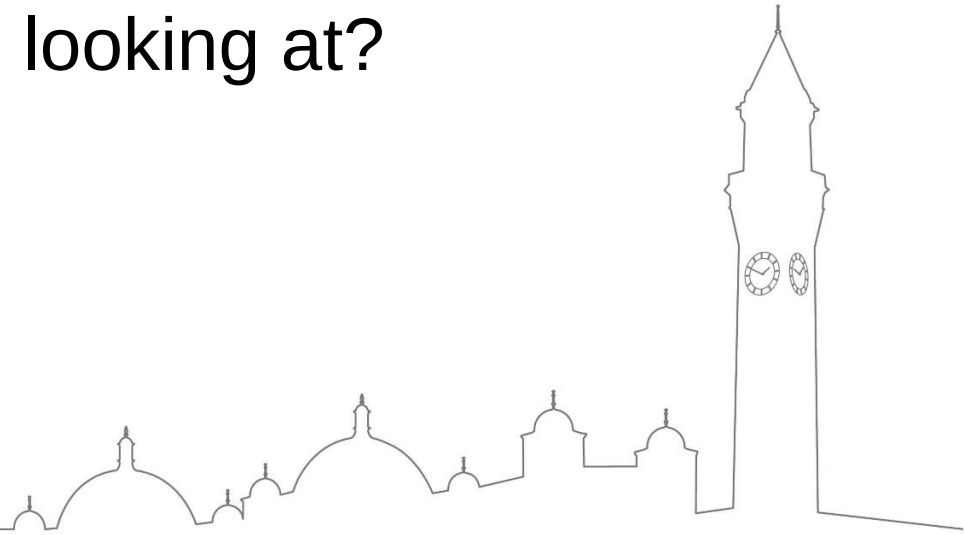
- From the cartoons shown by ITS3 (so far), this main PCB appears to mainly be housing (large) DC/DCs to power the sensors.





Why DC/DCs?

- DC/DCs are used to keep the material budget of power cables for sensors down.
- Enable transformation between the low voltage, high current power needed by the sensors (requires large wires to transport the high currents) and high voltage, low current supply power (lower gauge wire can be used, reducing material).
- However, how much power/current are we looking at?



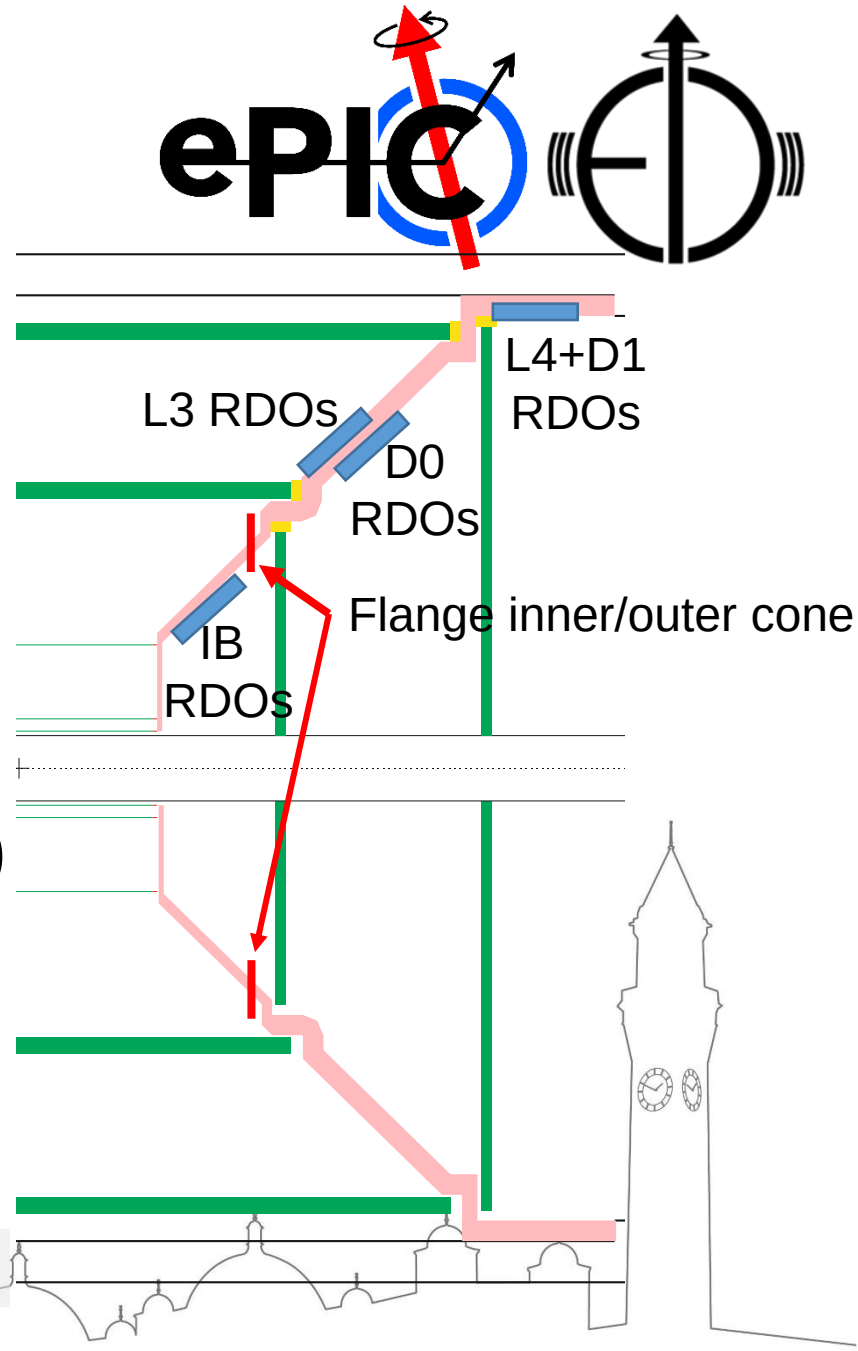
L2's global digital domain example

- For L2 (the outer-most layer of the IB) 5 sensor segments will be diced into one structure (quarter barrel).
- As these segments will be 1 piece of silicon, they need the same ground reference.
  - All 5 segments must be powered in parallel from the same PSU channel!
- The Global digital domain has the highest power requirement* on a single segment (approx. 1.2 V, 1.4 A).
  - ∴ this parallel circuit needs (O) 1.2 V, 7.0 A!
- That is quite a lot of current.

*See "ITS3's power domains" in Backup.

Keeping the current down

- Using DC/DCs could be an option* for keeping the current (from the PSU) and material down.
- How close can we get a DC/DC to the IB?
  - Will a similar sized board to ITS3 fit on the IB support cone (→)?
- Material (due to the wires for the high current) will still be high between the DC/DCs and sensors.
  - Probably also need other voltage regulators close to sensors (if wire length and IR-drop too great).



*This is not the only and may not even be the best option.

Double-sided power connections

- Wafer-scale sensors require power connections to both sensor peripheries (A-side/LEC, and C-side/REC).
- Both sides must be at the same potential/ground reference, and so need to connect to the same PSU channel.
  - Connection required to run along the barrel length.
- Voltages on both sides need to be balanced.

From ITS3 TDR:

"The half-detector presents a mechanical interface for the connection to the service support structure and power/data connectivity at the A-side (see Section 6.1 for additional information). From here, power lines reach the C-side FPCs, travelling along the CYSS (Fig. 4.3.a)."

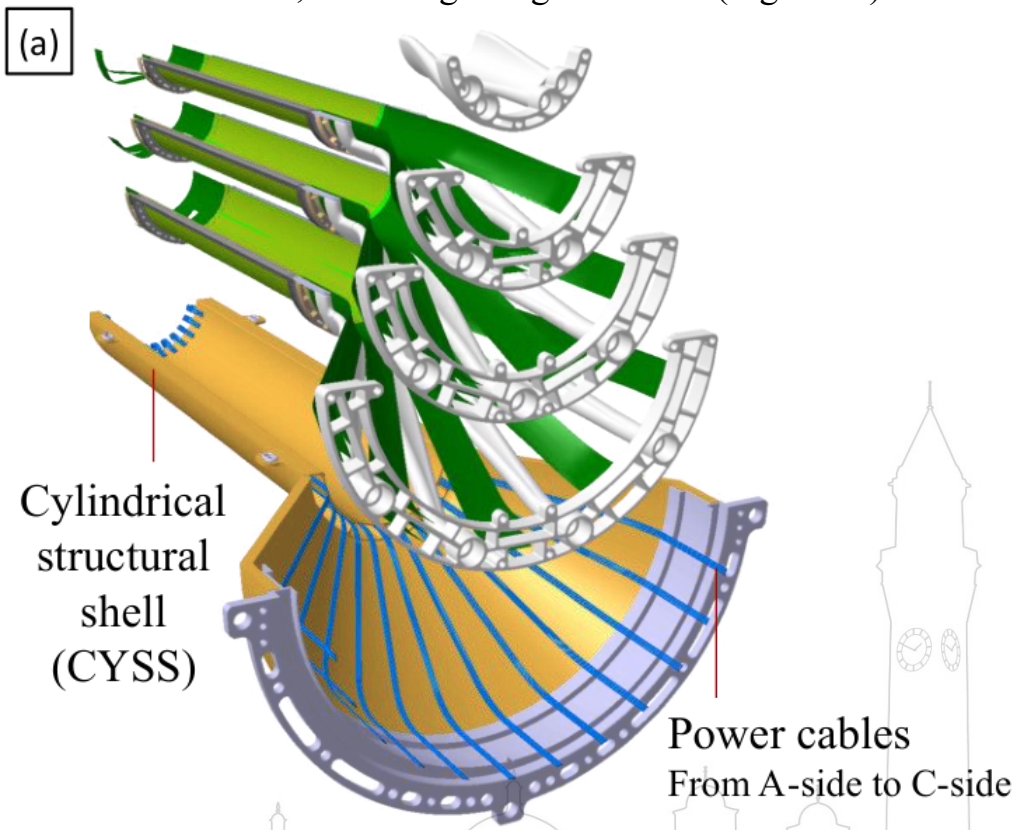
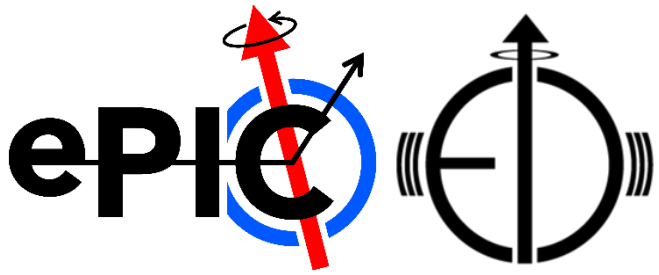


Figure 4.3: Half-detector: (a) Exploded

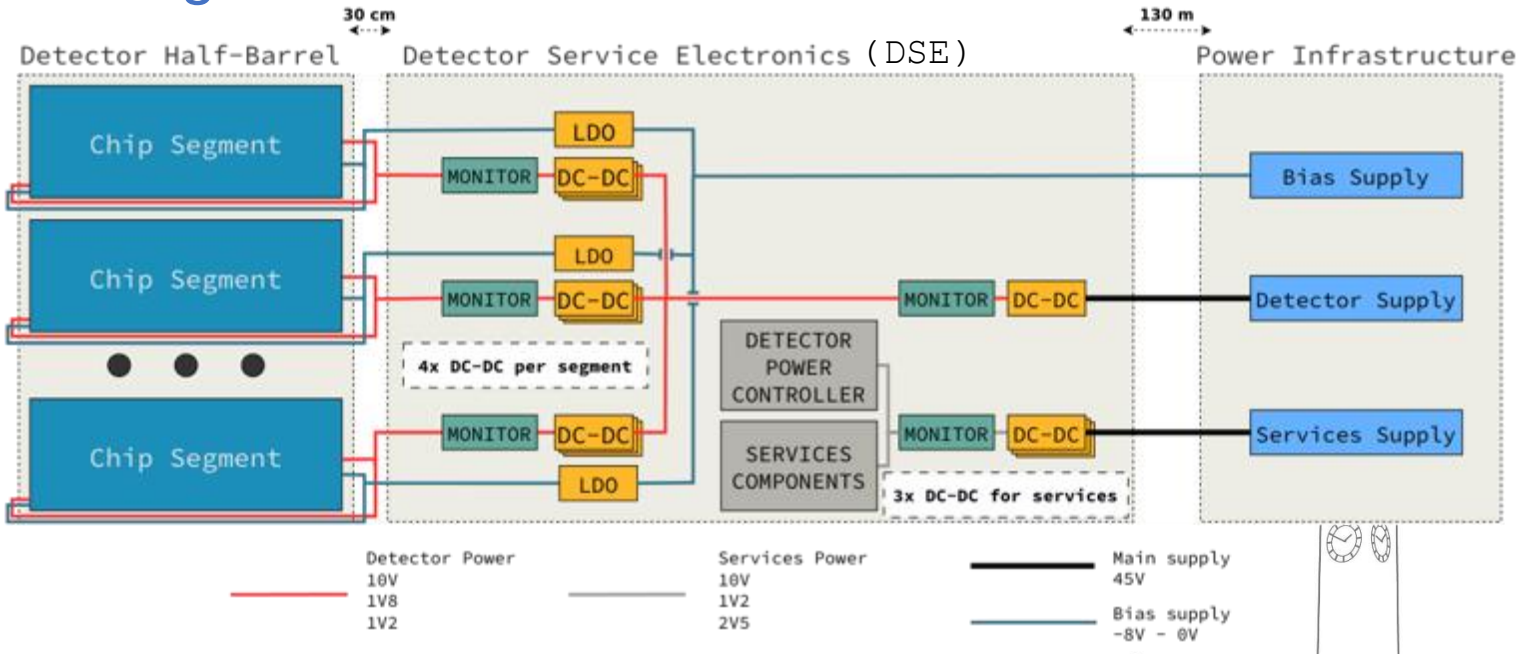
ITS3's power distribution summary



[See section 6.1.2 from ITS3 TDR]:

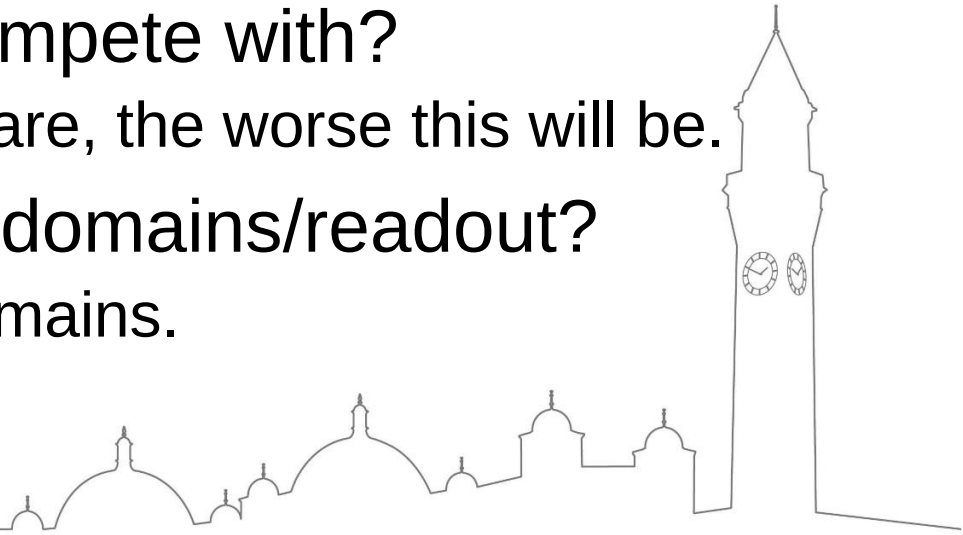
ITS3 half-barrel = ePIC quarter-barrel

- Detector supplied with 1.2 V via both edges.
  - Achieved by resistance matching of the cables.
- bPol DC/DC, converting from 48 V.
  - Efficiency: ~60%.
- lpGBT ASICs to provide ADCs for current monitoring.
- DSE to be water-cooled!



Questions (1)

- Could a selection of linear voltage regulators be an option to get the supply current down?
  - How many regulators would be needed (for a comparable current reduction to the DC/DC)?
  - Would they be less material than one DC/DC?
- Where could regulators be placed on the support structure?
- How much of an IR-drop do we have to compete with?
  - The longer wires (especially at high currents) are, the worse this will be.
- Do we use the same method for all power domains/readout?
  - Current is less problematic for other power domains.



Questions (2)

- Is resistance matching the best way to go for balancing voltages on both sides of the wafer-scale sensors?
  - Would we be better with regulators on both sides?
- Could the regulation (close to the sensors), after the DC/DC be done with the S-LDO (in LDO-mode)?
- This would include the additional 1.8 V S-LDO (suggested for the ancillary ASIC) to regulate for the Serialisers domain of the wafer-scale sensors (as there are no plans to modification to this sensor and remove the in chip LDOs).

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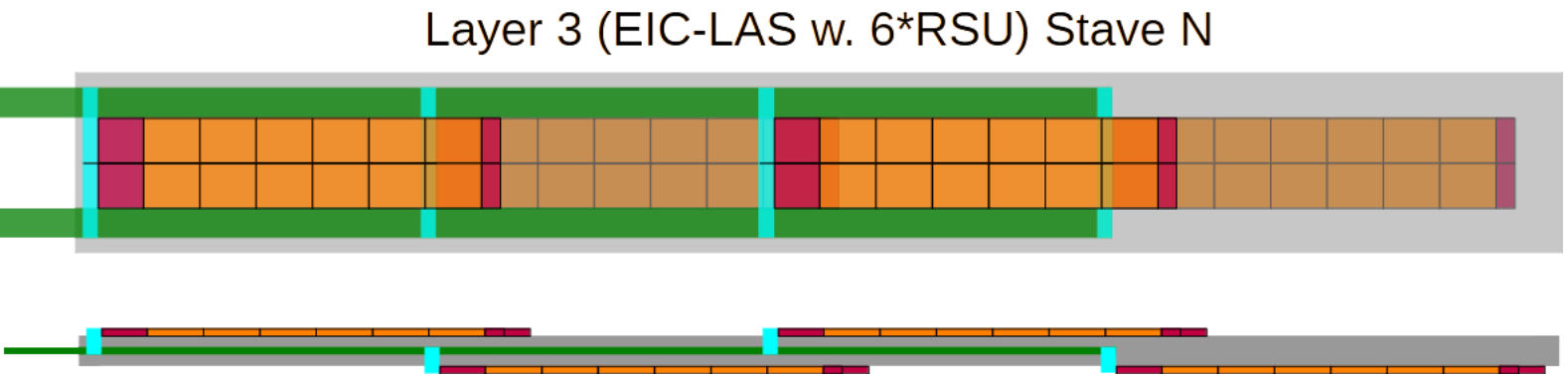
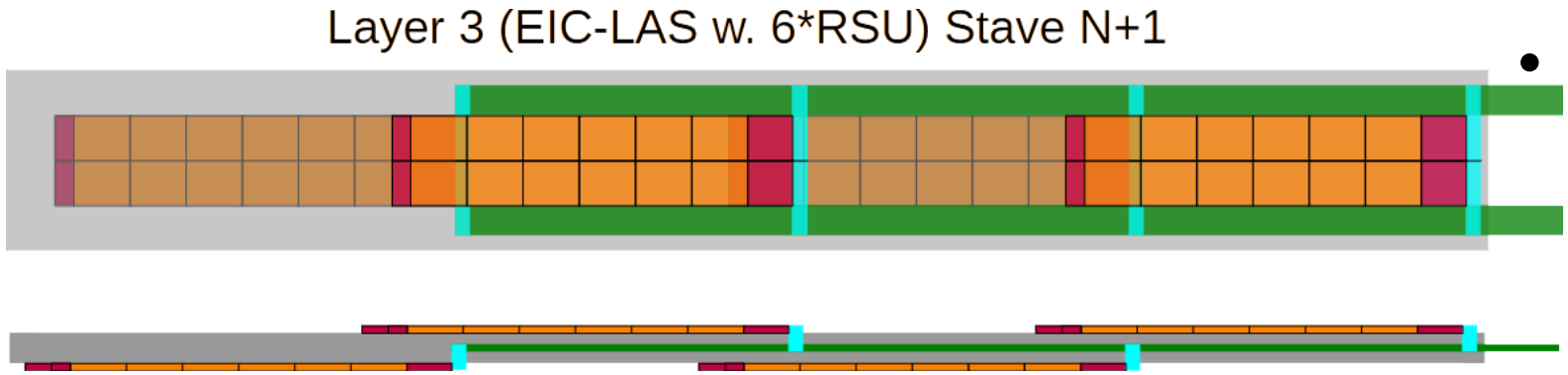
Thank you very much!

Any questions?

Additional (support) slides

Likely L3 (6 RSU) layout

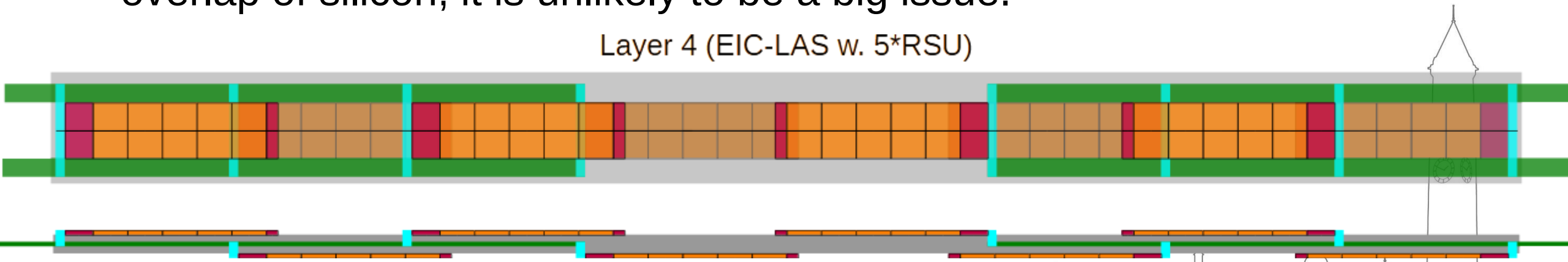




- Both FPCs (on 1 stave) are likely to come from the same stave edge.
  - Having neighbouring EIC-LAS in the same orientation for easier mounting.
- If so, alternating staves would need to be connected to from opposite sides (to balance material).

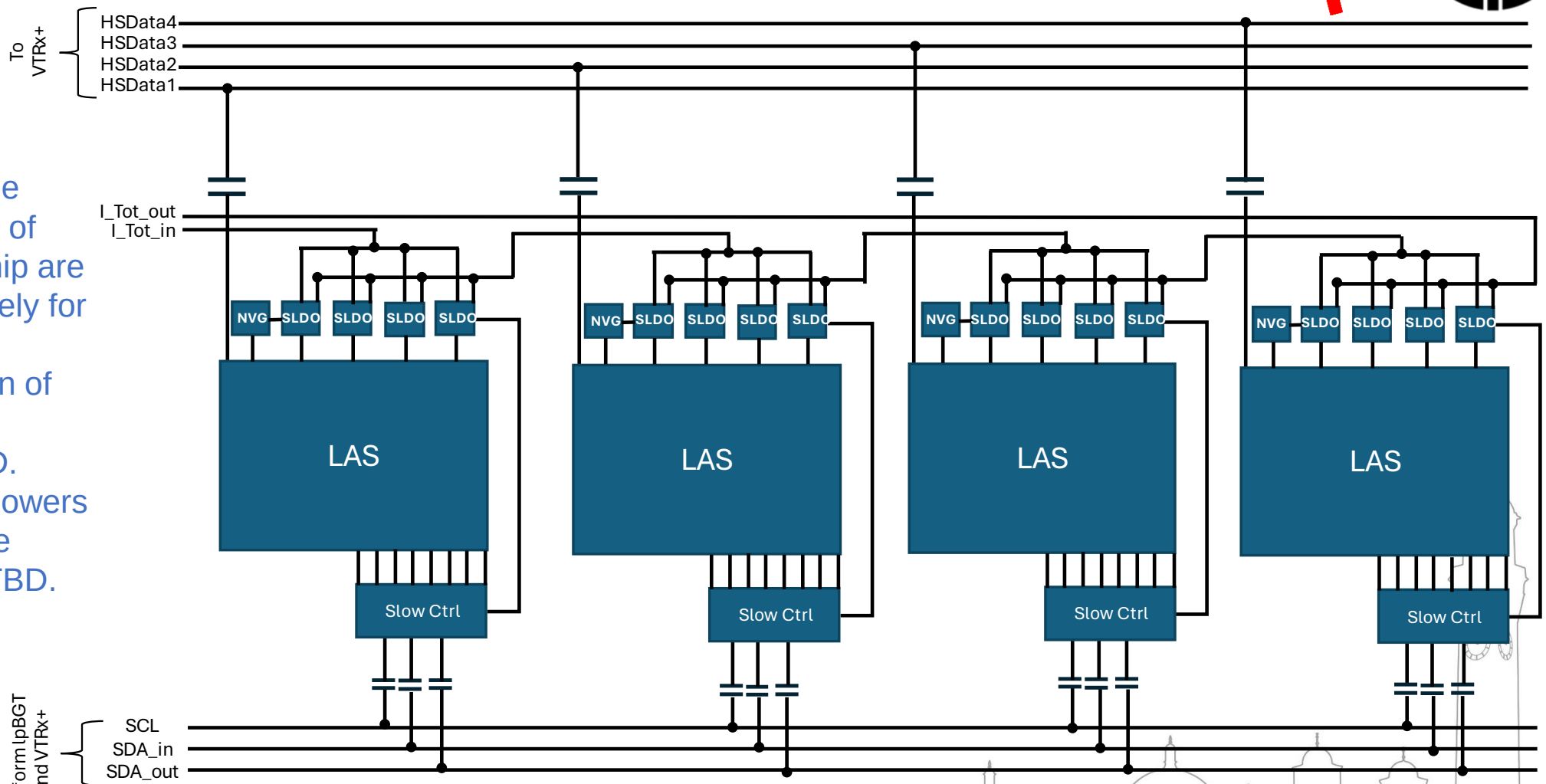
Layer 4 (5 RSU) layout

- To enable multiples of 4 in a L4 stave, shorter 5 RSU long EIC-LAS would be closer to the suggested stave lengths (slightly too long).
- This will lead to needing some additional overlap of RSUs to get to the required lengths.
- As material budget for L4 is 0.55% X/X_0. As this is a (relatively) small overlap of silicon, it is unlikely to be a big issue.



EIC-LAS connections on FPC

- On this slide the three functions of the ancillary chip are shown separately for clarity.
- Precise location of AC-coupling capacitors TBD.
- Which SLDO powers what part of the auxiliary chip TBD.



Schematic drawing by Marcello Borri (STFC)