EIC-LAS:
data and slow control

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Introduction

- The OB and disks will use the EIC-LAS sensor
- The EIC-LAS is one segment of 1x5 or 1x6 RSUs plus LEC for power and data
  - There is probably also going to be a REC to terminate the design; no power or data connection
- The EIC-LAS will have one data link
- The EIC-LAS works with an auxiliary chip that will provide
  - Current to voltage conversion for the serial powering scheme – SLDO
  - Negative voltage generation to bias the sensor – NVG
  - Slow control interface – Slow Ctrl
- In the current OB and disks design concepts, groups of up to 4 EIC-LAS sensors will be one powering, data, slow control unit
- An FPC will route power, data and slow control between sensors and auxiliary chips on the staves/disks and the readout and control boards

EIC-LAS power and sensor bias

Power Domains and Currents

Supply purpose	Nets	Voltage [V]	Current [mA]	Pads on LEC	Pads on REC
Services	SDVDD-SDVSS	1.2 to 1.32	227	Yes	Yes
Global analog	GAVDD-GAVSS	1.2 to 1.32	540	Yes	Yes
Global digital	GDVDD-GDVSS	1.2 to 1.32	1369	Yes	Yes
Serializers	TXVDD-TXVSS	1.8	200	Yes	No
Substrate bias	PSUB	−1.2 to 0			

Table 3.11: Power domains of one sensor segment. The substrate bias is common to all the segments composing a sensor. The nominal operating voltage are referred to the potential of the GAVSS input net. The input currents are obtained assuming the maximum estimated power consumption of the LEC and RSU circuits at 25 °C.

From: 20th Nov '23, EP R&D WP 1.2 – G. Rinella, "Design of MOSAIX - ER2 Stitched Sensor Prototype", https://indico.cern.ch/event/1339888/contributions/5680443/attachments/2755393/4797584/20231120-ER2-Stitched-Sensor.pdf

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From the serial powering supply through four SLDO regulators

- 3 domains all around +1.2 V
  - Services
  - Global analogue
  - Global digital
- 1 Serializers domain at +1.8 V.

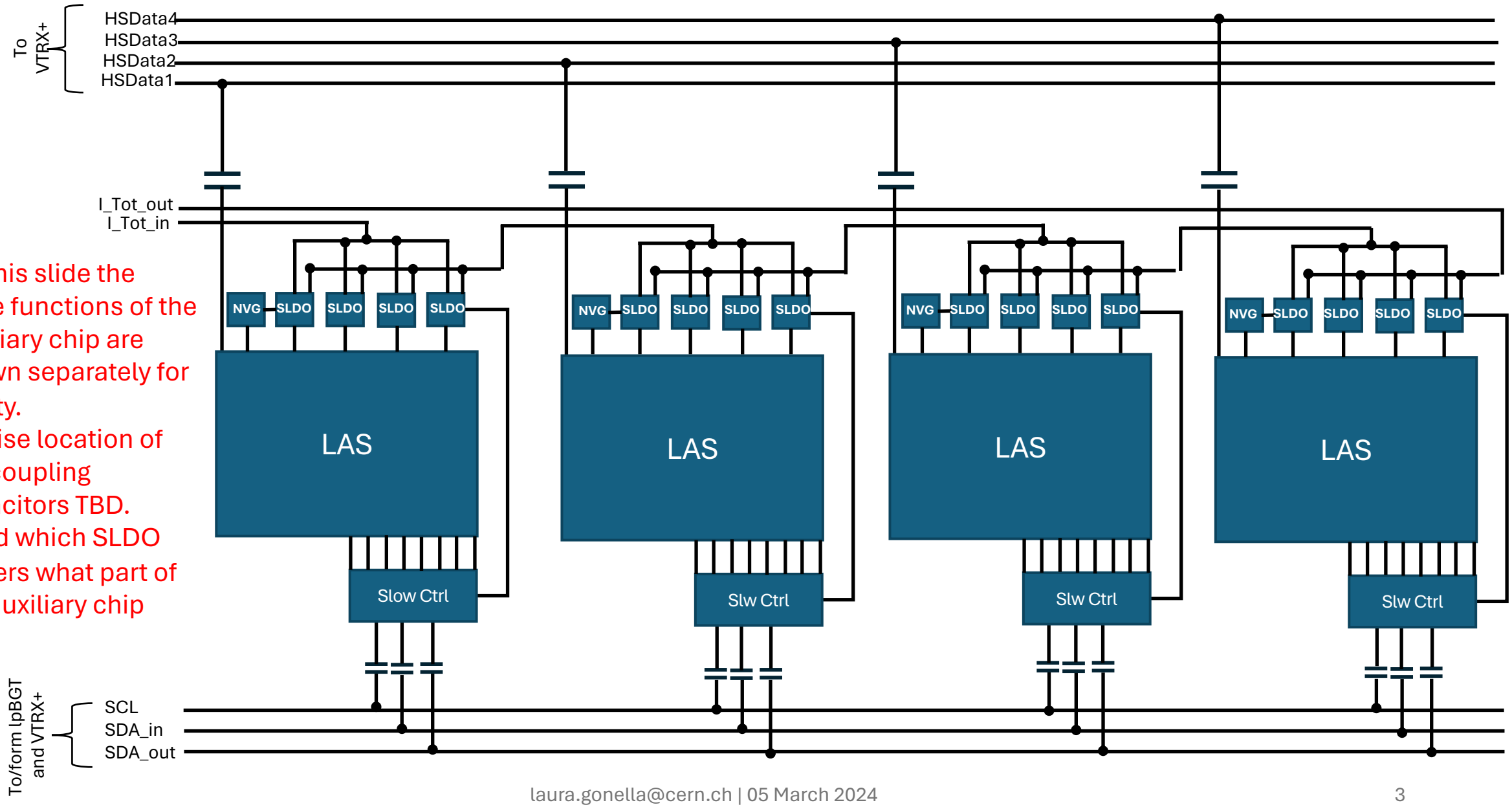
- 1 Substrate bias domain at -1.2 V.

Sensor bias from the NVG

EIC-LAS connections on FPC along stave/disk

Schematic drawing by Marcello Borri (STFC)

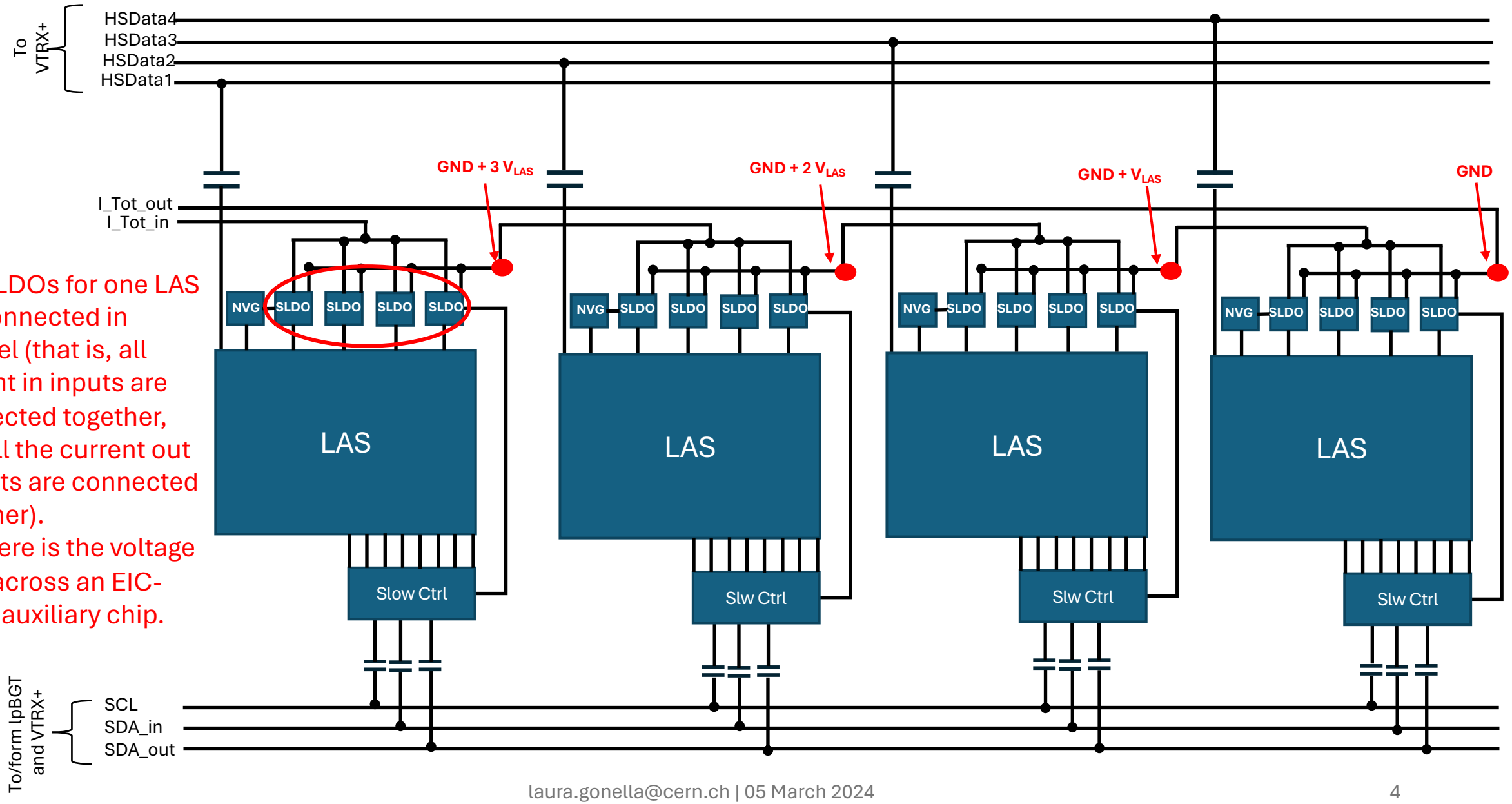
- On this slide the three functions of the auxiliary chip are shown separately for clarity.
- Precise location of AC-coupling capacitors TBD.
- If and which SLDO powers what part of the auxiliary chip TBD.



EIC-LAS connections on FPC along stave/disk

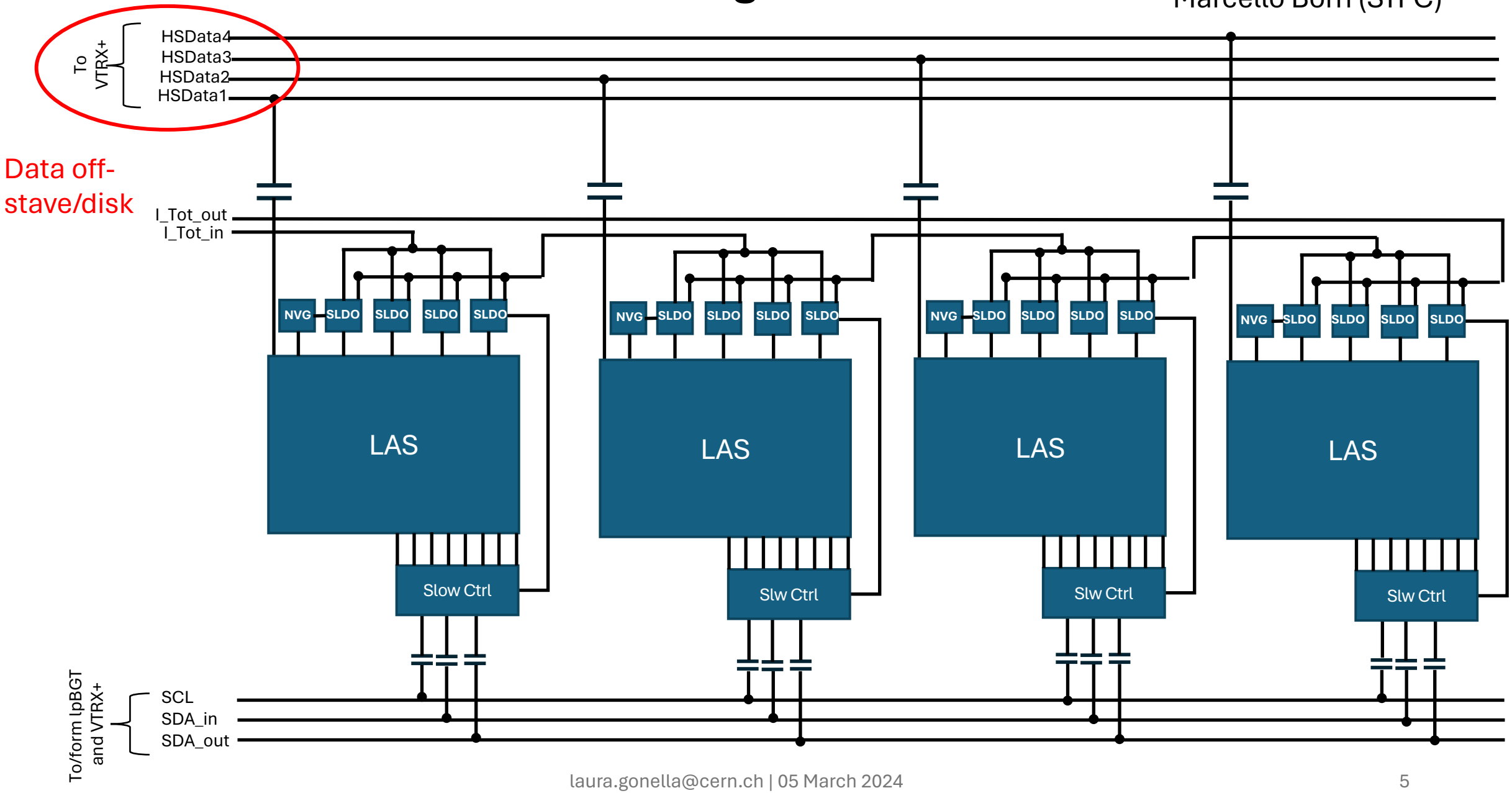
Schematic drawing by Marcello Borri (STFC)

- The SLDOs for one LAS are connected in parallel (that is, all current in inputs are connected together, and all the current out outputs are connected together).
- V_{LAS} here is the voltage drop across an EIC-LAS + auxiliary chip.



EIC-LAS connections on FPC along stave/disk

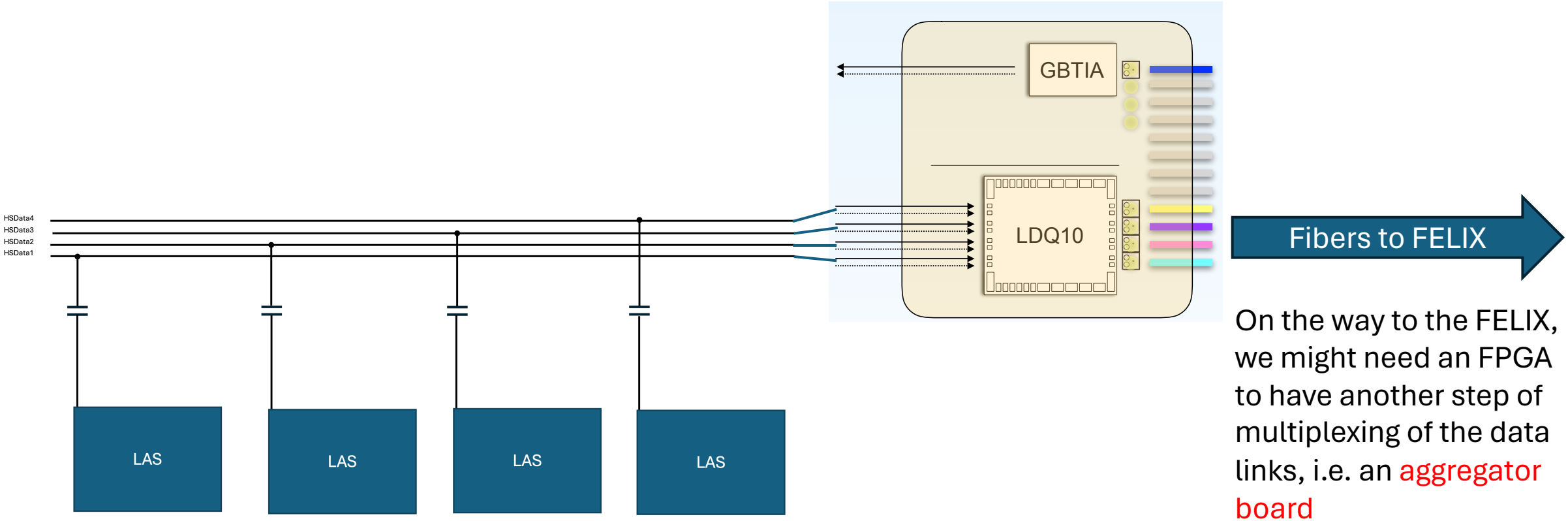
Schematic drawing by
Marcello Borri (STFC)



Data from stave/disk to control room

Up to 4 EIC LAS to 1 VTRX+ to 4 fibers
# of EIC-LAS = # data fibers at the output of the VTRX+

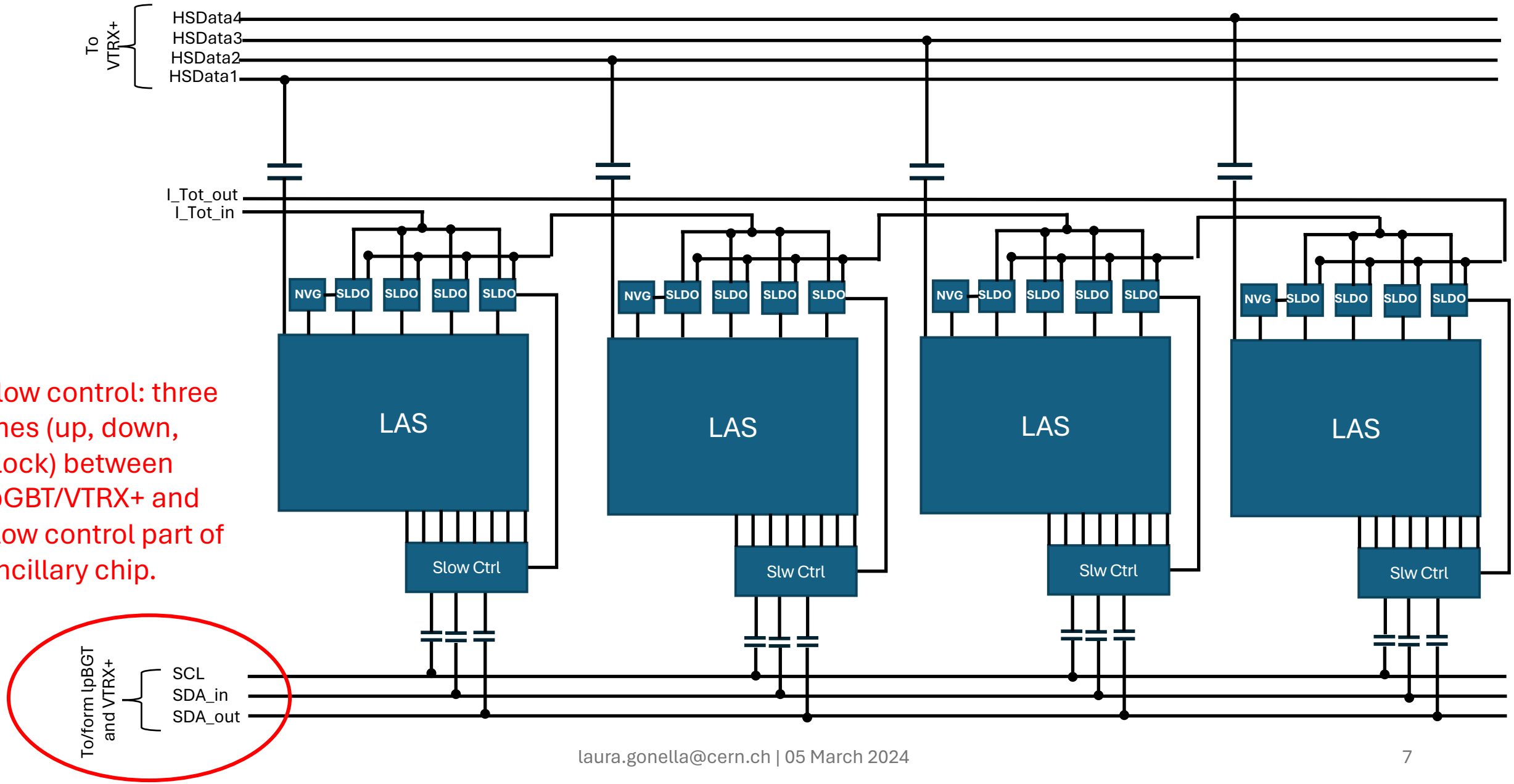
VTRX+ on readout board at end of stave/disk



On the way to the FELIX, we might need an FPGA to have another step of multiplexing of the data links, i.e. an aggregator board

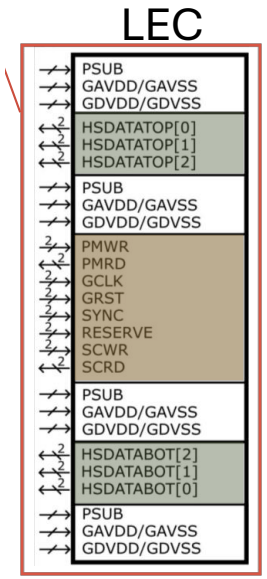
EIC-LAS connections on FPC along stave/disk

Schematic drawing by Marcello Borri (STFC)



Slow control: three lines (up, down, clock) between lpGBT/VTRX+ and slow control part of ancillary chip.

EIC-LAS slow control interface to stave/disks



All I/Os are differential

6x 5.12 Gb/s data outputs

1x clock at 320 MHz

2x slow control at 2.5 Mbps

Global analog and digital supplies per *segment*

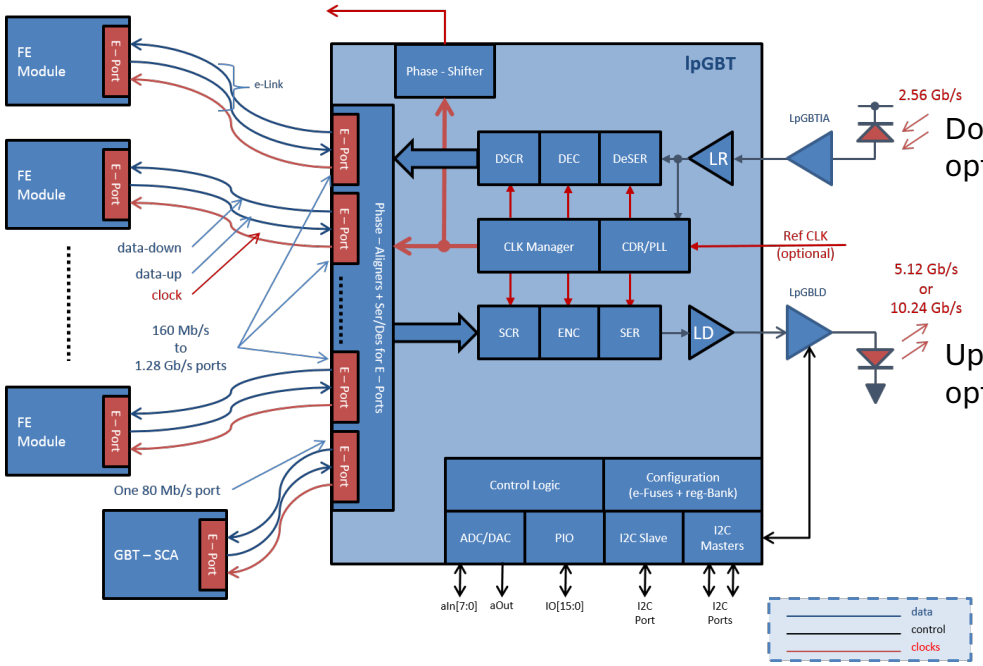
On-chip supply segmentation and control

Reverse biasing of substrate (PSUB)

Down	**Up**
PMWR	PMRD
SCWR	SCRD
GCLK	
GRST	
SYNC	

lpGBT

From the lpGBT manual



Down-link:
optical fiber at 2.56 Gbps

Up-link:
optical fiber at 5.12 or 10.24 Gbps

Output eLinks (down-link)			
Bandwidth [Mb/s]	80	160	320
Maximum number	16	8	4

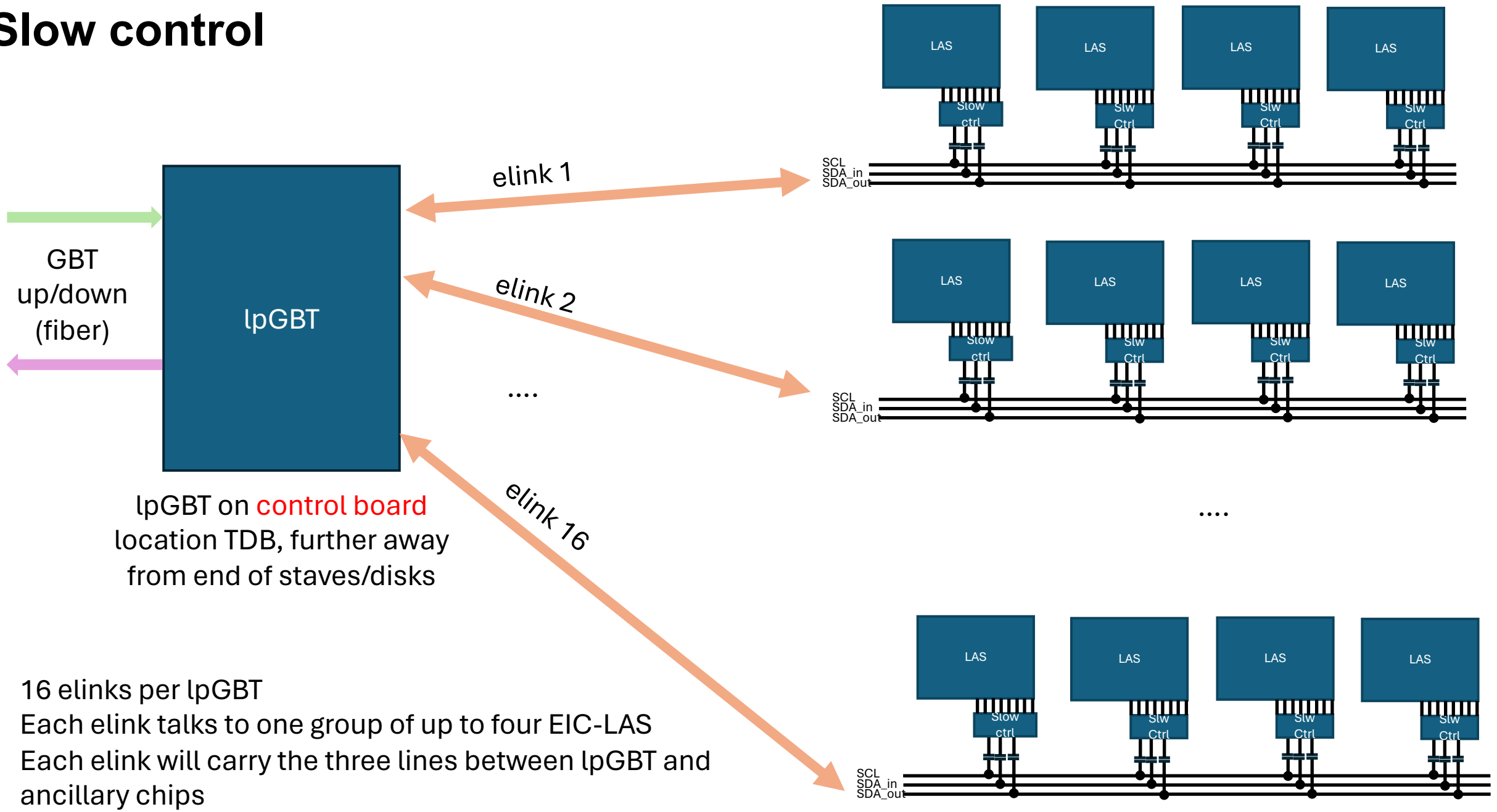
Input eLinks (up-link)												
Up-link bandwidth [Gb/s]	5.12						10.24					
FEC coding	FEC5			FEC12			FEC5			FEC12		
Bandwidth [Mb/s]	160	320	640	160	320	640	320	640	1280	320	640	1280
Maximum number	28	14	7	24	12	6	28	14	7	24	12	6

Electrical links (eLinks) interconnect the lpGBT with the front-end electronics (detector modules or ASICs) (see Fig. 1.2). They consist of three differential pairs: two to transmit data from the front-end to the lpGBT (input eLinks) or from the lpGBT to the front-end (output eLinks) and a differential pair to transmit a clock to the front-end. Notice that, because of the asymmetric bandwidth of the up and downlinks, the number of input and output eLinks is not the same. The same is true for the bandwidth of the input/output eLinks. The number of **clock eLinks (eClocks)** available is the same as the number of input eLinks. The bandwidth of the eLinks is programmable and, in the case of the input eLinks, it also depends on the uplink bandwidth (5.12 or 10.24 Gb/s) and on the FEC code selected (FEC5 or FEC12).

- Each elink has three differential pairs : 1 data-down (output elink), 1 data-up (input elink), 1 clock

- For one down-link at 2.56 Gbps, there can be 16 output elinks at 80 Mbps
- For one up-link at 5.12 Gbps (FEC12), there can be 16 input elinks at 160 Mbps

Slow control



lpGBT on control board location TDB, further away from end of staves/disks

- 16 elinks per lpGBT
- Each elink talks to one group of up to four EIC-LAS
- Each elink will carry the three lines between lpGBT and ancillary chips

Boards

Readout board

- Located at the end of staves/disks; could be an extension of the FPC
- Each serves a group of up to four EIC-LAS
- Hosting the VTRX+
- Routing data lines from FPC to VTRX+
- Routing serial powering current to/from FPC
- Routing slow control I2C lines to to/from FPC
- Hosting connection for current and slow control (elinks) cables
- Hosting connection for readout board power cables

Aggregator board

- Further out, possibly outside of the ePIC detector volume, before FELIX
- Aggregates data fibers
- Hosting commercial FPGA
- Hosting connection for fibers from readout board
- Hosting connection for fibers to FELIX
- Hosting connection for aggregator board power cables

Boards

Control board

- Location TBD, can be further away from staves/disks as speed of slow control lines is low
- Hosting the lpGBT and VTRX+
- Hosting connection for down-link and up-link
- Hosting connection for 16 elinks (cables? FPC?)
- Hosting connection for control board power cables

Notes

- Identify who works on what board
  - Specify power consumption and area of each board
  - Develop powering scheme for these board
  - “Connection” for now left generic, needs specifying what type of connection

Conclusion

- High level sketch of data and slow control paths presented
- Provided to give an overview and highlight areas that need better definition/work/resources assigned
- Three boards needed: readout, aggregator, slow control
  - Need to identify workforce
- Number of VTRX+ and lpGBT presented at the TIC meeting 4 December and currently being checked; update to be given at one of the next SVT meetings