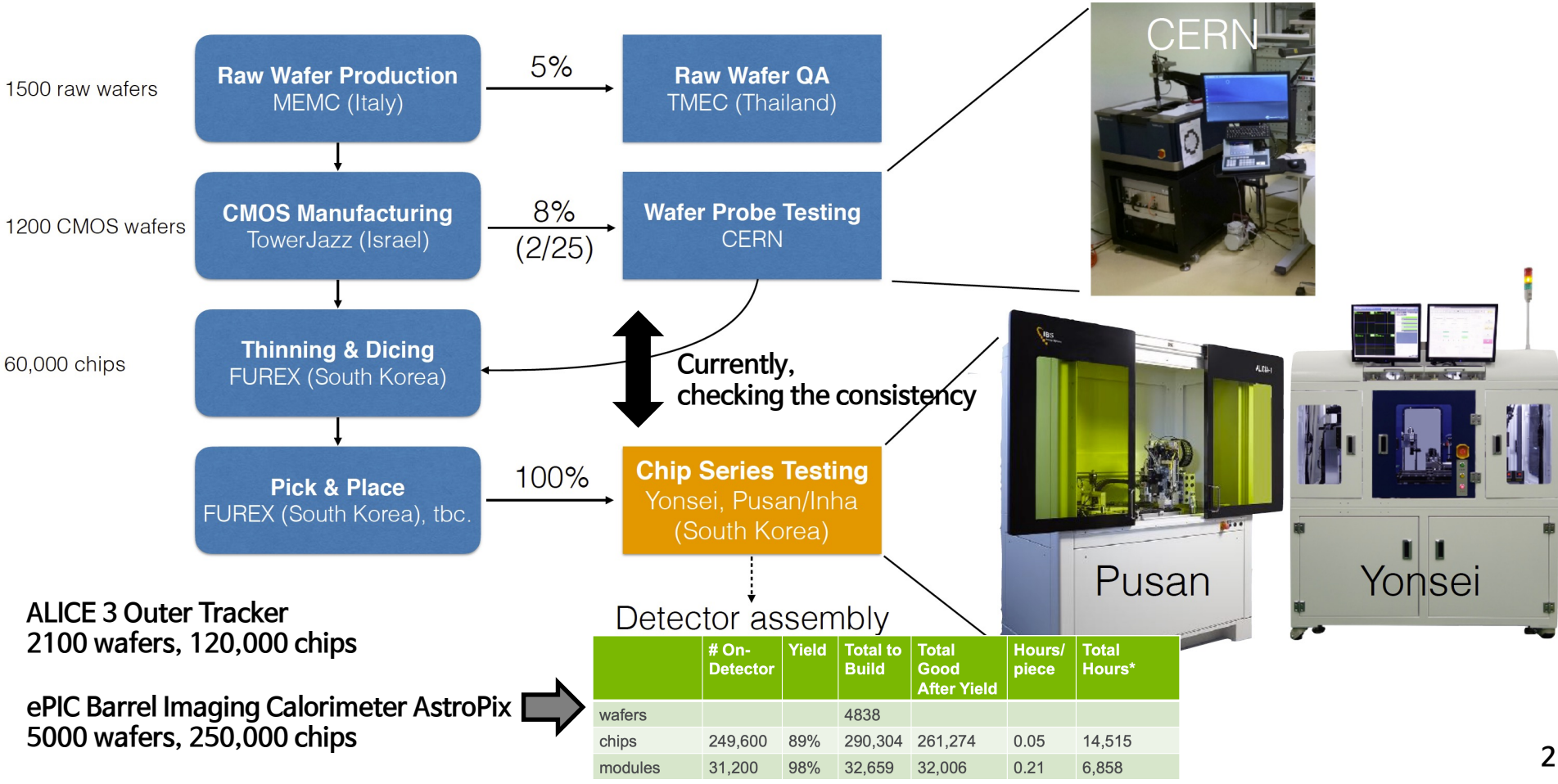


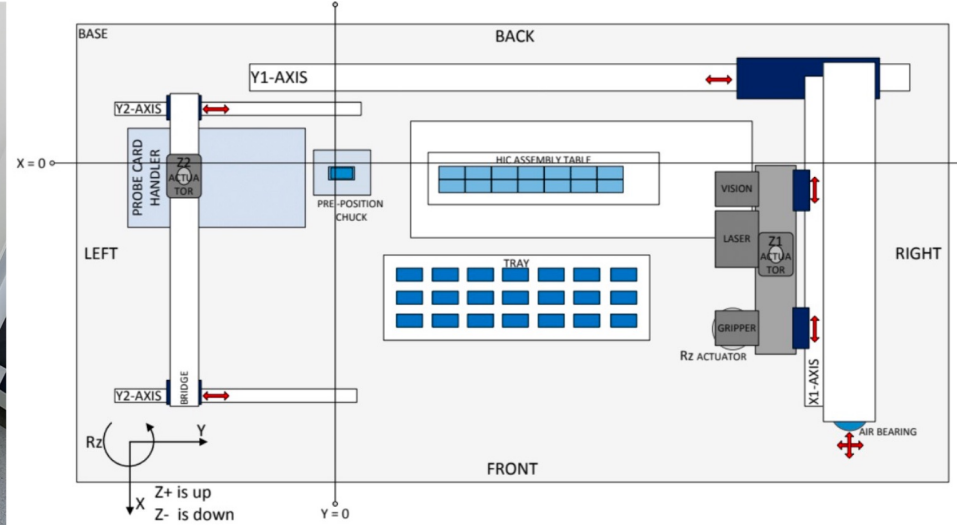
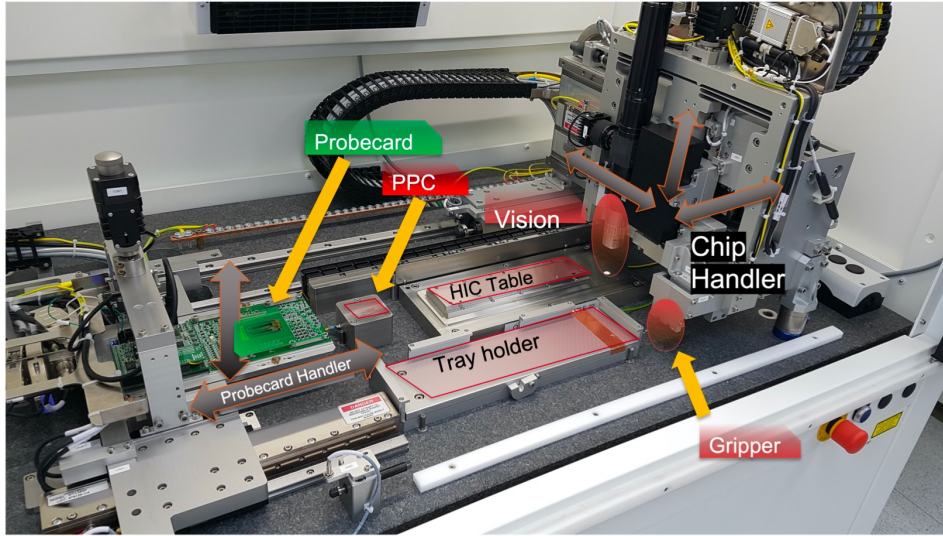
Wafer QC

Sanghoon Lim
Pusan National University

Overview of chip production and test for ALICE ITS2

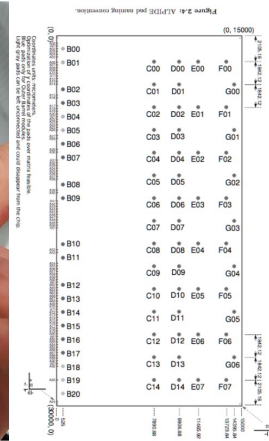
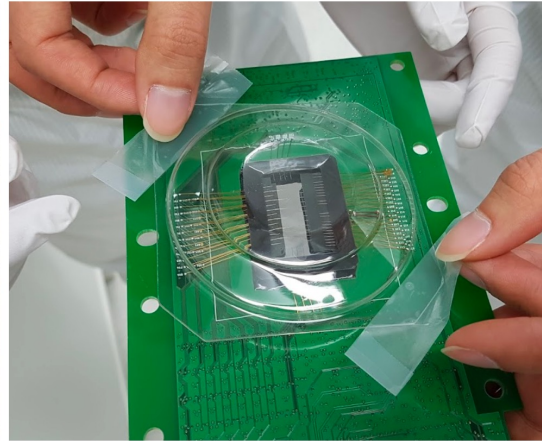
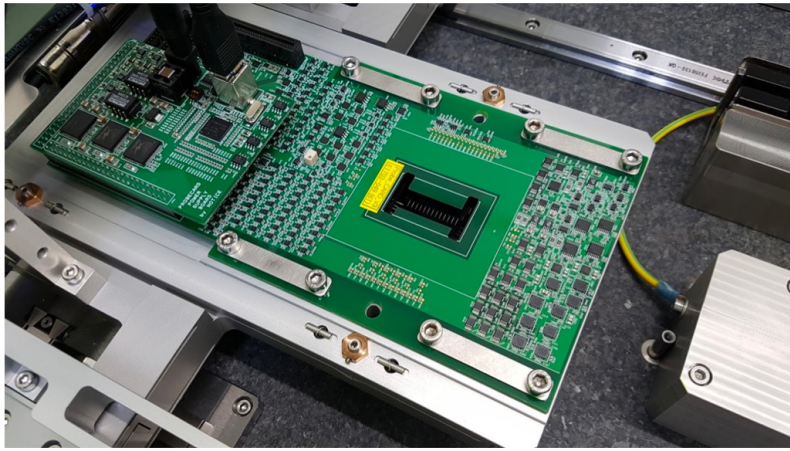
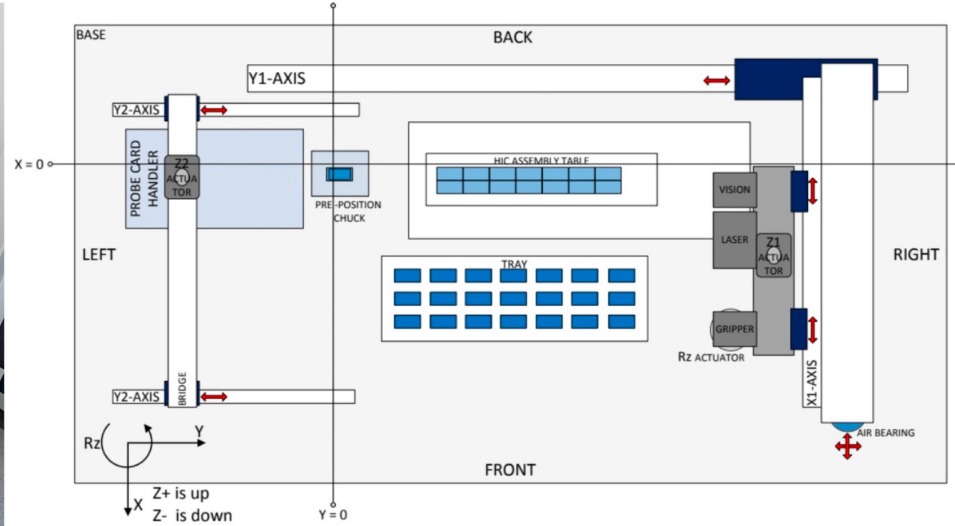
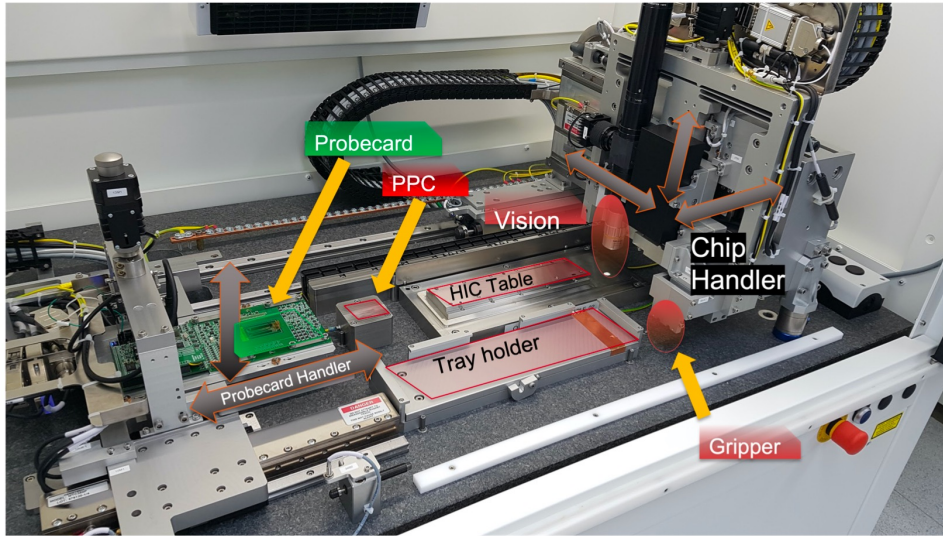


Chip test machine (ALICE ITS2, ALICIA)



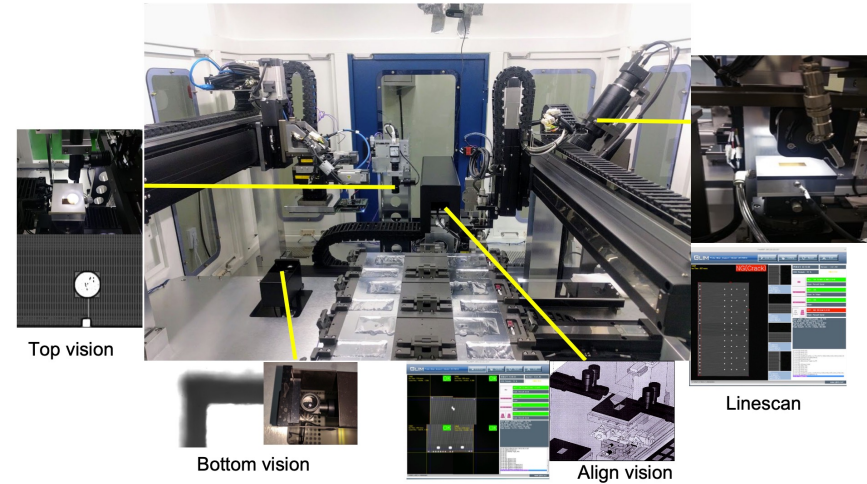
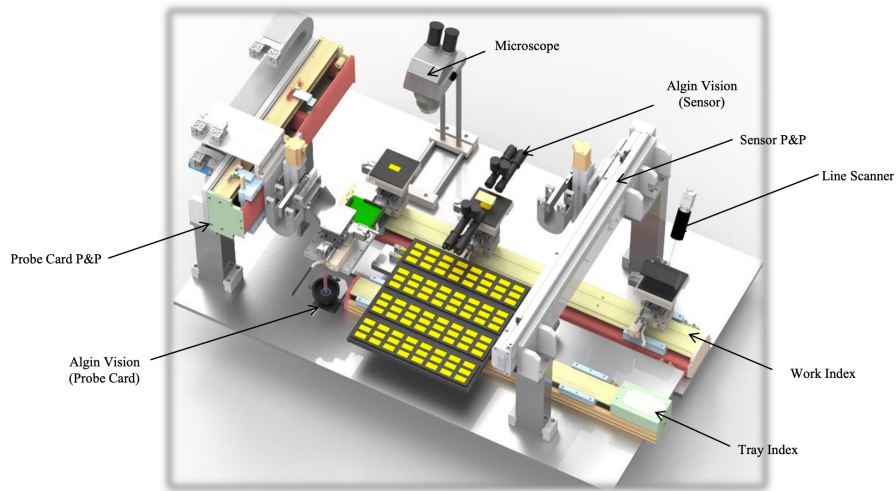
- Two PCs control the chip test system
- One (right) PC to control the chip handler
- Another (left) PC to control the probe card
- Two PCs are communicating to check the status and transfer test results

Chip test machine (ALICE ITS2, ALICIA)

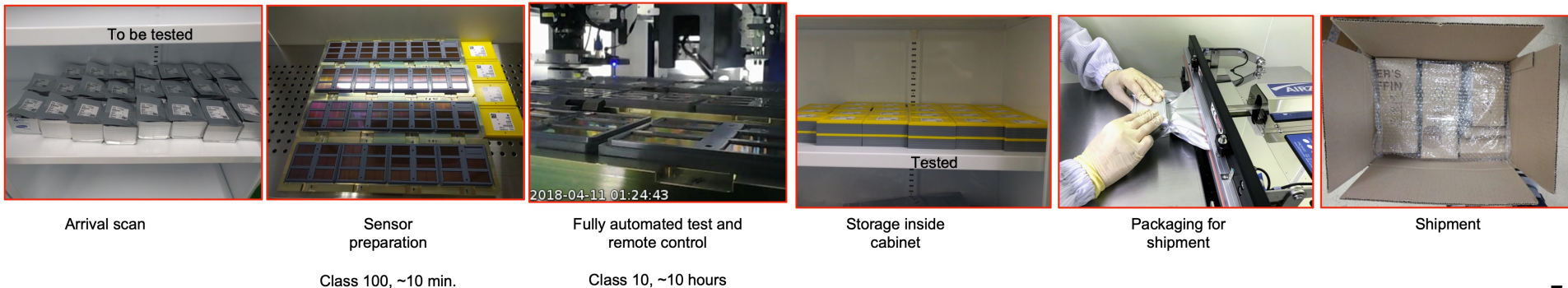


Need an extra circuit to check electrical contact between needles and bonding pads

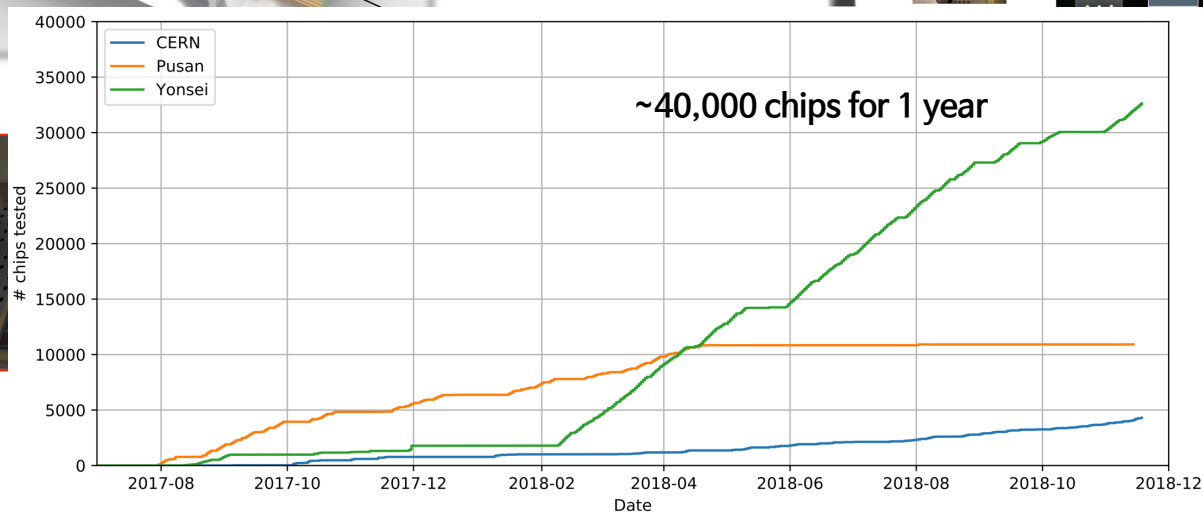
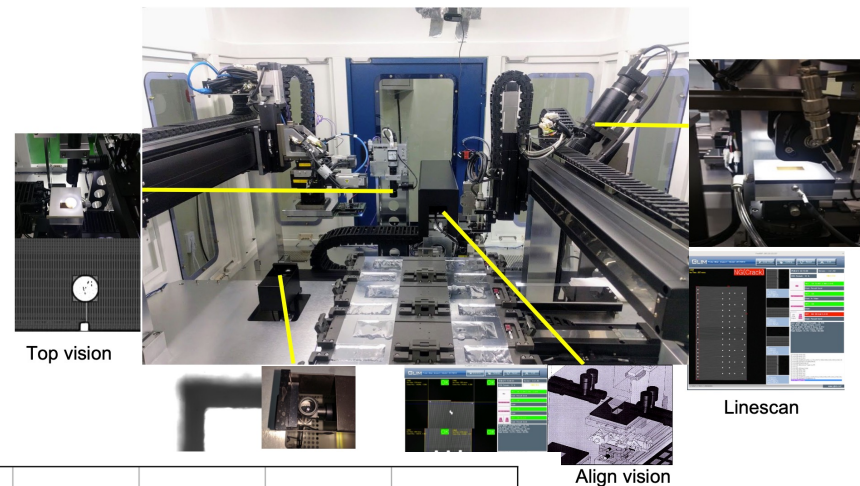
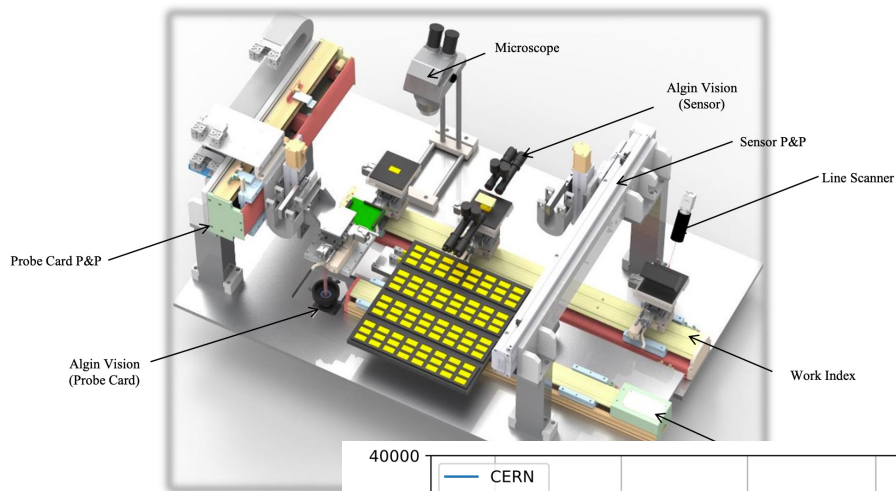
Chip test machine (ALICE ITS2, COREA-YS-01)



A simpler version of the machine dedicated to chip test



Chip test machine (ALICE ITS2, COREA-YS-01)



Arrival scan

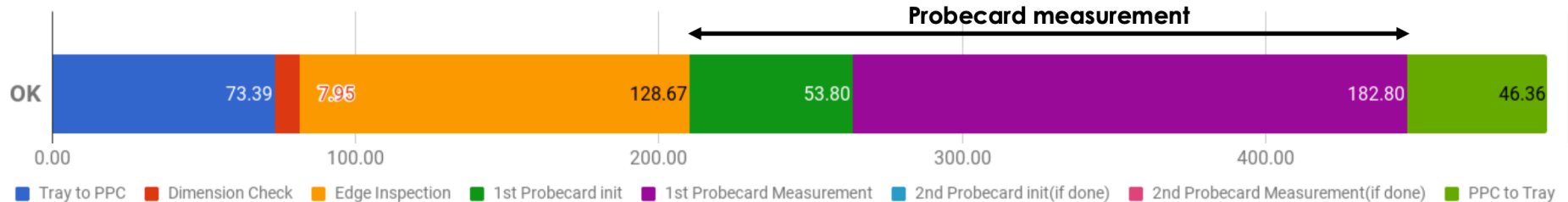


Shipment

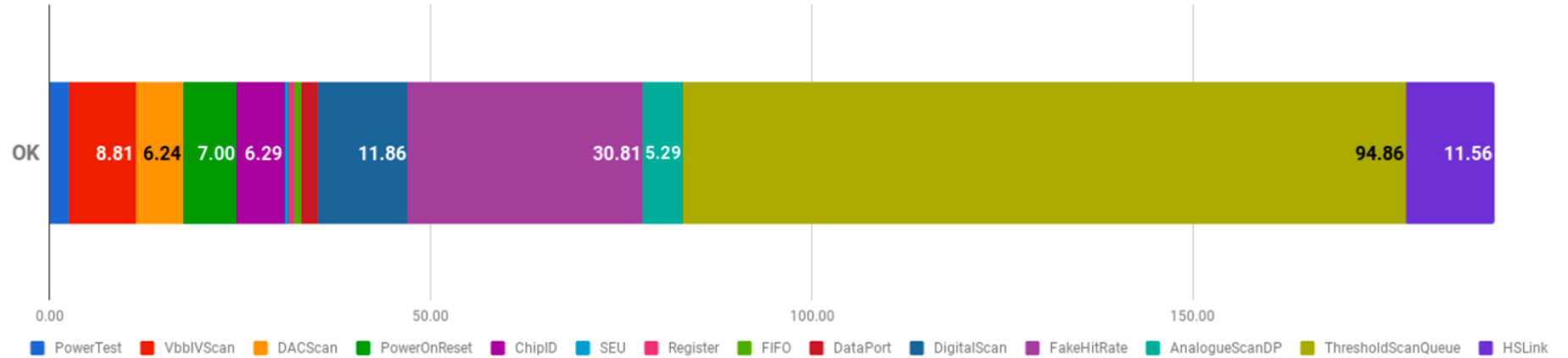
ed to chip test

Chip test procedure (ALPIDE)

Chip Test Time



Probecard Measurement Time

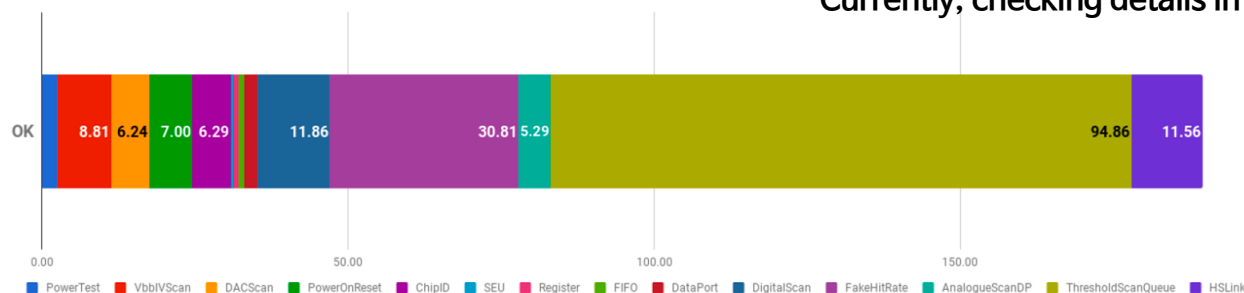


Chip test procedure (ALPIDE)

- **Powering test:** just power on/off
- **V_{bb} I-V test:** apply the reverse substrate bias from 0 V down to -6 V
- **DAC scan:** verify that each DAC is working by scanning through all its code words
- **Power on reset test:** check the functionality of power on reset
- **SEU check:** monitor the SEU counter and the flag bits on idle operation
- **Register test:** check all registers by writing and reading back to find stuck bit
- **FIFO test:** check all the generated memory blocks
- **Data port test:** verify its functionality to send quasi-static patterns in case of the readout test failure
- **Digital scan:** inject single hits directly into the in-pixel memories and read back
- **Fake hit rate:** measures the number of noisy pixels and faulty front-ends
- **Analog scan DP:** exercise the analog front-end and the full readout chain of ALPIDE
- **Threshold scan:** test all analog front-ends/pixels by using analog pulse injection
- **High speed link check:** check its functionality

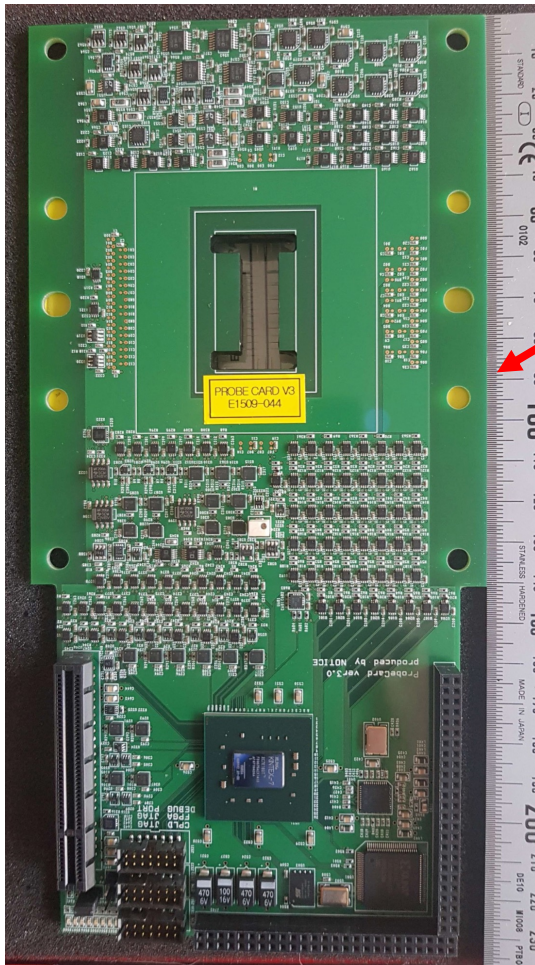


Probecard Measurement Time

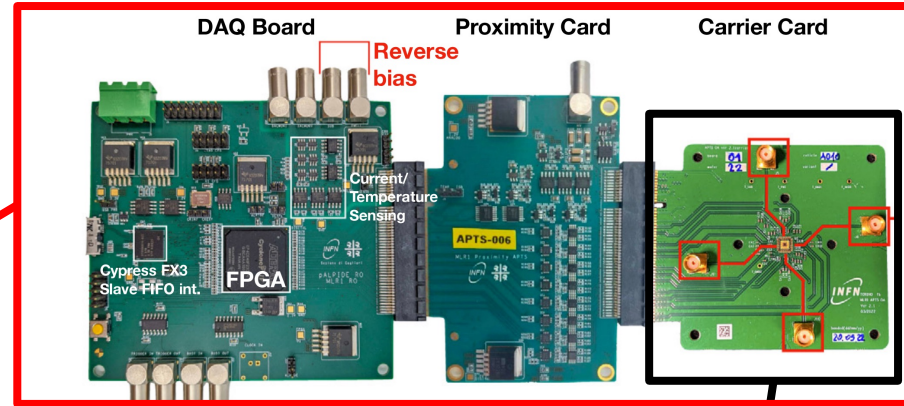


Currently, checking details in software and firmware

Probe card for ALICE ITS2/3

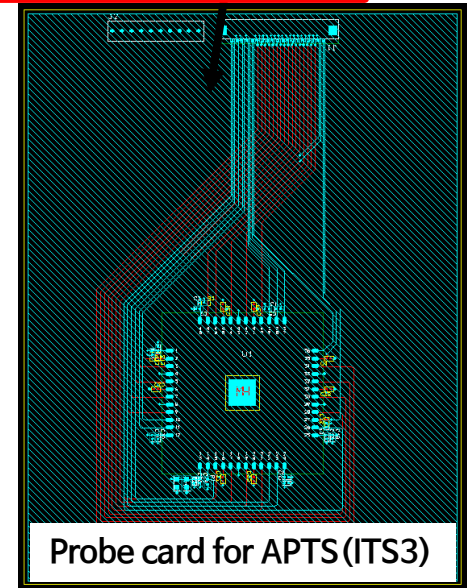
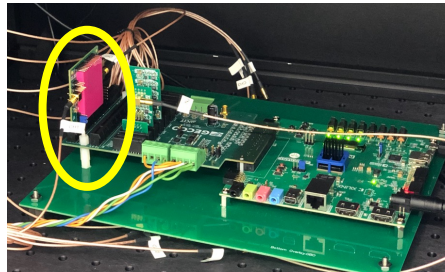


Probe card for ALPIDE



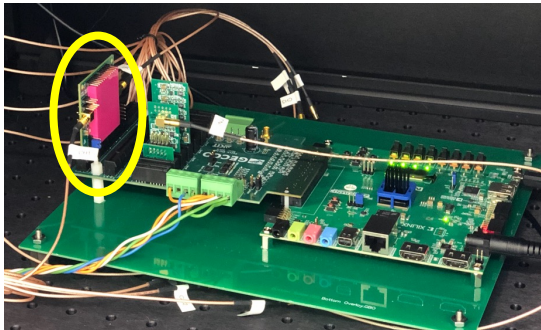
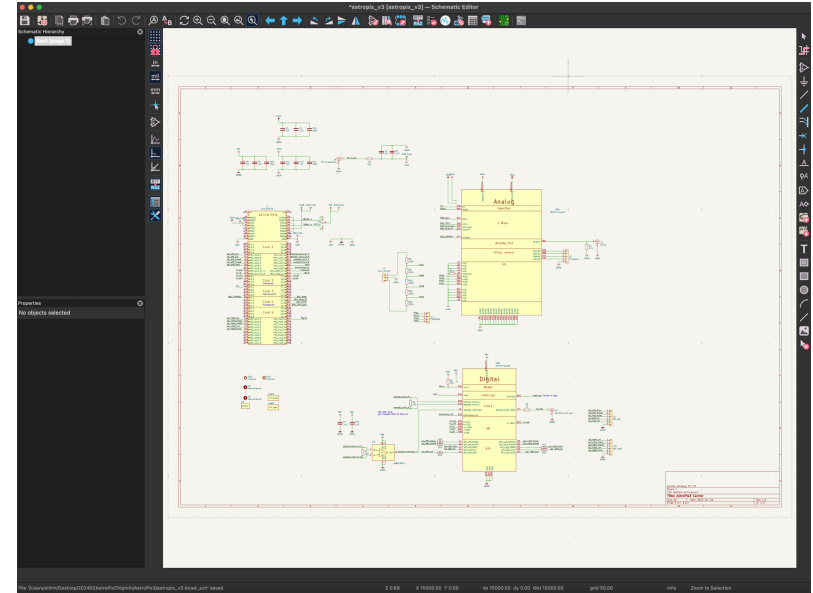
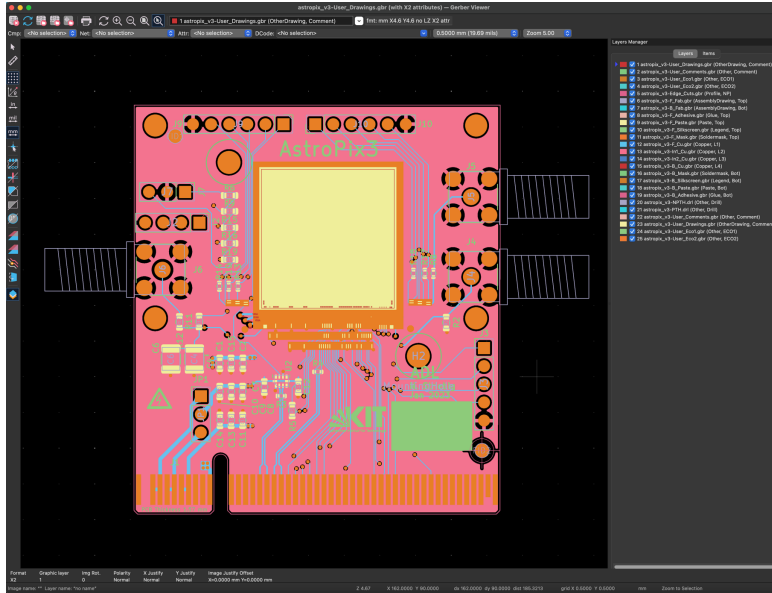
Trig. I/O Busy I/O

- Initial version for AstroPix v3: a simple version for the carrier card only
- Considering the same dimension as the ITS2 probe card to utilize the ALICIA machine for the initial test



Probe card for APTS (ITS3)

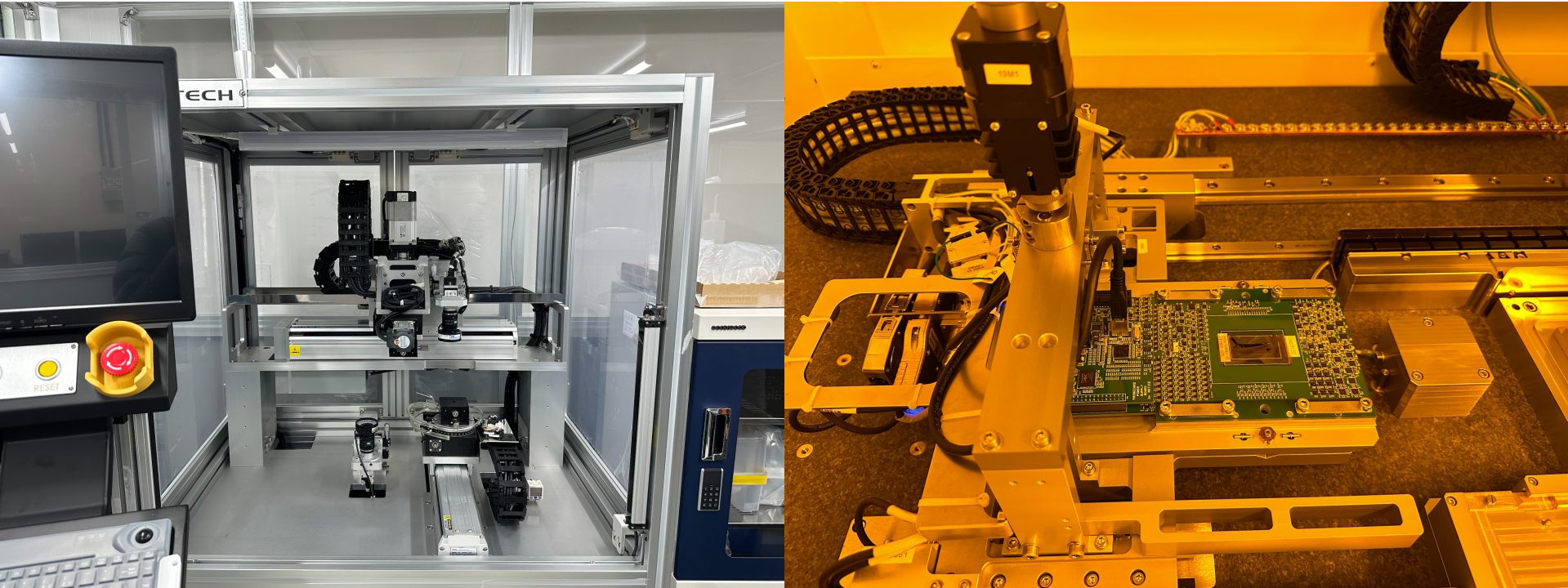
Probe card for AstroPix v3



- Received design files for AstroPix v3 single chip carrier board and bonding pads
- Working with a local company (NOTICE) to design a probe card
- Need single chip carrier boards, bare chips for further development for AstroPix

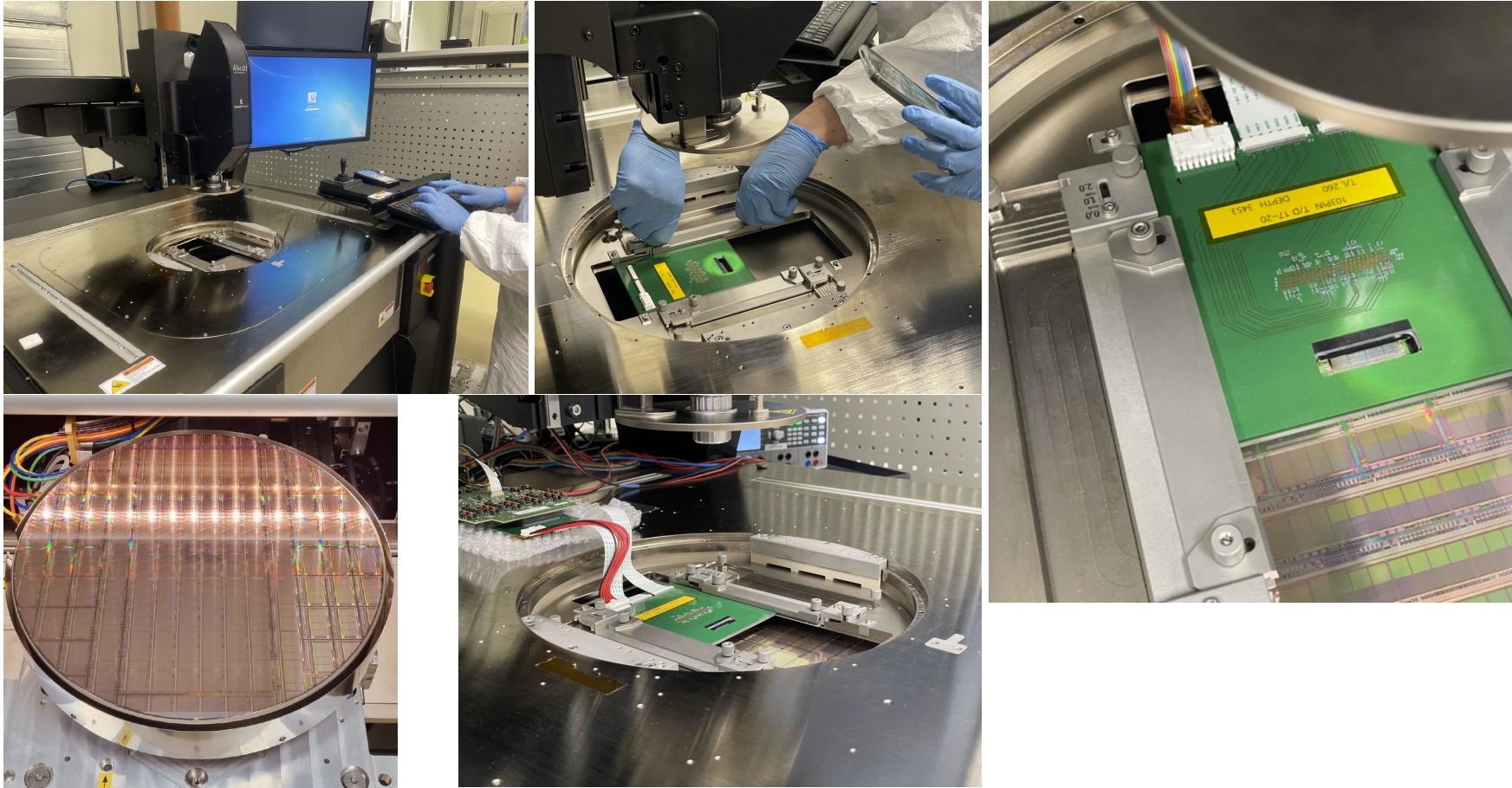
Preparation for development of chip test procedure

- Preparation for a setup to develop the chip test procedure
 - Tune up an automatic chip handler machine for various chip design
 - Plan to verify the performance by comparing it with the reference results (ALPIDE chip tested by ALICIA)
 - Plan to contact the ALICIA manufacturer for customizing



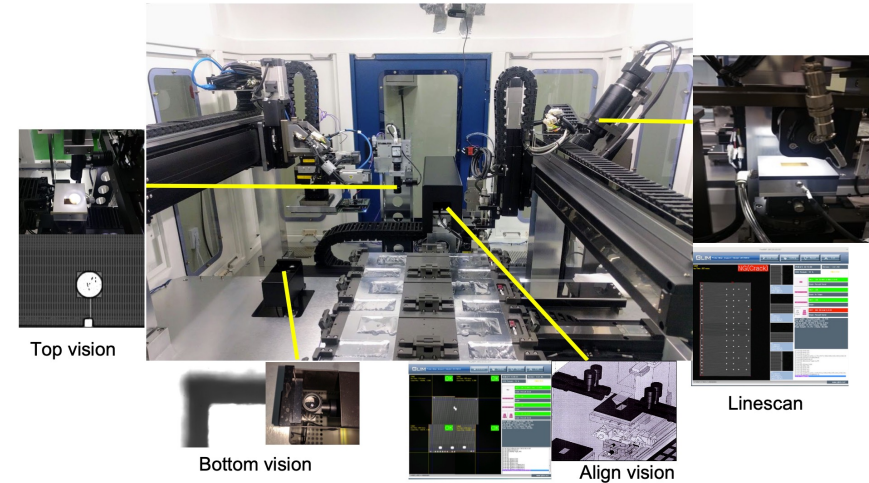
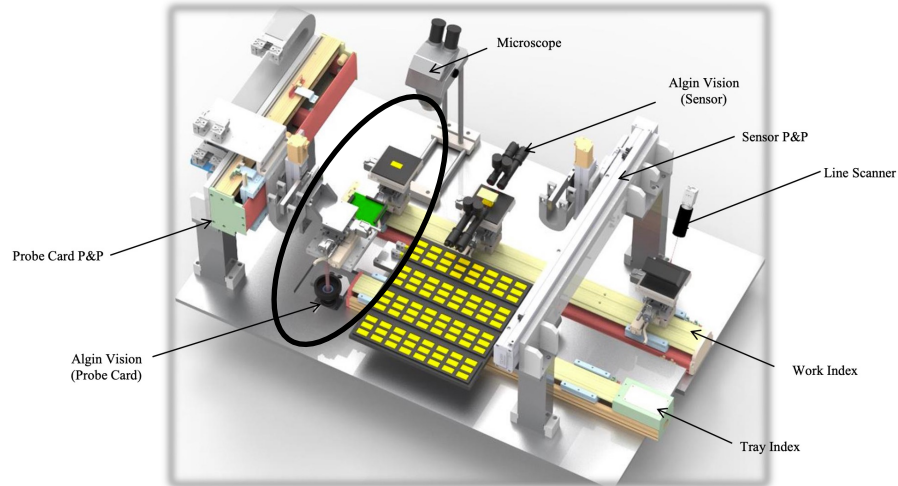
Preparation for development of chip test procedure

- Wafer testing system for ALICE ITS3 at CERN

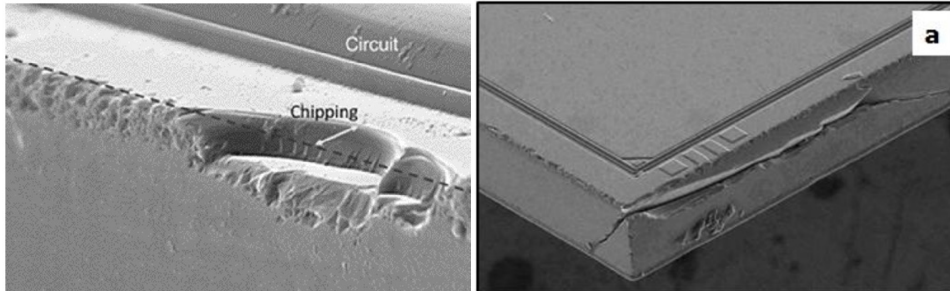


Preparation for development of chip test procedure

- One possible option: chip-level tests with multiple probe cards doing tests in parallel



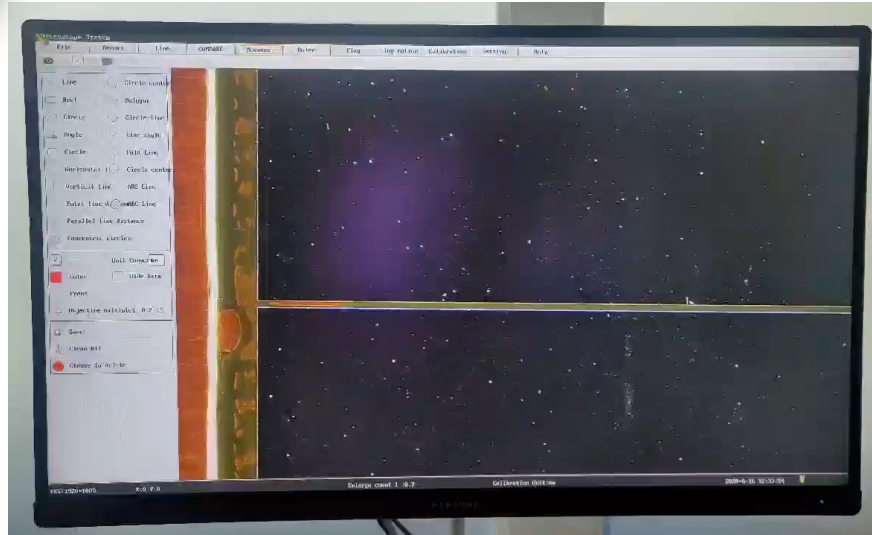
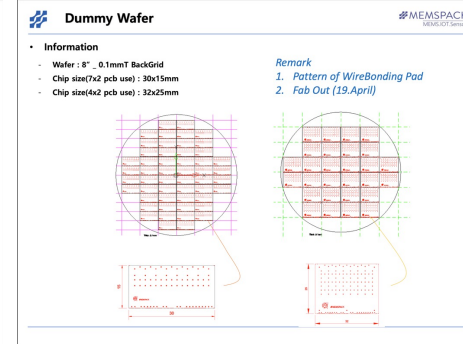
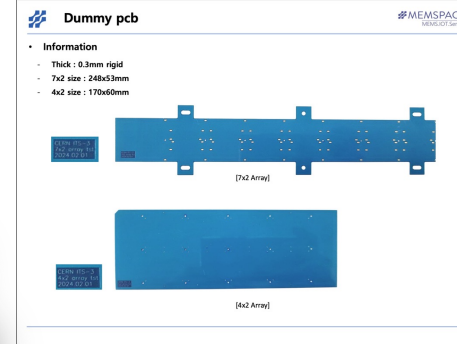
- It depends on the failure rate from dicing



Short update on the module assembly

- Recently produced a few dummy modules of ITS2 OB design with good position precision by a local company

Datacon 2200 evo+



BACKUP